Preliminary Information

- **High performance, low power pipeline burst SRAM**
  - Ultra low power for green PC and battery powered PC
- **High performance**
  - 83-133MHz Speed grades
  - 3-1-1-1 Burst Read
  - 1-1-1-1 Burst Write
  - 3-1-1-1-1-1-1-1... pipeline operation
- **Low power**
  - Low active power
  - Ultra low power ZZ standby mode
  - Single 3.3V supply (V_{DD})
  - Isolated 3.3V or 2.5V I/O supply (V_{DDQ})
- **Compatibility**
  - Individual Byte Write and Global Write masking
  - Interleave and burst address support
  - Three chip enables for easy expansion
  - Industry standard 100-Pin PBSRAM pinout
  - Industry standard PBSRAM specification
- **Applications**
  - Pentium® and PowerPC™ pipelined L2 Cache
  - Ideal for high speed, low power communications buffers
  - Power sensitive portable DSP applications

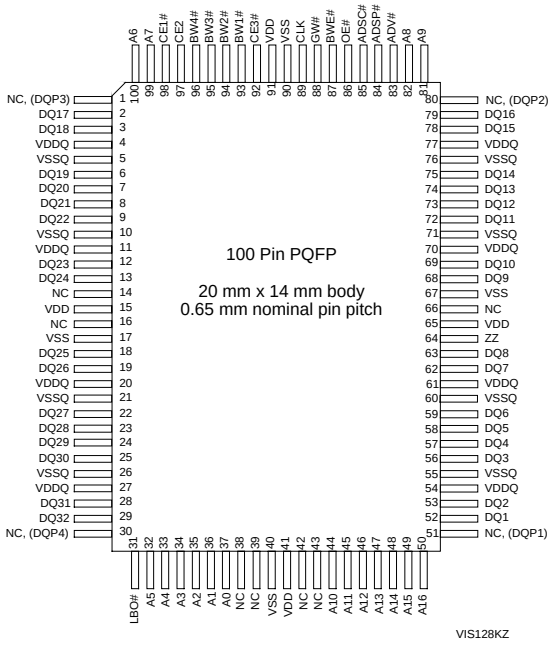

Figure 1. Pin Function

Overview

The MoSys MC803128K and MC80364K are high performance, low power pipeline-burst-SRAMs (PBSRAMs). Fabricated using an advanced low power, high performance CMOS process, the MoSys MC803128K and MC80364K are backward pin and function compatible with standard 32Kx32 PBSRAM with additional operating features like low power ZZ standby mode and linear burst order addressing. These additional operating features are defined so that, with proper implementation, PC boards can work transparently with, 32Kx32, 64Kx32 or 128Kx32 configurations, allowing the designer maximum configuration flexibility within a single footprint layout.

The MoSys MC803128K and MC80364K support PBSRAM operating modes at maximum burst frequency including indefinite pipeline read or write (3-1-1-1-1-1-1...)

The MC803128K and MC80364K are packaged in a standard 100 lead PQFP or TQFP.

Lowest Power

The MC803128K and MC80364K PBSRAMs afford systems dramatic power savings due to the benefits of their proprietary MoSys technology. Peak operating power of typical PBSRAM is 5x that of MC803128K. Making it ideal for portable applications, as well as applications requiring a large amount of RAM.

Part Number Designation

Example*: MC803128K32Q-10*
Device Designation: *MC8*:, Series: *03*
Organization: *128K32*
Package Type: Q=PQFP, L=LQFP
Speed: – 12 83MHz
– 10 100MHz
– 8R5 117MHz
– 7R5 133MHz

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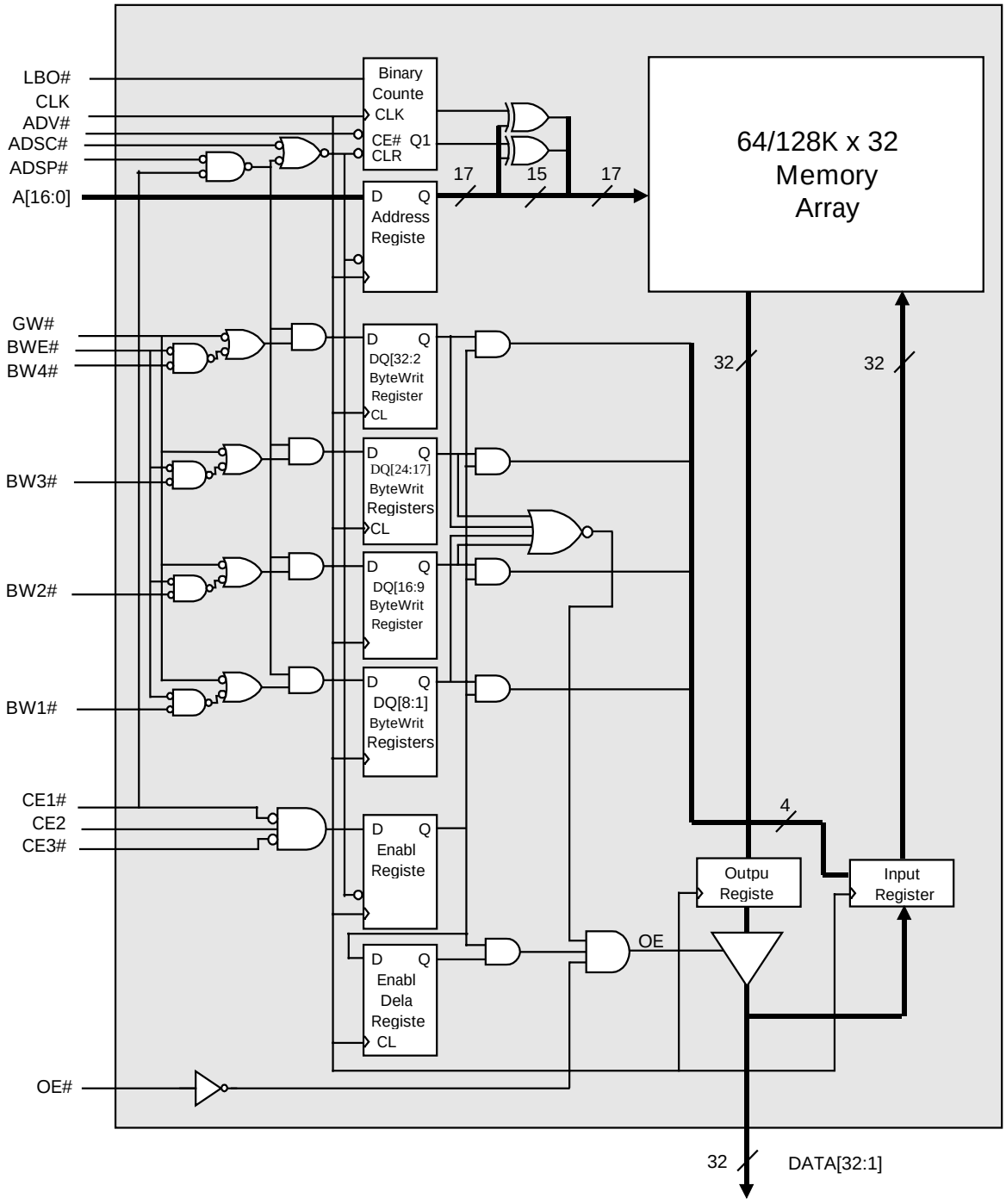

Figure 2 Functional Block Diagram

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Table 1. Pin Description

Pin Number	Symbol	Type	Description
50, 49, 48, 47, 46, 45, 44, 81, 82, 99, 100, 32, 33, 34, 35, 36 ,37	A[16:0]	Input	Processor Addresses
96,95, 94, 93	BW[4:1]#	Input	Processor host bus byte enables.
88	GW#	Input	Global Write from cache controller
87	BWE#	Input	Byte Write Enable from controller
89	CLK	Input	Processor host bus clock
98	CE1#	Input	ADSP# mask and ADSC# chip enable
97	CE2	Input	Depth expansion chip enable
92	CE3#	Input	Depth expansion chip enable
86	OE#	Input	Asynchronous output enable
83	ADV#	Input	Burst address counter advance
84	ADSP#	Input	ADS# of processor
85	ADSC#	Input	ADS# of controller
64	ZZ		Low power sleep mode
31	LBO#		Linear Burst Order
29, 28, 25, 24, 23, 22, 19, 18, 13, 12, 9, 8, 7, 6, 3, 2, 79, 78, 75, 74, 73, 72, 69, 68, 63, 62, 59, 58, 57, 56, 53, 52	DQ[32:1]	I/O	Data I/O pins
30, 1, 80, 51	NC/DQP[4:1]	I/O	Data parity I/O pins
16, 38, 39, 42, 43, 66	NC	-	unused
15, 41, 65, 91	VDD	3.3 Volts	Power
17, 40, 67, 90	VSS	Ground	Ground
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	I/O Sup-ply	I/O Buffer Supply
5, 10, 21, 26, 55, 60, 71, 76	VSSQ	I/O Ground	I/O Buffer Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Core Supply Voltage		3.6	V
V_{DDQ}	I/O Supply Voltage		3.6	V
V_{ih}	Input High Voltage		V_{DDQ} +0.5	V
V_{il}	Input Low Voltage	V_{SSQ}?0.5		V
Ts	Storage Temperature	-65	150	?C

Notes: Max Vih is not to exceed maximum VDDQ

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Table 3. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply Voltage	3.3V +10%/-5%	3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	2.5V +44%/-5%	2.375	3.6	V
V_{ih}	Input High Voltage		1.8	V_{DDQ} + .3	V
V_{il}	Input Low Voltage		-0.3	0.8	V
V_{oh}	Output High Voltage	I_{oh} = -5 mA	2.4		V
V_{ol}	Output Low Voltage	I_{ol} = 5 mA		0.4	V

Table 4. Absolute Maximum AC Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{ih}	Input High Voltage	1.8	V_{DDQ}+1.0	V
V_{il}	Input Low Voltage	V_{SSQ} ? 1.0	0.8	V
tOVR	Overshoot/Undershoot Voltage Duration		0.2*tCY	ns
tSET	Overshoot/Undershoot Settling Time		0.8*tCY	ns

Table 5. Maximum DC Current Requirements

Symbol	Condition	Current	Units
I_{DD}	Operating current, device selected; all inputs ≤ Vil or ≥ Vih; cycle time ≥ tKC min, V_{DD}= max, 0 pF load	50	mA
I_{DD1}	Idle current, device selected; ADSP#, ADSC#, GW#, BW#s, ADV# and all other inputs ≥ 2.8 volts; cycle time ≥ tKC min, V_{DD}= max, 0 pF load	10	mA
I_{DD2}	Clock stopped, all inputs ≥ 2.8 v, V_{DD}= max, 0 pF load	2	mA
I_{DDZ}	Sleep mode, clock stopped, all inputs ≥ 2.8 v, V_{DD}= max	1	mA

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Table 6. AC Timing Characteristics at Recommended Operating Conditions

		-7R5 (133 MHz)		-8R5 (117 MHz)		-10 (100 MHz)		-12 (83 MHz)		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
tAAH	ADV# hold	0.5		0.5		0.5		0.5		ns
tAAS	ADV# setup	2		2		2		2		ns
tADSH	ADSx# hold	0.5		0.5		0.5		0.5		ns
tADSS	ADSx# setup	2		2		2		2		ns
tAH	Address hold	0.5		0.5		0.5		0.5		ns
tAS	Address setup	2		2		2		2		ns
tCEH	Chip Enable hold	0.5		0.5		0.5		0.5		ns
tCES	Chip Enable setup	2		2		2		2		ns
tDH	Write Data hold	0.5		0.5		0.5		0.5		ns
tDS	Write Data setup	2		2		2		2		ns
tKC	Clock cycle	7.5		8.5		10		12		ns
tKH	Clock high	2		2.5		3.2		4		ns
tKL	Clock low	2		2.5		3.2		4		ns
tKQ	Clock to output valid		4.5		5		5.5		6	ns
tKQHZ	Clock to output high-Z	1.5	7.5	1.5	8.6	1.5	10	1.5	12	ns
tKQLZ	Clock to output low-Z	0		0		0		0		ns
tKQX	Clock to output invalid	1.5		1.5		1.5		1.5		ns
tOELZ	OE# to output low-Z	0		0		0		0		ns
tOEHZ	OE# to output high-Z		4.5		4.8		5.5		6	ns
tOEQ	OE# to output valid		4.5		4.8		5.5		6	ns
tOEQX	OE# to output invalid	0		0		0		0		ns
tWS	GW#, BWx# setup	2		2		2		2		ns
tWH	GW#, BWx# hold	0.5		0.5		0.5		0.5		ns
tZZs	ZZ standby		100		100		100		100	ns
tZZREC	ZZ recovery	100		100		100		100		

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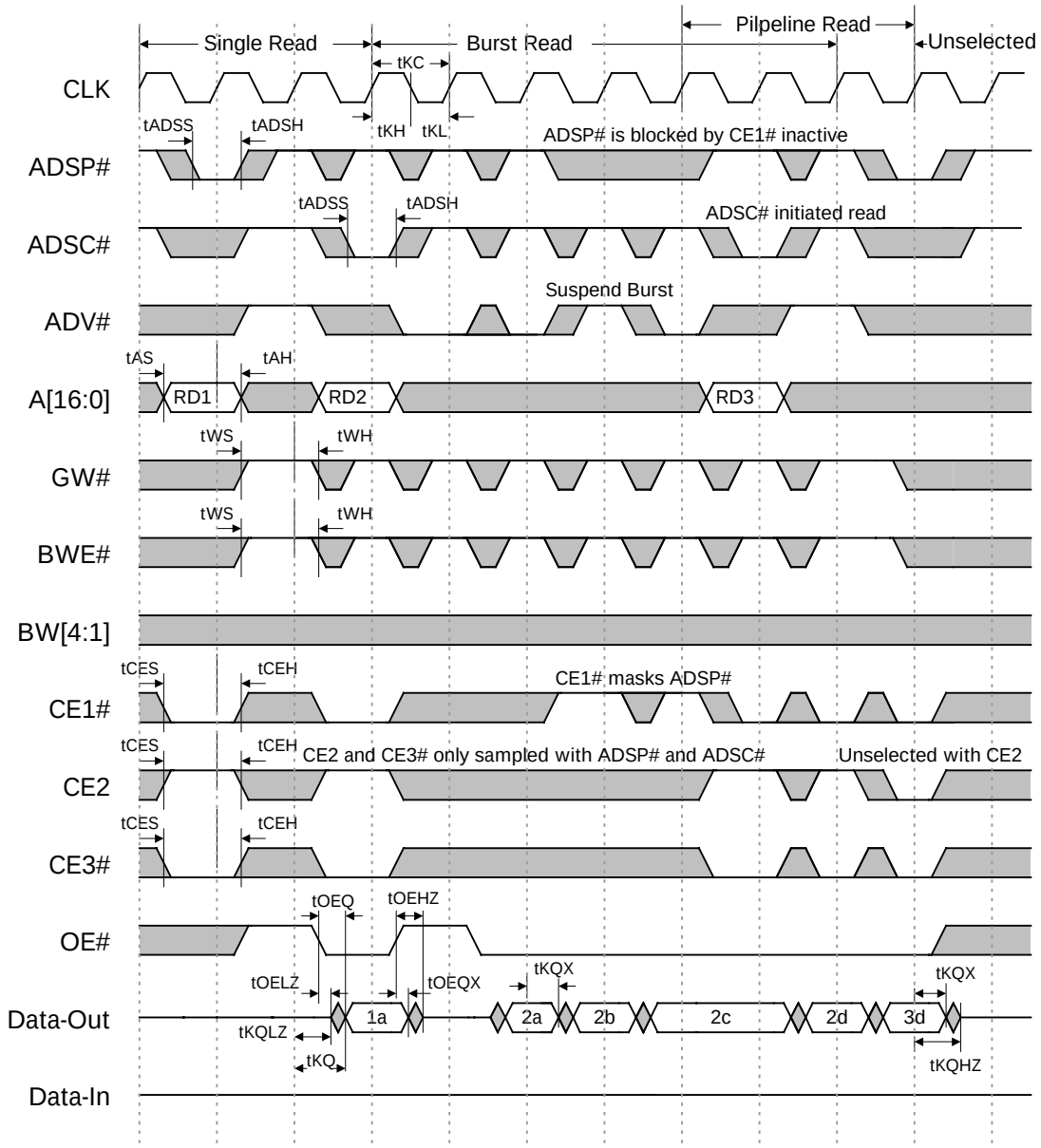

Figure 3 Read Cycle Timing

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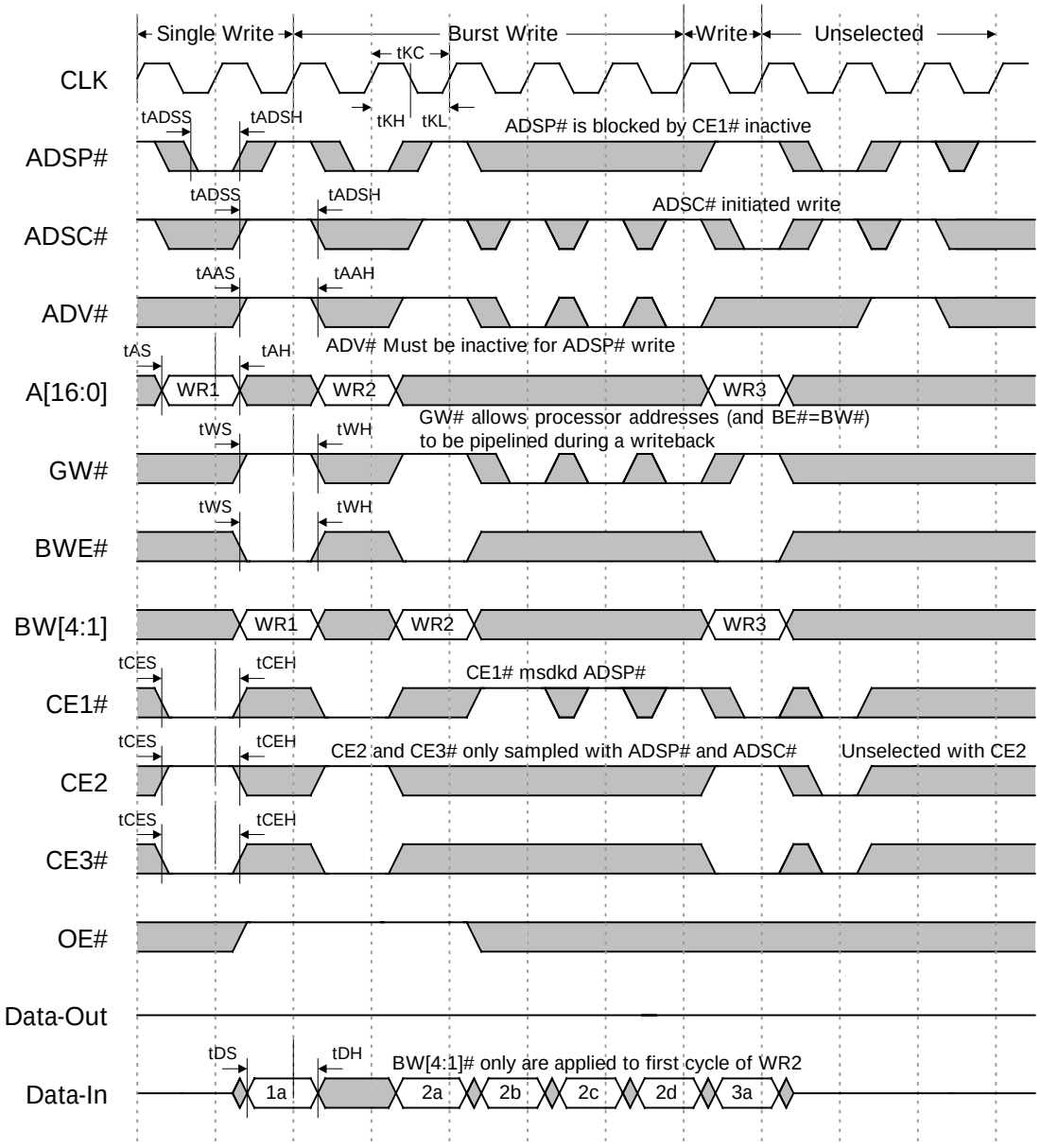

Figure 4 Write Cycle Timing

Preliminary Information

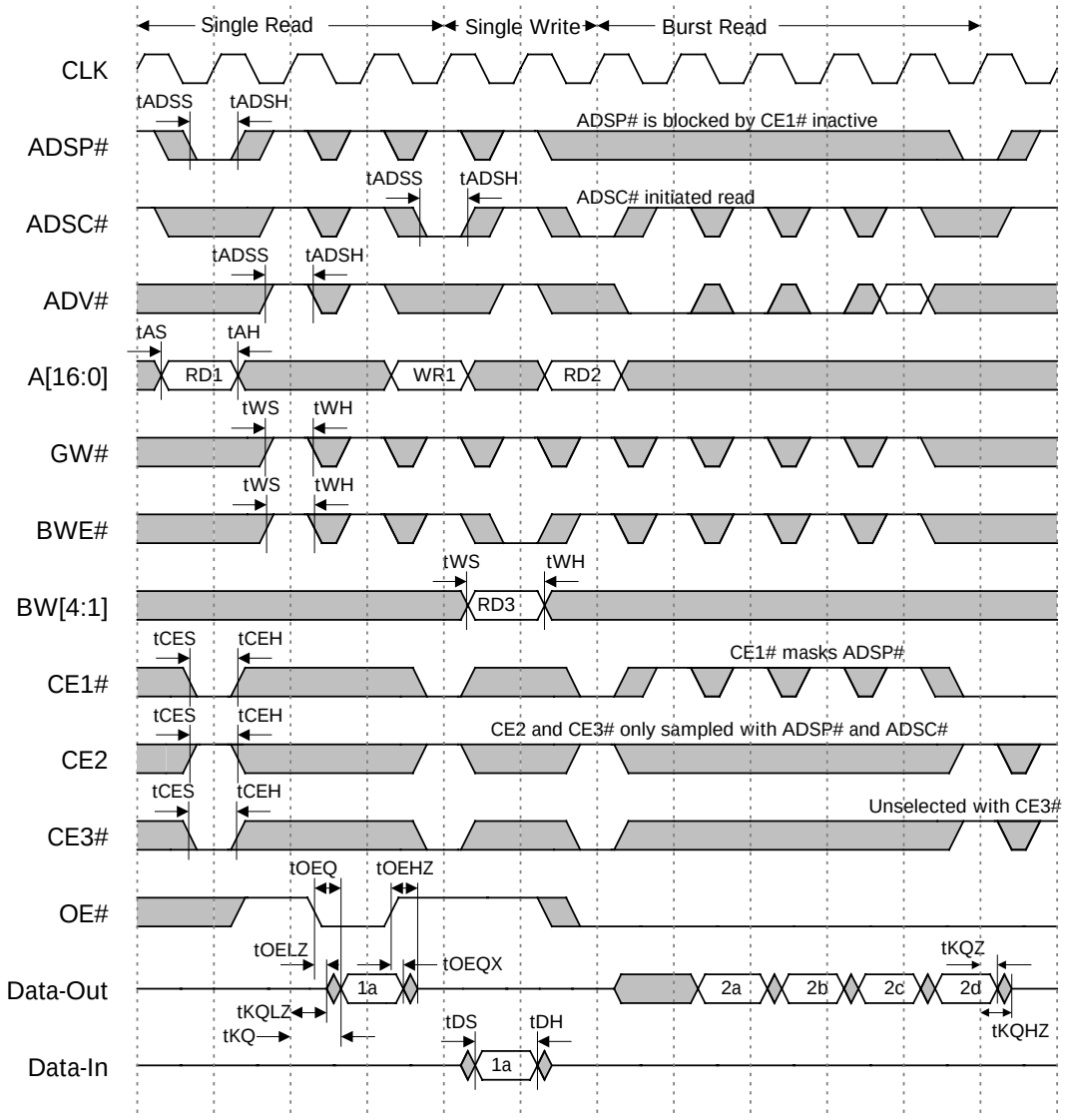

Figure 5 Read/Write Cycle Timing

Preliminary Information

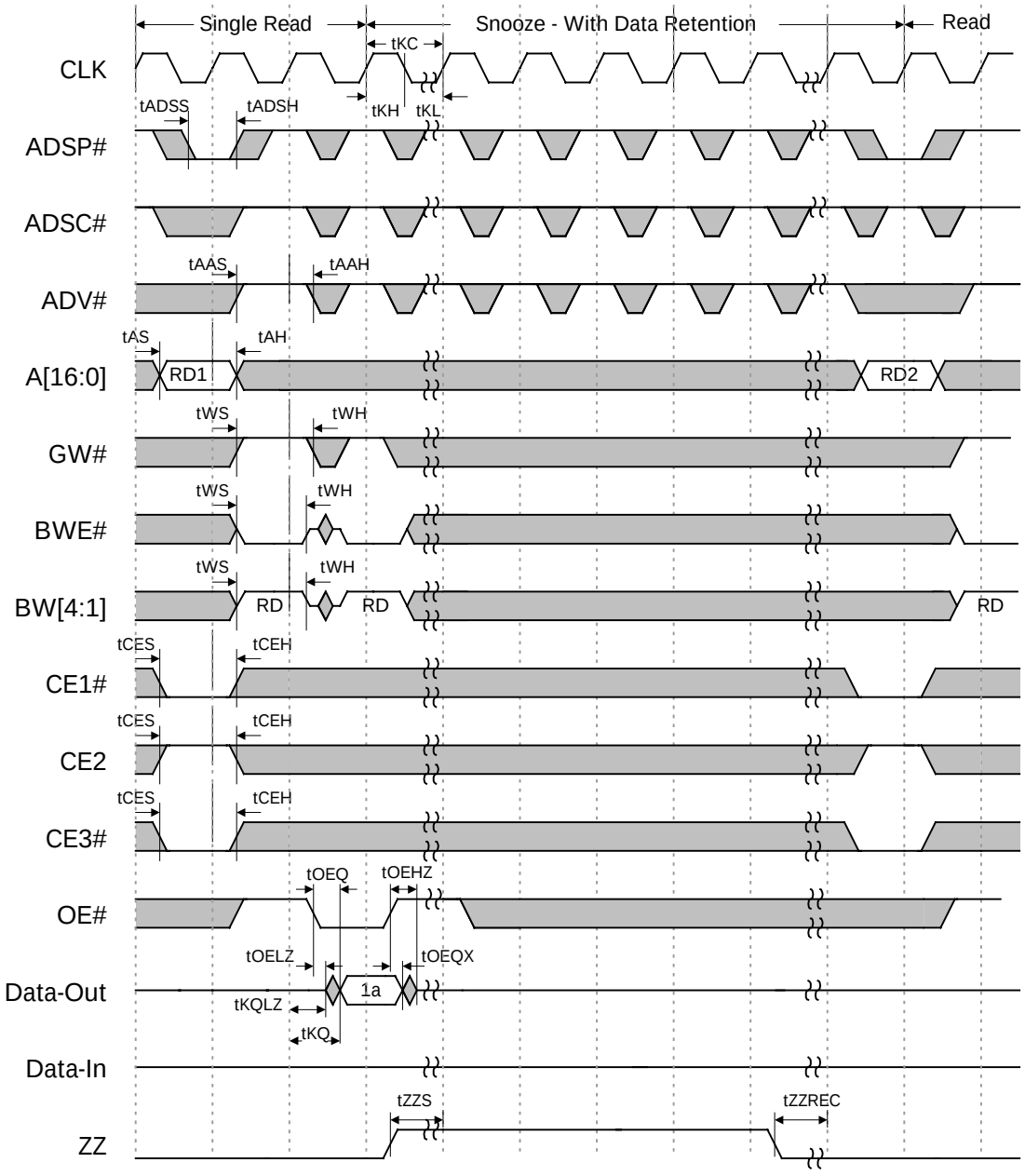

Figure 6 ZZ and RD Timing

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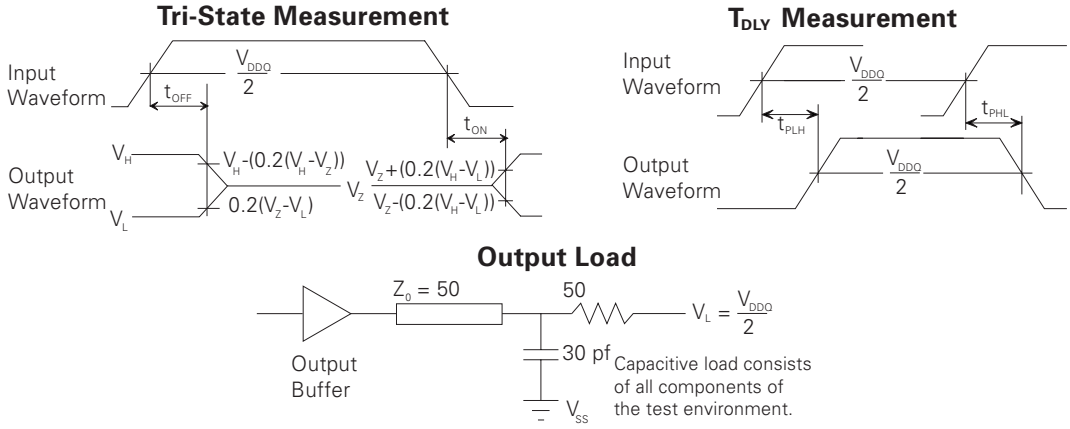
Test and Measurement



Test Structure and Measurement Points

Notes

1. Valid Delay Measurement is made from the VDDQ / 2 on the input waveform to the VDDQ / 2 on the output waveform. Input waveform should have a slew rate of 1V/ns.
2. Tri-state t_{off} measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial to final value VDDQ/2.

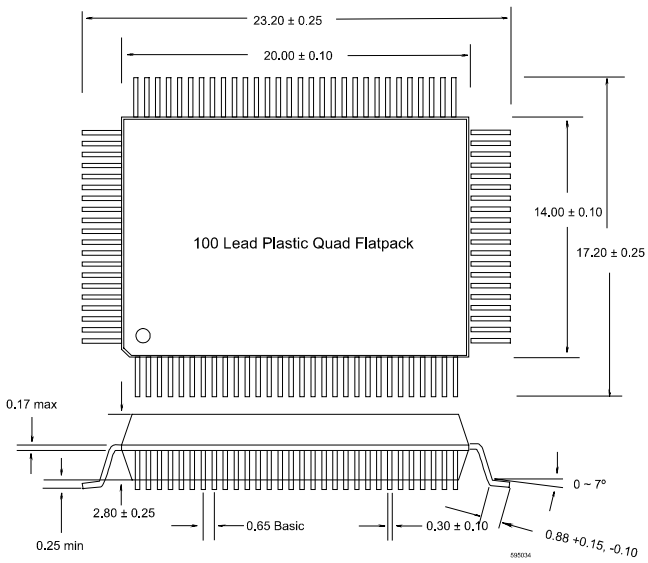


Figure 7. PQFP Mechanical Characteristics

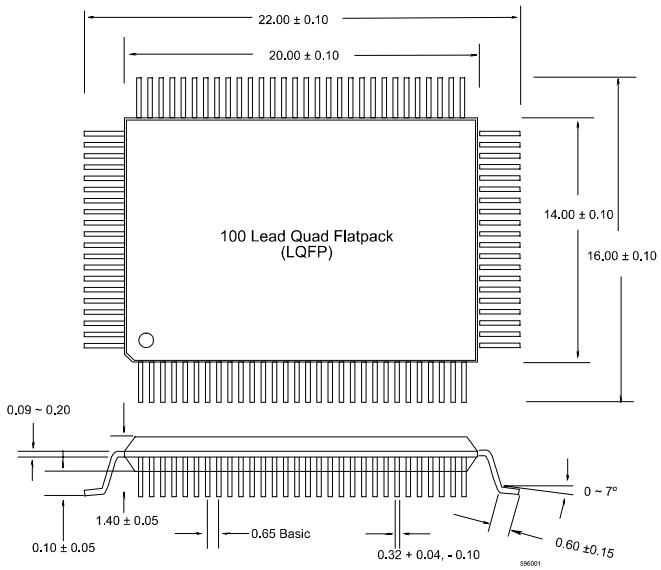


Figure 8. LQFP Mechanical Characteristics