

## PIC16C73A Rev. A Silicon Errata Sheet

The PIC16C73A (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30390E), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C73A silicon.

### 1. Module: 8-bit A/D Module

If the Analog Port is configured so that all analog pins are digital inputs (PCFG2:PCFG0 = 11xb), then doing a conversion on any pin of the analog port will give a result of ADRES = 0xFF.

#### Work Around

Configure the PCFG2:PCFG0 bits to a value that has any pin of the analog port configured as an analog input (such as PCFG2:PCFG0 = 100b). Conversion on any pin of the analog port (analog or digital) will now convert as expected.

### 2. Module: CCP (Compare Mode)

The Compare mode may not operate as expected when configuring the compare match to drive the I/O pin low (CCPxM<3:0> = 1001).

When the CCP module is changed to compare output low (CCPxM<3:0> = 1001) from any other non-compare CCP mode, the I/O pin will immediately be driven low regardless of the state of the I/O data latch. The pin will remain low when the compare match occurs (see Table 1).

However, when the CCP module is changed to compare output high (CCPxM<3:0> = 1000) from any other CCP mode, the I/O pin will immediately be driven low regardless of the state of the I/O data latch. The pin will be driven high when the compare match occurs.

**TABLE 1: Compare Output Low Switching**

CCP Mode CCPxM<3:0> =	I/O pin State	Change CCP to CCPxM<3:0> =	
		1001	1000
0xxx	H	L	L
	L	L	L
1000	H	H	—
	L	L	—
1001	H	—	L
	L	—	L
101x	H	L	L
	L	L	L
11xx	H	L	L
	L	L	L

#### Work Around

To have the I/O pin high until the compare match low occurs, force a compare match high to get the I/O pin into the high state, then reconfigure the compare match to force the I/O low, when the compare condition occurs.

**Note:** As with any windowed EPROM device, please cover the window at all times, except when erasing.

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## 3. Module: CCP (Compare Mode)

The special event trigger of the Compare mode may not occur if both of the following conditions exist:

- An instruction one cycle (Tcy) prior to a Timer1/Compare register match has literal data equal to the address of a CCP register being used.<sup>(1)</sup>
- An instruction in the same cycle as a Timer1/Compare register match has an MSb of '0'.

The interrupt for the compare event will still be generated, but no special event trigger will occur.

**Note 1:** 15h(CCP1L), 16h(CCP1H) or 17h(CCP1CON) for CCP1; 1Bh(CCP2L), 1Ch(CCP2H) or 1Dh(CCP2CON) for CCP2.

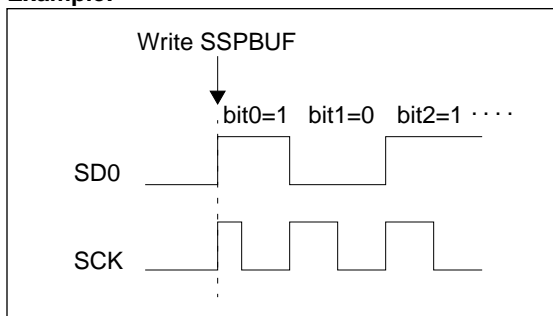
### Work Around

Use the interrupt service routine instead of using the special event trigger to reset Timer1 (and start an A/D conversion, if applicable).

## 4. Module: SSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter-than-expected SCK pulse may occur on the first bit of the transmitted/received data.

### Example:



### Work Around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit, and then turn Timer2 back on.

### Example Code:

```
BSF STATUS, RP0      ;Bank 1
LOOP BTFSS SSPSTAT, BF ;Data received?
                        ;(Xmit complete?)
GOTO LOOP             ;No
BCF STATUS, RP0      ;Bank 0
MOVF SSPBUF, W        ;W = SSPBUF
MOVWF RXDATA          ;Save in user RAM
MOVF TXDATA, W        ;W = TXDATA
BCF T2CON, TMR2ON     ;Timer2 off
CLR TMR2              ;Clear Timer2
MOVWF SSPBUF          ;Xmit New data
BSF T2CON, TMR2ON     ;Timer2 on
```

## 5. Module: SSP Module (I<sup>2</sup>C™ mode)

If the bus is active when the I<sup>2</sup>C mode is enabled, and the next 8-bits of data on the bus match the address of the device, then the SSP module will generate an acknowledge pulse.

### Work Around

Before enabling the I<sup>2</sup>C mode, ensure that the bus is not active.

## 6. Module: Timer0

The TMR0 register may increment when the WDT postscaler is switched to the Timer0 prescaler. If TMR0 = FFh, this will cause TMR0 to overflow (setting T0IF).

### Work Around

Follow the following sequence:

- a) Read the 8-bit TMR0 register into the W register
- b) Clear the TMR0 register
- c) Assign WDT postscaler to Timer0
- d) Write W register to TMR0

## 7. Module: Timer1

The Timer1 value may unexpectedly increment if either the TMR1H or the TMR1L register is written. If Timer1 is ON, then turned OFF, performing any write instruction with TMR1H as the destination may cause TMR1L to increment.

### Example 1:

```
BSF T1CON, TMR1ON
:
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:

TMR1H:TMR1L = 3F:00

TMR1 value after MOVF instruction:

TMR1H:TMR1L = 3F:01

### Example 2:

```
BSF T1CON, TMR1ON
:
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:

TMR1H:TMR1L = FF:FF

TMR1 value after MOVF instruction:

TMR1H:TMR1L = FF:00

If Timer1 is ON, then turned OFF when TMR1H:TMR1L = xx:FF, performing any write instruction with TMR1L as the destination may cause TMR1H to increment.

Example 3:

```
BSF T1CON, TMR1ON
:
BCF T1CON, TMR1ON
CLR F TMR1L
```

TMR1 value before CLR F instruction:

TMR1H:TMR1L = FF:FF

TMR1 value after CLR F instruction:

TMR1H:TMR1L = 00:00

(TMR1IF is **not** set.)

## Work Around

To preserve Timer1 register values:

Read Timer1 register values into “shadow” registers. Perform any write instruction(s) on the shadow registers. Write the shadow register values back into the Timer1 registers.

## **8. Module: USART**

When the USART (SCI) is configured in asynchronous mode with the BRGH bit set, a high number of receive errors may be experienced. For asynchronous receive operations it is recommended that the USART be configured with the BRGH bit cleared.

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## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30390E), the following clarifications and corrections should be noted.

## 1. Module: I/O Ports

The specification for the High Voltage Open Drain I/O (The RA4 pin on most devices) cannot be met without possible long term reliability issues on that I/O pin. If a high voltage drive is required, use an external transistor that can support the required voltage.

**TABLE 2: DC SPECIFICATION CHANGES FROM DATA SHEET**

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D150	VOD	Open-drain High Voltage	—	—	<b>10</b>	—	—	14	V

## 2. Module: 8-Bit A/D

- a) The minimum A/D reference voltage has been improved to the values shown in Table 3.

**TABLE 3: DC SPECIFICATION CHANGES FROM DATA SHEET**

Parm No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
A20	VREF	Reference Voltage	2.5 *	—	VDD + 0.3 V	3.0	—	VDD + 0.3 V	V

\* This parameter is characterized but not tested

## 3. Module: SSP (SPI Mode Timing Specifications)

- a) The SPI interface timings have been modified to the values shown in Table 3.

**TABLE 4: DC SPECIFICATION CHANGES FROM DATA SHEET**

Parm No.	Sym.	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
71	Tsch	SCK input high time (slave mode)	Continuous	1.25 TCY + 30 ns	—	—	TCY + 20 ns	—	—	ns
71A			Single Byte <sup>(1)</sup>	40	—	—	N.A.			ns
72	TscL	SCK input low time (slave mode)	Continuous	1.25 TCY + 30 ns	—	—	TCY + 20 ns	—	—	ns
72A			Single Byte <sup>(1)</sup>	40	—	—	N.A.			ns
73A	TB2B	Last clock edge of the Byte1 to 1st clock edge of the Byte2 <sup>(1)</sup>		1.5 TCY + 40 ns	—	—	N.A.			ns

\* This parameter is characterized but not tested

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.

## 4. Module: Timer1

- a) The operation of Timer1 needs some clarification when the timer registers are written when the TMR1ON bit is set.

The internal clock signal that is the input to the TMR1 prescaler affects the incrementing of Timer1 (TMR1H:TMR1L registers and the Timer1 prescaler). When the Timer1 registers are NOT written, the Timer1 will increment on the rising edge of the TMR1 increment clock.

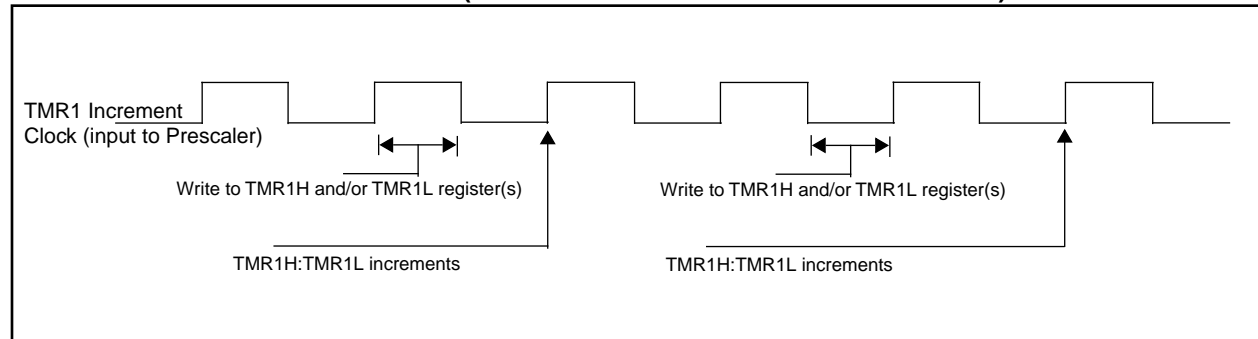
When the TMR1H and/or TMR1L registers are written while this clock is high, TMR1 will increment on the next rising edge of this clock.

When the TMR1H and/or TMR1L registers are written while this clock is low, TMR1 will not increment on the next rising edge of this clock, but must first have a falling clock and the rising clock for TMR1 to increment.

Figure 1 shows the two cases of writes to the TMR1H and/or TMR1L registers. Due to the  $V_{IH}$  and  $V_{IL}$  thresholds on the oscillator/clock pins, external Timer1 oscillator components, and external clock frequency, the Timer1 increment clock may not be of a 50% duty cycle.

The TMR1 increment clock is out of phase of the T1OSO/T1CKI pin by a small propagation delay.

**FIGURE 1: WRITES TO TIMER1 (EXTERNAL CLOCK / OSCILLATOR MODE)**



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## 5. Module: RC Oscillator

The table for RC Oscillator Frequencies in the Device Characterization section of the Data Sheet is incorrect. The correct characterization information is shown in Table 5.

**TABLE 5: RC OSCILLATOR FREQUENCIES CHARACTERIZATION CHANGES FROM DATA SHEET**

Cext	Rext	Correct Characterization Data		Current Data Sheet Values	
		Average	% Variation	Average	% Variation
22 pF	5.1 K	3.55 MHz	± 9.63%	4.12 MHz	± 1.4%
	10 K	1.99 MHz	± 10.53%	2.35 MHz	± 1.4%
	100 K	221.9 KHz	± 12.10%	268 KHz	± 1.1%
100 pF	3.3 K	1.77 MHz	± 10.67%	1.80 MHz	± 1.0%
	5.1 K	1.22 MHz	± 10.41%	1.27 MHz	± 1.0%
	10 K	669.4 KHz	± 10.92%	688 KHz	± 1.2%
	100 K	71.5 KHz	± 11.21%	77.2 KHz	± 1.0%
330 pF	3.3 K	625.1 KHz	± 10.68%	707 KHz	± 1.4%
	5.1 K	428.5 KHz	± 10.96%	501 KHz	± 1.2%
	10 K	231.9 KHz	± 11.32%	269 KHz	± 1.6%
	100 K	24.4 KHz	± 12.93%	28.3 KHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from the average value for Vdd = 5V





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18201 Von Karman, Suite 1090  
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Tel: 714-263-1888 Fax: 714-263-1338

#### New York

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150 Motor Parkway, Suite 202  
Hauppauge, NY 11788  
Tel: 516-273-5305 Fax: 516-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

### AMERICAS (continued)

#### Toronto

Microchip Technology Inc.  
5925 Airport Road, Suite 200  
Mississauga, Ontario L4V 1W1, Canada  
Tel: 905-405-6279 Fax: 905-405-6253

### ASIA/PACIFIC

#### Hong Kong

Microchip Asia Pacific  
RM 3801B, Tower Two  
Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2-401-1200 Fax: 852-2-401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
No. 6, Legacy, Convent Road  
Bangalore 560 025, India  
Tel: 91-80-229-0061 Fax: 91-80-229-0062

#### Japan

Microchip Technology Intl. Inc.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa 222-0033 Japan  
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

#### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

#### Shanghai

Microchip Technology  
RM 406 Shanghai Golden Bridge Bldg.  
2077 Yan'an Road West, Hong Qiao District  
Shanghai, PRC 200335  
Tel: 86-21-6275-5700 Fax: 86 21-6275-5060

### ASIA/PACIFIC (continued)

#### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore 188980  
Tel: 65-334-8870 Fax: 65-334-8850

#### Taiwan, R.O.C

Microchip Technology Taiwan  
10F-1C 207  
Tung Hua North Road  
Taipei, Taiwan, ROC  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Winkers Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44-1189-21-5858 Fax: 44-1189-21-5835

#### France

Arizona Microchip Technology SARL  
Zone Industrielle de la Bonde  
2 Rue du Buisson aux Fraises  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Arizona Microchip Technology GmbH  
Gustav-Heinemann-Ring 125  
D-81739 München, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Arizona Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-39-6899939 Fax: 39-39-6899883

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