PIC17C42

Errata Sheet for PIC17C42 Rev. C Silicon

The PIC17C42 (Rev. C) parts that you have received conform to the preliminary data sheet (DS30073C), except for the anomalies described below.

1. The Watchdog Timer (WDT) does not operate as documented for sleep mode, when the Oscillator Start-Up Timer (OST) is enabled (in LF or XT crystal mode). Regardless of the mode of the WDT (enabled or disabled), if the SLEEP instruction was executed when the WDT is greater than or equal to 50% of the time-out period, any interrupt that wakes the processor will cause a WDT reset.

Work-arounds

a) For the case where the WDT is disabled. Before executing the SLEEP instruction, ensure that the WDT has timed-out. This can be done by monitoring the $\overline{TO}$ bit for when it goes from set to clear. Sample code for this test is shown below. The first bit test determines if the WDT has cleared the $\overline{TO}$ bit yet. If the $\overline{TO}$ bit is cleared, the state of the WDT is unknown and must be cleared, This sets the $\overline{TO}$ bit so the WDT roll-over can be observed.

```
      BTFSS  CPUSTA, TO  ; TO = 0?
      CLRWDT            ; YES, WDT = 0
LOOP  BTFSC  CPUSTA, TO  ; WDT rollover?
      GOTO   LOOP        ; NO, wait
      SLEEP              ; YES, goto sleep
```

b) For both the WDT enabled and disabled. Ensure that the CLRWDT instruction is executed before the WDT increments past 50% of the WDT period.

c) Use EC or RC oscillator modes

2. When the clock source of Timer1, Timer2, or Timer3 is selected to external clock, The overflow interrupt flag of the timer will be set twice. Once when the timer value equals the period register, and a second time when the timer value is reset to 0h (this is the correct flag). If the interrupt latency to clear the timer interrupt flag bit is greater than the time to the next timer clock pulse, no problems will be noticed. If the interrupt latency to clear the timer interrupt flag bit is less than the time to the next timer clock pulse, the interrupt will be serviced twice.

Work-arounds

a) While in the Interrupt Service Routine, ensure that the timer has rolled over to 0h before clearing the flag bit.

b) If the time before the next clock is great, have a flag bit which indicates that the Interrupt Service Routine should ignore the first occurrence of the timer interrupt.

c) Clear the timer in software. Doing this causes the period to be one timer count less then expected.

Clarifications / Corrections to the Data Sheet

1. The XT and LF oscillator ranges have been respecified. The typical IDD curves will correlate to the devices if the new oscillator option is used for the desired frequency range. This is shown in Table 1.

TABLE 1: OSCILLATOR FREQUENCY OPTIONS

Old Spec.		New Spec.		Oscillator Fuse Option
Min	Max	Min	Max	
DC	200 KHz	DC	2 MHz	LF mode
200 KHz	25 MHz	2 MHz	25 MHz	XT mode

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11/01/94