PIC16C73B

PIC16C73B Rev. A Silicon Errata Sheet

The PIC16C73B (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30605**A**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C73B silicon.
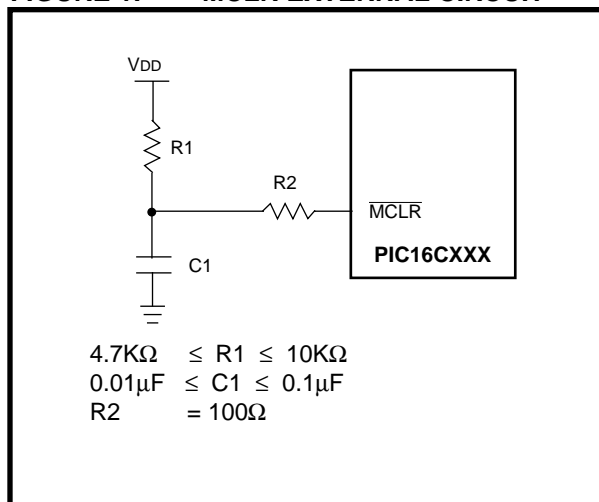
1.   Module: RESET

The minimum specification for the $\overline{\text{MCLR}}$ must be met in order to RESET the PIC16CXXX. If a $\overline{\text{MCLR}}$ pulse occurs that is less that the minimum specification (parameter #30), improper device operation can occur.

If the Minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the $\overline{\text{MCLR}}$ pin.

<u>Work Around</u>

A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desire operation over the applications operating conditions

FIGURE 1: $\overline{\text{MCLR}}$ **EXTERNAL CIRCUIT**

$$4.7\text{K}\Omega \quad \leq \text{R1} \leq 10\text{K}\Omega$$
$$0.01\mu\text{F} \quad \leq \text{C1} \leq 0.1\mu\text{F}$$
$$\text{R2} \quad = 100\Omega$$

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

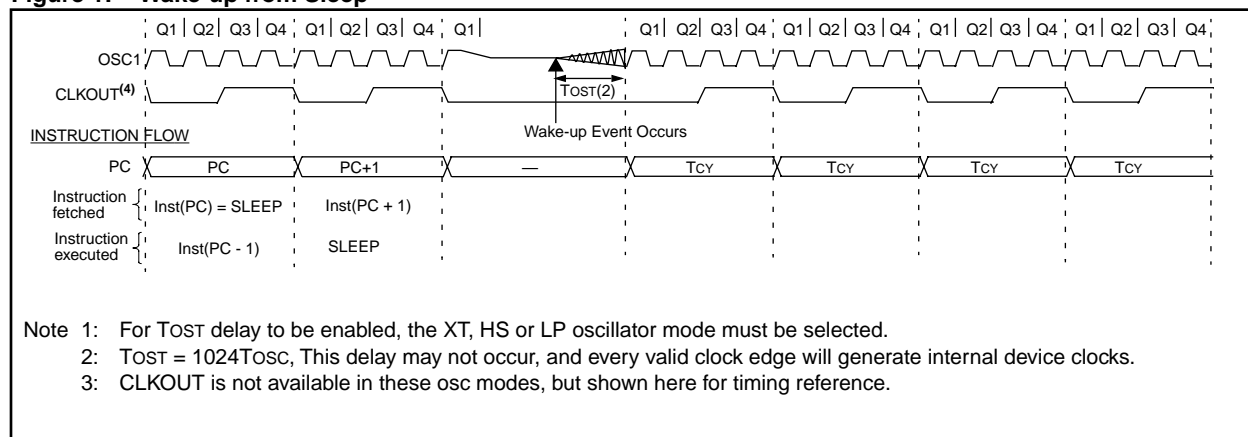# PIC16C73B

2. Module: OSCILLATOR

The Oscillator Start-up Timer (T_{OST}) delay may not occur when the device wakes-up from sleep.

Figure 1 shows the start-up of the crystal after the event that causes the device to wake up from sleep mode (as specified in device data sheet). The start-up time (T_{OST}) may not occur.

The events that wake-up the device from sleep are:

• An interrupt
• A WDT overflow (wake-up)
• A Brown-out Reset
• A $\overline{MCLR}$ reset

Figure 1:   Wake-up from Sleep

Note 1:   For T_{OST} delay to be enabled, the XT, HS or LP oscillator mode must be selected.
        2:   T_{OST} = 1024T_{OSC}, This delay may not occur, and every valid clock edge will generate internal device clocks.
        3:   CLKOUT is not available in these osc modes, but shown here for timing reference.

In applications where time based measurements are started immediately after wake-up from sleep, the suggested work around should be implemented.

Work Around

After the SLEEP instruction, do a software delay of 256 T_{CY} (same as 1024 T_{OSC}). At the Reset and Interrupt vector addresses, test to see if the device woke from sleep (the $\overline{TO}$ and $\overline{PD}$ bits), and if the device did wake from sleep, ensure that the total cycle delay is 256 T_{CY}.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30605**A**), the following clarifications and corrections should be noted.

    none

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