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## Errata Sheet for Rev. B PIC16C71 Silicon

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The PIC16C71 (Rev. B) parts you have received conform functionally to the PIC16C7x preliminary data sheet (DS30390A), except for the anomalies described below.

All the problems listed here will be addressed in the future revisions of the PIC16C71 silicon.

1. The internal Power-On Reset pulse may not generate the power-up timer, time-out delay. This means that the EPROM could be accessed before the device reaches a valid operational V<sub>DD</sub> voltage. The master clear (**MCLR**) pin should be held at low level (device in reset), until a valid device V<sub>DD</sub> operating voltage is reached.
2. When the device oscillator is in RC mode and the A/D clock source is the internal RC, the A/D may generate an erroneous result (in the ADRES register). The erroneous value is typically around 00h or around FFh.

### Work-arounds

The use of one or more of the following techniques will allow the proper results to be obtained.

1. Start the A/D conversion, then immediately place the device into sleep mode.
2. Select an A/D clock source that is derived from TOSC (that is: TOSC/2, TOSC/8, or TOSC/32).
3. Ensure that proper noise reduction design techniques are used, such as using bypass capacitors from V<sub>DD</sub> to V<sub>SS</sub>.

### Clarifications / Corrections to the Data Sheet:

None

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