PIC16C65A

Errata Sheet for Rev. B PIC16C65A Silicon

The PIC16C65A (Rev. B) parts you have received conform functionally to the PIC16C6X data sheet (DS30234**C**), except for the anomalies described below.

All the problems listed here will be addressed in the future revisions of the PIC16C65A silicon.

1. Module: USART

   When the USART (SCI) is configured in asynchronous mode with the BRGH bit set, a high number of receive errors may be experienced. For asynchronous receive operations it is recommended that the USART be configured with the BRGH bit cleared.

2. Module: CCP

   The special event trigger of the Compare mode may not occur if both of the following conditions exist:

   - An instruction one cycle (T_{CY}) prior to a Timer1/ Compare register match has literal data equal to the address of a CCP register being used.*
   - An instruction in the same cycle as a Timer1/ Compare register match has an MSb of '0'.

   The interrupt for the compare event will still be generated, but no special event trigger will occur.

   * 15h(CCPR1L), 16h(CCPR1H) or 17h(CCP1CON) for CCP1; 1Bh(CCPR2L), 1Ch(CCPR2H) or 1Dh(CCP2CON) for CCP2.

   Work Around

   Use the interrupt service routine instead of using the special event trigger to reset Timer1 (and start an A/D conversion, if applicable).

3. Module: Timer1

   The Timer1 value may unexpectedly increment if either the TMR1H or the TMR1L register is written.

   If Timer1 is ON, then turned OFF, performing any write instruction with TMR1H as the destination may cause TMR1L to increment.

   Example 1:

```
BSF T1CON, TMR1ON
          :
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

   TMR1 value before MOVF instruction:
   TMR1H:TMR1L = 3F:00
   TMR1 value after MOVF instruction:
   TMR1H:TMR1L = 3F:01

   Example 2:

```
BSF T1CON, TMR1ON
          :
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

   TMR1 value before MOVF instruction:
   TMR1H:TMR1L = FF:FF
   TMR1 value after MOVF instruction:
   TMR1H:TMR1L = FF:00

   If Timer1 is ON, then turned OFF when TMR1H:TMR1L = xx:FF, performing any write instruction with TMR1L as the destination may cause TMR1H to increment.

   Example 1:

```
BSF T1CON, TMR1ON
          :
BCF T1CON, TMR1ON
CLRF TMR1L
```

   TMR1 value before CLRF instruction:
   TMR1H:TMR1L = FF:FF
   TMR1 value after CLRF instruction:
   TMR1H:TMR1L = 00:00
   (TMR1IF is **not** set.)

   Work Around

   To preserve Timer1 register values:

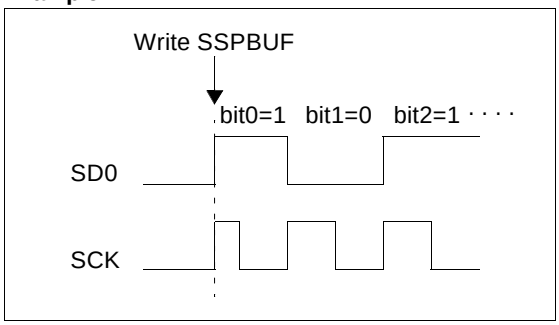
   Read Timer1 register values into "shadow" registers. Perform any write instruction(s) on the shadow registers. Write the shadow register values back into the Timer1 registers.

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

4. Module: SSP

When the SPI is using Timer2/2 as the clock source, a shorter-than-expected SCK pulse may occur on the first bit of the transmitted/received data.

Example:



Work Around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit, and then turn Timer2 back on.

Example Code:

```
     BSF   STATUS, RP0    ;Bank 1
LOOP BTFSS SSPSTAT, BF    ;Data received?
                          ;(Xmit complete?)
     GOTO  LOOP           ;No
     BCF   STATUS, RP0    ;Bank 0
     MOVF  SSPBUF, W      ;W = SSPBUF
     MOVWF RXDATA         ;Save in user RAM
     MOVF  TXDATA, W      ;W = TXDATA
     BCF   T2CON, TMR2ON  ;Timer2 off
     CLR   TMR2           ;Clear Timer2
     MOVWF SSPBUF         ;Xmit New data
     BSF   T2CON, TMR2ON  ;Timer2 on
```

Clarifications/Corrections to the Data Sheet:

In the PIC16C6X Data Sheet (DS30234**C**), the following clarifications and corrections should be noted.

NONE