PIC16C64

Errata Sheet of Rev. B PIC16C64 Silicon

The PIC16C64 (Rev. B) parts you have received conform functionally to the PIC16C6X preliminary data sheet (DS30234**C**), except for the anomalies described below.

All the problems listed here will be addressed in the future revisions of the PIC16C64 silicon.

1. Module: SSP

   When using the SPI, the master mode with clock = OSC/64 does not function correctly (at any voltage).

2. Module: SSP

   When using the I²C™, in the master mode, the TRISC<4:3> bits will NOT manipulate the corresponding SCL and SDA pins. Note that in slave mode the device will drive out the proper levels.

Work-around:

For the SDA pin.

To control the level of the SDA pin, connect an additional I/O pin to the SDA pin. Use this additional I/O pin to control the output for the master data (via the TRIS and PORT bits of that pin). Note that since a general purpose I/O pin is now controlling the output data, the SDA will not have slope control.

For the SCL pin.

To control the level of the SCL pin, use the CKP bit (SSPCON<4>). The SCL pin will continue to have slope control.

CKP = 0 will force the SCL line low.

CKP = 1 will enable the SCL line to be pulled high (via the external pull-up).

3. Module: Timer1

   When the Timer1 counter uses the external oscillator (T1OSCEN is set), the Timer1 counter may increment faster than expected. This occurs because the OSC2/CLKOUT output signal may be coupled into the T1CKI input, giving additional clock pulses. When the device is in sleep the Timer1 counter increments correctly. This is because the device's oscillator is turned off. If the T1CKI is driven with an external clock (with reasonable drive capability), the OSC2/CLKOUT signal will not be coupled into the T1CKI pin. This will allow the Timer1 counter to increment at the expected frequency.

4. Module: Timer1

   When the Timer1 oscillator circuit is used (enabled and oscillating), the digital input buffers are not disabled. This causes the device to have a greater than expected current consumption in both normal operation and sleep mode.

5. Module: SSP

   When the SSP module is programmed for any I²C mode, but the SSP module is disabled (SSPEN is cleared), unexpected data may be driven from the SCK pin. This occurs when the CKP bit (SSPCON<4>) is cleared, which then drives the value of PORTC<3>.

Work-around:

When disabling the SSP module, ensure that the CKP bit is set or that the SSP module is not in any I²C mode.

6. Module: Parallel Slave Port

   When using the Parallel Slave Port (PSP), the IBF flag may not be set. The IBF flag is not set if a write to the data output latch (PORTD) occurs at the same time as an external system write to the input data latch. However, the PSPIF bit will still be set. If the input buffer is not read before the next external system write, the overflow bit (IBOV) will not be set, and the data will be overwritten.

   Work-arounds

   Interrupt Method:

   If the PSP is the source of the interrupt, then the IBF and OBF bits need to be checked. If either the IBF bit or the OBF bit is set, then the input buffer is full.

```
PSP_INT_SOURCE
  BSF   STATUS, RP0 ; Bank 1
  BTFSC TRISE, IBF  ; Test the IBF bit
  GOTO  READ_IB     ; Read the Input Buffer
  BTFSC TRISE, OBF  ; Test the OBF bit
  GOTO  READ_IB     ; Read the Input Buffer
WRITE_OB   :        ; Write the next value
    :               ; into the Output Buffer
READ_IB    :        ; Read the Input Buffer
```

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

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Polled Method:

After the program writes to the output buffer, the program should check the state of the PSPIF flag. If the PSPIF is set, the IBF is cleared, and the OBF is set, then an external write has occurred (input buffer full).

```
  MOVWF PORTD        ; Load the Output
                     ;   Buffer
  BTFSC PIR, PSPIF   ; Did the PSP
                     ;   Interrupt flag
                     ;   get set?
  GOTO  PSP_EVENT    ; Yes
    :                ; No
    :
PSP_EVENT
  BSF   STATUS, RP0  ; Bank 1
  BTFSC TRISE, IBF   ; Test the IBF bit
  GOTO  READ_IB      ; Read the Input
                     ; Buffer
  BTFSC TRISE, OBF   ; Test the OBF bit
  GOTO  READ_IB      ; Read the Input Buffer
WRITE_OB
    :                ; Write the next value
    :                ;   into the Output
                     ;   Buffer
READ_IB
    :                 ; Read the Input Buffer
```

Note: Regardless of the method used, the IBF cleared and OBF set state will also occur if an external system read occurs immediately followed by a write to the output buffer.

7. Feature: POR

   The internal Power-On Reset pulse may not generate the power-up timer time-out delay. This means that the EPROM could be accessed before the device reaches a valid, operational V_{DD} voltage. The master clear ($\overline{MCLR}$) pin should be held at low level (device in reset), until a valid device V_{DD} operating voltage is reached.

8. Module: Parallel Slave Port

   The IBF flag will be set while the $\overline{CS}$ and $\overline{WR}$ pins are held low. The input date is only valid after the rising edge of the $\overline{WR}$ or $\overline{CS}$ pin. The status of the input buffer should only be checked by monitoring the PSPIF bit.

9. Module: Parallel Slave Port

   The IBF flag is cleared when a `RETURN` instruction is executed. When using the Parallel Slave Port (PSP) it is recommended to avoid the use of the `RETURN` instruction, by using either the `RETLW` or `RETFIE` instruction (note that `RETLW` affects the W register, and `RETFIE` will set the GIE bit).

10. Module: Timer1

    When Timer1 is used with a synchronized external clock input (T1CON<TMR1CS=1> and T1CON<T1SYNC=0>), unexpected operation may occur. The external clock is not guaranteed to be synchronized with internal phase clocks. This may result in missing or additional clocks on Timer1.

11. Module: SSP

    In the SPI Master mode, the use of TMR2 as the clock source will cause the SPI CLK pin to continuously output the clock pulses. These pulses will start once the mode is enabled and can only be disabled by changing the SPI mode or making the CLK pin an input.

12. Module: Timer1

    When using the T1CKI pin as the clock source for Timer 1, care should be taken to ensure that the clock edge is “fast”. In this mode, the input does not have a Schmitt Trigger input. This can cause the timer to increment several times if the clock edge is “slow” (and has some noise). The use of a “fast” clock edge, or an external Schmitt Trigger buffer to the clock edge is recommended. This is not an issue when Timer 1 uses an crystal with the internal oscillator circuit.

13. Feature: POR

    The $\overline{POR}$ bit in the PCON register is not guaranteed to be cleared on a power-up situation. It is recommended that this bit not be used to determine if a power-up had occurred.

14. Module: CCP

    The special event trigger of the Compare mode may not occur if both of the following conditions exist:

    - An instruction one cycle (T_{CY}) prior to a Timer1/ Compare register match has literal data equal to the address of a CCP register being used.*
    - An instruction in the same cycle as a Timer1/ Compare register match has an MSb of ‘0’.

    The interrupt for the compare event will still be generated, but no special event trigger will occur.

    * 15h(CCPR1L), 16h(CCPR1H) or 17h(CCP1CON) for CCP1; 1Bh(CCPR2L), 1Ch(CCPR2H) or 1Dh(CCP2CON) for CCP2.

    Work Around

    Use the interrupt service routine instead of using the special event trigger to reset Timer1 (and start an A/D conversion, if applicable).

15. Module: Timer1

The Timer1 value may unexpectedly increment if either the TMR1H or the TMR1L register is written.

If Timer1 is ON, then turned OFF, performing any write instruction with TMR1H as the destination may cause TMR1L to increment.

Example 1:

```
BSF T1CON, TMR1ON
          :
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:
TMR1H:TMR1L = 3F:00
TMR1 value after MOVF instruction:
TMR1H:TMR1L = 3F:01

Example 2:

```
BSF T1CON, TMR1ON
          :
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:
TMR1H:TMR1L = FF:FF
TMR1 value after MOVF instruction:
TMR1H:TMR1L = FF:00

If Timer1 is ON, then turned OFF when TMR1H:TMR1L = xx:FF, performing any write instruction with TMR1L as the destination may cause TMR1H to increment.

Example 1:

```
BSF T1CON, TMR1ON
          :
BCF T1CON, TMR1ON
CLRF TMR1L
```

TMR1 value before CLRF instruction:
TMR1H:TMR1L = FF:FF
TMR1 value after CLRF instruction:
TMR1H:TMR1L = 00:00
(TMR1IF is **not** set.)

Work Around

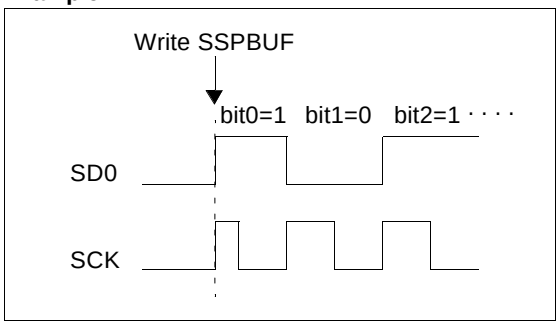
To preserve Timer1 register values:

Read Timer1 register values into “shadow” registers. Perform any write instruction(s) on the shadow registers. Write the shadow register values back into the Timer1 registers.

16. Module: SSP

When the SPI is using Timer2/2 as the clock source, a shorter-than-expected SCK pulse may occur on the first bit of the transmitted/received data.

Example:



Work Around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit, and then turn Timer2 back on.

Example Code:

```
      BSF   STATUS, RP0    ;Bank 1
LOOP  BTFSS SSPSTAT, BF    ;Data received?
                           ;(Xmit complete?)
      GOTO  LOOP           ;No
      BCF   STATUS, RP0    ;Bank 0
      MOVF  SSPBUF, W      ;W = SSPBUF
      MOVWF RXDATA         ;Save in user RAM
      MOVF  TXDATA, W      ;W = TXDATA
      BCF   T2CON, TMR2ON  ;Timer2 off
      CLR   TMR2           ;Clear Timer2
      MOVWF SSPBUF         ;Xmit New data
      BSF   T2CON, TMR2ON  ;Timer2 on
```

Clarifications/Corrections to the Data Sheet:

In the PIC16C6X Preliminary Data Sheet (document DS30234**C**), the following clarifications and corrections should be noted.

NONE

Design Considerations:

The purpose of these recommendations is to forewarn you of issues that you may incur if the device is operated out of specification.

1. In a device brown-out, some peripheral modules may be disabled. After these modules have been disabled only a Power-on Reset will re-enable them ($\overline{MCLR}$ will not).

TABLE 1: DC SPECIFICATION LIMITS THAT VARY FROM DATA SHEET

DC Characteristics		**Operating Temperature -40 °C ≤ TA ≤ 85°C**					
Characteristic	**Sym.**	**Characterized**		**Corp. Std.**		**Units**	**Condition**
		Min.	**Max.**	**Min.**	**Max.**		
ESD Voltage on VDD pin - pin 20 (DIP) - pin 20 (SOIC)	VESD HBM	1500	—	N.A.	N.A.	V	Human Body Model (HBM)