PIC16C62

Errata Sheet of Rev. B PIC16C62 Silicon

The PIC16C62 (Rev. B) parts you have received conform functionally to the upcoming PIC16C6X preliminary data sheet (DS30234**B**), except for the anomalies described below.

All the problems listed here will be addressed in the future revisions of the PIC16C62 silicon.

1. When using the SPI (SSP module), the master mode with clock = OSC/64 does not function correctly (at any voltage).
2. When using the I^2C™ (SSP module), in the master mode, the TRISC<4:3> bits will NOT manipulate the corresponding SCL and SDA pins. Note that in slave mode the device will drive out the proper levels.

Work-around:

For the SDA pin.

To control the level of the SDA pin, connect an additional I/O pin to the SDA pin. Use this additional I/O pin to control the output for the master data (via the TRIS and PORT bits of that pin). Note that since a general purpose I/O pin is now controlling the output data, the SDA will not have slope control.

For the SCL pin.

To control the level of the SCL pin, use the CKP bit (SSPCON<4>). The SCL pin will continue to have slope control.

CKP = 0 will force the SCL line low.

CKP = 1 will enable the SCL line to be pulled high (via the external pull-up).

3. When the Timer1 counter uses the external oscillator (T1OSCEN is set), the Timer1 counter may increment faster than expected. This occurs because the OSC2/CLKOUT output signal may be coupled into the T1CKI input, giving additional clock pulses. When the device is in sleep the Timer1 counter increments correctly. This is because the device's oscillator is turned off. If the T1CKI is driven with an external clock (with reasonable drive capability), the OSC2/CLKOUT signal will not be coupled into the T1CKI pin. This will allow the Timer1 counter to increment at the expected frequency.
4. When the Timer1 oscillator circuit is used (enabled and oscillating), the digital input buffers are not disabled. This causes the device to have a greater than expected current consumption in both normal operation and sleep mode.
5. When the SSP module is programmed for any I^2C mode, but the SSP module is disabled (SSPEN is cleared), unexpected data may be driven from the SCK pin. This occurs when the CKP bit (SSPCON<4>) is cleared, which then drives the value of PORTC<3>.

Work-around:

When disabling the SSP module, ensure that the CKP bit is set or that the SSP module is not in any I^2C mode.

I^2C is a trademark of Philips Corporation.

6. The internal Power-On Reset pulse may not generate the power-up timer, time-out delay. This means that the EPROM could be accessed before the device reaches a valid operational V_{DD} voltage. The master clear ($\overline{MCLR}$) pin should be held at low level (device in reset), until a valid device V_{DD} operating voltage is reached.
7. When Timer1 is used with a synchronized external clock input (T1CON<TMR1CS=1> and T1CON<T1SYNC=0>), unexpected operation may occur. The external clock is not guaranteed to be synchronized with internal phase clocks. This may result in missing or additional clocks on Timer1.
8. In the SPI Master mode, the use of TMR2 as the clock source will cause the SPI CLK pin to continuously output the clock pulses. These pulses will start once the mode is enabled and can only be disabled by changing the SPI mode or making the CLK pin an input.
9. When using the T1CKI pin as the clock source for Timer 1, care should be taken to ensure that the clock edge is “fast”. In this mode, the input does not have a Schmitt Trigger input. This can cause the timer to increment several times if the clock edge is “slow” (and has some noise). The use of a “fast” clock edge, or an external Schmitt Trigger buffer to the clock edge is recommended. This is not an issue when Timer 1 uses an crystal with the internal oscillator circuit.
10. The $\overline{POR}$ bit in the PCON register is not guaranteed to be cleared on a power-up situation. It is recommended that this bit not be used to determine if a power-up had occurred.

Clarifications/Corrections to the Data Sheet:

In the PIC16C6X Preliminary Data Sheet (document DS30234**B**), the following clarifications and corrections should be noted.

1. The AC specifications are not yet implemented in the device test program. Characterization has shown a specification that may vary from the data sheet specification. This specification is shown in Table 1.
2. If peripherals on PORTC are operating, then read-modify-write instructions should not be used on the TRISC register. This could lead to an unexpected change of data direction on some PORTC pins. This is because the peripherals may temporarily override the data direction of the pin, and it may be this value that is read. Use of a TRISC shadow register is recommended, where all operations are applied to the shadow register. This shadow register then can be written to TRISC at any time.
3. In the PIC16C62 Product Brief (DS30414A), the pin-out of the SSOP package is wrong. The correct pin-out is shown in Figure 0-1.

FIGURE 0-1: NEW SSOP PIN-OUT

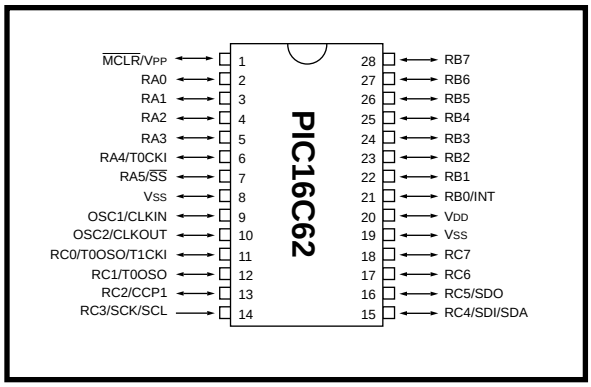

TABLE 1: AC SPECIFICATION LIMITS THAT VARY FROM DATA SHEET

Parameter No.	Sym.	Characteristic		Char. Data		Data Sheet		Units	Condition
				Min.	Max.	Min.	Max.		
73	TdiV2scH TdiV2scL	Setup time of SDI data input to SCK edge		Tosc	-	Tcy	-		
74	TscH2diI TscL2diI	Hold time of SDI data input to SCK edge		Tosc	-	0.5 Tcy	-		
106	THD:DAT	Data Input Hold Time	100 kHz mode	20	-	0	-	ns	Automotive Temperature range
			400 kHz mode	0.02	0.9	0	0.9	us	

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

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