



PIC16C61

Errata Sheet for Rev. B PIC16C61 Silicon

The PIC16C61 (Rev. B) parts you have received conform functionally to the PIC16C6x preliminary data sheet (DS30234A), except for the anomalies described below.

All the problems listed here will be addressed in the future revisions of the PIC16C61 silicon.

1. The internal Power-On Reset pulse may not generate the power-up timer, time-out delay. This means that the EPROM could be accessed before the device reaches a valid operational V_{DD} voltage. The master clear ($\overline{\text{MCLR}}$) pin should be held at low level (device in reset), until a valid device V_{DD} operating voltage is reached.

Clarifications / Corrections to the Data Sheet:

None

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