PIC17C44

PIC17C44 Rev. A Silicon Errata Sheet

The PIC17C44 (Rev. A) parts you have received conform functionally to the PIC17C4X preliminary data sheet (DS30412**C**), except for the following clarifications and corrections.

NONE

Clarifications/Corrections to the Data Sheet:

The PIC17C44 Preliminary Data Sheet (document DS30412**C**) that you have received, requires the following clarifications and corrections.

1. The clearing of any interrupt enable bit(s) in the INTSTA register should be preceded by the disabling of the global interrupt control bit (setting GLINTD). Global interrupts may then be re-enabled. The individual interrupts may be re-enabled without further control of the GLINTD bit.

   When global interrupts are enabled, if the interrupt flag is being set when the corresponding enable bit is being cleared the device will branch to the reset vector address (0h). The interrupt flag will not be (automatically) cleared.

2. The RETURN instruction causes an update of the PCLATH register. The PCLATH register is loaded with the high address of the RETURN instruction.

3. The Table write to internal program memory (self programming) can occur even when the $\overline{MCLR}$ pin is either at the V_{IH} or V_{IHH} voltage level. When the $\overline{MCLR}$ pin is at V_{IH}, the table write sequence occurs, but the programming voltage is marginal since the $\overline{MCLR}$ pin is not at the correct level. This table write may cause the specified program memory location to be corrupted (depending on the data in the TABLAT register).

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

4. Unexpected results may occur if a table write (TABLWT instruction) to external memory occurs after a table read (TABLRD instruction).

   To ensure that the proper 16-bit value is written, a table write (TLWT) intruction(s) needs to be followed by the TABLWT instruction. If not the value that is written will not be as expected. The value will contain the values that were last written to the TABLATH and TABLATL registers and will not contain the values that had been read from the external memory into the TABLATH:TABLATL registers by the TABLRD instruction.

   Example:

```
                        TABLAT   Ext Bus
TLWT    LO, fn1          x:fn1    -:-
TABLWT  HI, 1, fn2    fn2:fn1  fn2:fn1
:
TABLRD  HI, 0, fn3     X1:X0    X1:X0
TLRD    LO, fn4        X1:X0     -:-
:
TABLWT  HI, 1, fn5    fn5:X0   fn5:fn1
```

5. The Power-down current of the PIC17**C**44 has been increased as shown in Table 1. The specification of 5 µA remains for the PIC17**LC**44 devices.

TABLE 1: DC SPECIFICATION LIMITS THAT VARY FROM DATA SHEET

Param No.	Sym.	Characteristic	Tested			Data Sheet			Units	Condition
			Min	Typ	Max	Min	Typ	Max		
D021	IPD	Power-down Current	—	< 1	10	—	< 1	5	µA	PIC17**C**44
			—	< 1	5	—	< 1	5	µA	PIC17**LC**44

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