Section 35. Glossary

A

A/D

See Analog to Digital.

Acquisition Time (TACQ)

This is related to Analog to Digital (A/D) converters. This is the time that the A/D's holding capacitor acquires the analog input voltage level connected to it. When the GO bit is set, the analog input is disconnected from the holding capacitor and the A/D conversion is started.

ALU

Arithmetical Logical Unit. Device logic that is responsible for the mathematical (add, subtract, ...), logical (and, or, ...), and shifting operations.

Analog to Digital (A/D)

The conversion of an analog input voltage to a ratiometric digital equivalent value.

Assembly Language

A symbolic language that describes the binary machine code in a readable form.

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B

Bank

This is a method of addressing Data Memory. Since midrange devices have 7-bits for direct addressing, instructions can address up to 128 bytes (including special function registers). To allow more data memory to be present on a device, data memory is partitioned into contiguous banks of 128 bytes each. To select the desired bank, the bank selection bits (RP1:RP0) need to be appropriately configured. Since there are presently 2 bank selection bits, 4 banks can be implemented.

Baud

Generally how the communication speed of serial ports is described. Equivalent to bits per second (bps).

BCD

See Binary Coded Decimal.

Binary Coded Decimal (BCD)

Each 4-bit nibble expresses a digit from 0-9. Usually two digits are packed to a byte giving a range of 0 - 99.

BOR

See Brown-out Reset.

Brown-out

A condition where the supply voltage of the device temporarily falls below the specified minimum operation point. This can occur when a load is switched on and causes the system/device voltage to drop.

Brown-out Reset (BOR)

Circuitry which will force the device to the reset state if the (device) voltage falls below a specified voltage level. Some devices have an internal BOR circuit, while other devices would require an external circuit to be created.

Bus width

This is the number of bits of information that the bus carries. For the Data Memory, the bus width is 8-bits. For the midrange devices the Program Memory bus width is 14-bits.

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C

Capture

A function of the CCP module in which the value of a timer/counter is “captured”, into a holding register, when a predetermined event occurs.

CCP

Capture, Compare, Pulse Width Modulation (PWM). This module can be configured to operate as an input capture, or a timer compare, or a PWM output.

Common RAM

This is a region of the data memory RAM that is the same RAM location across all banks. This common RAM maybe implemented between addresses 70h -7Fh (inclusive). This common area is useful for the saving of required variables during context switching (such as during an interrupt).

Compare

A function of the CCP module in which the device will perform an action when a timer’s register value matches the value in the compare register.

Compare Register

A 16-bit register that contains a value that is compared to the 16-bit TMR1 register. The compare function triggers when the counter matches the contents of the compare register.

Capture Register

A 16-bit register that gets loaded with the value of the 16-bit TMR1 register when a capture event occurs.

Configuration Word

This is a location that specifies the characteristics that the device will have for operation (such as oscillator mode, WDT enable, start-up timer enables). These characteristics can be specified at time of device programming. For EPROM memory devices, as long as the bit is a '1', it may at a later time be programmed as a '0'. The device must be erased for a '0' to be returned to a '1'.

Conversion Time (Tconv)

This is related to Analog to Digital (A/D) converters. This is the time that the A/D converter requires to convert the analog voltage level on the holding capacitor to a digital value.

CPU

Central Processing Unit. Decodes the instructions, and determines the operands that are needed and the operations that need to be done. Arithmetic, logical, or shift operations will be passed to the ALU.

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D

D/A

See Digital to analog

DAC

Digital to analog converter

Data Bus

The bus which is used to transfer data to and from the data memory.

Data EEPROM

Data Electrically Erasable Programmable Read Only Memory. This memory has the capability to be programmed and re-programmed by the CPU to ensure that in the case of a power loss critical values/variables are retained in the non-volatile memory.

Data Memory

The memory that is on the Data Bus. This memory is volatile (SRAM) and contains both the Special Function Registers and General Purpose Registers.

Direct Addressing

When the Data Memory Address is contained in the Instruction. The execution of this type of instruction will always access the data at the embedded address.

Digital to Analog

E

EEPROM

Electrically Erasable Programmable Read Only Memory. This memory has the capability to be programmed and erased in-circuit.

EPROM

Electrically Programmable Read Only Memory. This memory has the capability to be programmed in-circuit. Erasing requires that the program memory be exposed to UV light.

EXTRC

External Resistor-Capacitor (RC). Some devices have a device oscillator option that allows the clock to come from an external RC. This is the same as RC mode on some devices.

F

Flash Memory

This memory has the capability to be programmed and erased in-circuit. Program Memory technology that is almost functionally equivalent to Program EEPROM Memory.

Fosc

Frequency of the device oscillator.

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G

GIO

General Input/Output

GPIO

General Purpose Input/Output

GPR

General Purpose Register (RAM). A portion of the data memory that can be used to store the program's dynamic variables.

H

Harvard Architecture

In this architecture the Program Memory and Data Memory buses are separated. This allows concurrent accesses to Data Memory and Program Memory, which increases the performance of the device.

Holding Capacitor

This is a capacitor in the Analog to Digital (A/D) module which "holds" to analog input level once the conversion is started. During acquisition, the holding capacitor is charged/discharged by the voltage level on the analog input pin. Once the conversion is started, the holding capacitor is disconnected from the analog input and "holds" this voltage for the A/D conversion.

HS

High Speed. One of the device oscillator modes. The oscillator circuit is tuned to support the high frequency operation. Used for operation from 4 MHz to 20 MHz.

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I

I^2C

Inter-Integrated Circuit. This is a two wire communication interface. This feature is one of the modes of the SSP module.

Indirect Addressing

When the Data Memory Address is not contained in the Instruction. The instruction operates on the INDF address, which causes the Data Memory Address to be the value in the FSR register. The execution of the instruction will always access the data at the address pointed to by the FSR register.

Instruction Bus

The bus which is used to transfer instruction words from the program memory to the CPU.

Instruction Fetch

Due to the Harvard architecture, when one instruction is to be executed, the next location in program memory is “fetched” and ready to be decoded as soon as the currently executing instruction is completed.

Instruction cycle

The events for an instruction to execute. There are four events which can generally be described as: Decode, Read, Execute, and Write. Not all events will be done by all instructions. To see the operations during the instruction cycle, please look in the description of each instruction. Four external clocks (Tosc) make one instruction cycle (TCY).

Interrupt

A signal to the CPU that causes the program flow to be forced to the Interrupt Vector Address (04h in program memory). Before the program flow is changed, the contents of the Program Counter (PC) are forced onto the hardware stack, so that program execution may return to the interrupted point.

INTRC

Internal Resistor-Capacitor (RC). Some devices have a device oscillator option that allows the clock to come from an internal RC.

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L

LCD

Liquid Crystal Display. Useful for giving visual status of a system. This may require the specification of custom LCD glass.

LED

Light Emitting Diode. Useful for giving visual status of a system.

Literal

This is a constant value that is embedded in an instruction word.

Long Word Instruction

An instruction word that embeds all the required information (opcode and data) into a single word. This ensures that every instruction is accessed and executed in a single instruction cycle.

LP

One of the device oscillator modes. Used for low frequency operation which allows the oscillator to be tuned for low power consumption. Operation is up to 200 kHz.

LSb

Least Significant Bit.

LSB

Least Significant Byte.

M

Machine cycle

This is a concept where the device clock is divided down to a unit time. For PICmicros this unit time is 4 times the device oscillator (4TOSC), also known as TCY.

MSb

Most Significant Bit.

MSB

Most Significant Byte.

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N

Non-Return to Zero

Two level encoding used to transmit data over a communications medium. A bit value of '1' indicates a high voltage signal. A bit value of '0' indicates a low voltage signal. The data line defaults to a high level.

NRZ

See Non-Return to Zero

O

Opcode

The portion of the 14-bit instruction word that specifies the operation that needs to occur. The opcode is of variable length depending on the instruction that needs to be executed. The opcode varies from 4-bits to x-bits. The remainder of the instruction word contains program or data memory information.

Oscillator Start-up Timer (OST)

This timer counts 1024 crystal/resonator oscillator clock before releasing the internal reset signal.

OST

See Oscillator Start-up Timer.

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P

Pages

Method of addressing the Program Memory. Midrange devices have 11-bit addressing for CALL and GOTO instructions, which gives these instructions a 2-Kword reach. To allow more program memory to be present on a device, program memory is partitioned into contiguous pages, where each page is 2-Kwords. To select the desired page, the page selection bits (PCLATCH<5:4>) need to be appropriately configured. Since there are presently 2 page selection bits, 4 pages can be implemented.

Parallel Slave Port (PSP)

A parallel communication port which is used to interface to a microprocessor's 8-bit data bus.

POP

A termed used to refer to the action of restoring information from a stack (software and/or hardware). See PUSH.

Postscaler

A circuit that slows the rate of the interrupt generation (or WDT reset) from a counter/timer by dividing it down.

Power-on Reset POR)

Circuitry which determines if the device voltage rose from a powered down level (0V). If the device voltage is rising from ground, a device reset occurs and the PWRT is started.

Power-up Timer (PWRT)

A timer which holds the internal reset signal low for a timed delay to allow the device voltage to reach the valid operating voltage range. Once the timer times out, the OST circuitry is enabled (for all crystal/resonator device oscillator modes).

Prescaler

A circuit that slows the rate of a clocking source to a counter/timer.

Program Bus

The bus which is used to transfer instruction words form the program memory to the CPU.

Program Counter

A register which specifies the address in program memory that is the next instruction to execute.

Program Memory

Any memory that is one the program memory bus. Static variables may be contained in program memory (such as tables).

PSP

See Parallel Slave Port.

Pulse Width Modulation (PWM)

A serial signal in which the information is contained in the width of a (high) pulse of a constant frequency signal. A PWM output, from the CCP module, of the same duty cycle requires no software overhead.

PUSH

A termed used to refer to the action of saving information onto a stack (software and/or hardware). See POP.

PWM

Pulse Width Modulation.

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Q

Q-cycles

This is the same as a device oscillator cycle. There are 4 Q-cycles for each instruction cycle.

R

RC

Resistor-Capacitor. The default configuration for the device oscillator. This allows a "**R**eal-**C**heap" implementation for the device clock source. This clock source does not supply an accurate time-base. Operation to 4 MHz is supported. (See EXTRC).

Read-Modify-Write

This is where a register is read, then modified, and then written back to the original register. This may be done in one instruction cycle or multiple instruction cycles.

Register File

This is the Data Memory. Contains the SFRs and GPRs.

ROM

Read Only Memory. Memory that is fixed and cannot be modified.

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S

Sampling Time

Sampling time is the complete time to get an A/D result. It includes the acquisition time and the conversion time.

Serial Peripheral Interface (SPI)

This is one of the modes of the SSP module. This is typically a 3-wire interface, with a data out line, a data in line, and a clock line. Since the clock is present, this is a synchronous interface.

SFR

Special Function Register. These registers contain the control bits and status information for the device.

Single cycle instruction

An instruction that executes in a “single” machine cycle (TCY).

Sleep

This is the low power mode of the device, where the device’s oscillator is disabled.This reduces the current the device consumes. Certain peripherals may be placed into modes where they continue to operate.

Special Function Registers (SFR)

These registers contain the control bits and status information for the device.

SPI

See Serial Peripheral Interface.

Stack

A portion of the CPU which retains the return address for program execution. The stack gets loaded with the value in the Program Counter when a CALL instruction is executed or an interrupt occurs.

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T

TAD

In the A/D Converter, the time for a single bit of the analog voltage to be converted to a digital value.

TCY

The time for an instruction to complete. This time is equal to Fosc/4 and is divided into four Q-cycles.

Tosc

The time for the device oscillator to do a single period.

U

USART

Universal Synchronous Asynchronous Receiver Transmitter. This module can either operate as a full duplex asynchronous communications port, or a half duplex synchronous communications port. When operating in the asynchronous mode, this can be interfaced to a PC's serial port.

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V

Voltage Reference (VREF)

A voltage level that can be used as a reference point for A/D conversions (AVDD and AVSS) or the trip point for comparators.

von Neumann Architecture

In this architecture the Program Memory and Data Memory are contained in the same area. This means that accesses to the program memory and data memory must occur sequentially, which affects the performance of the device.

W

W Register

See Working Register.

Watchdog Timer (WDT)

Used to increase the robustness of a design by recovering from software flows that were not expected in the design of the product or other system related issues. The Watchdog Timer causes a reset if it is not cleared prior to overflow. The clock source for a PICmicro is an on-chip RC oscillator which enhances system reliability.

WDT

Watchdog Timer.

Working Register (W)

Can also be thought of as the accumulator of the device. Also used as an operand in conjunction with the ALU during two operand instructions.

X

XT

One of the device oscillator modes. Used for operation from 100 kHz to 4 MHz.

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35.1 Revision History

Revision A

This is the initial released revision of the Glossary.

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