Section 34. Appendix

HIGHLIGHTS

This section of the manual contains the following major topics:

I²C is a trademark of Philips Corporation.

APPENDIX A: I²C™ OVERVIEW

This section provides an overview of the Inter-Integrated Circuit (I²C™) bus, with Subsection **A.2 "Addressing I²C Devices"** discussing the operation of the SSP modules in I²C mode.

The I²C bus is a two-wire serial interface. The original specification, or standard mode, is for data transfers of up to 100 Kbps. An enhanced specification, or fast mode (400 Kbps) is supported. Standard and Fast mode devices will operate when attached to the same bus, if the bus operates at the speed of the slower device.

The I²C interface employs a comprehensive protocol to ensure reliable transmission and reception of data. When transmitting data, one device is the "master" which initiates transfer on the bus and generates the clock signals to permit that transfer, while the other device(s) acts as the "slave." All portions of the slave protocol are implemented in the SSP module's hardware, except general call support, while portions of the master protocol need to be addressed in the PIC16CXX software. The MSSP module supports the full implementation of the I²C master protocol, the general call address, and data transfers upto 1 Mbps. The 1 Mbps data transfers are supported by some of Microchips Serial EEPROMs. Table A-1 defines some of the I²C bus terminology.

In the I²C interface protocol each device has an address. When a master wishes to initiate a data transfer, it first transmits the address of the device that it wishes to "talk" to. All devices "listen" to see if this is their address. Within this address, a bit specifies if the master wishes to read-from/write-to the slave device. The master and slave are always in opposite modes (transmitter/receiver) of operation during a data transfer. That is they can be thought of as operating in either of these two relations:

- Master-transmitter and Slave-receiver
- Slave-transmitter and Master-receiver

In both cases the master generates the clock signal.

The output stages of the clock (SCL) and data (SDA) lines must have an open-drain or open-collector in order to perform the wired-AND function of the bus. External pull-up resistors are used to ensure a high level when no device is pulling the line down. The number of devices that may be attached to the I²C bus is limited only by the maximum bus loading specification of 400 pF and addressing capability.

A.1 Initiating and Terminating Data Transfer

During times of no data transfer (idle time), both the clock line (SCL) and the data line (SDA) are pulled high through the external pull-up resistors. The START and STOP conditions determine the start and stop of data transmission. The START condition is defined as a high to low transition of the SDA when the SCL is high. The STOP condition is defined as a low to high transition of the SDA when the SCL is high. Figure A-1 shows the START and STOP conditions. The master generates these conditions for starting and terminating data transfer. Due to the definition of the START and STOP conditions, when data is being transmitted, the SDA line can only change state when the SCL line is low.

Figure A-1: Start and Stop Conditions

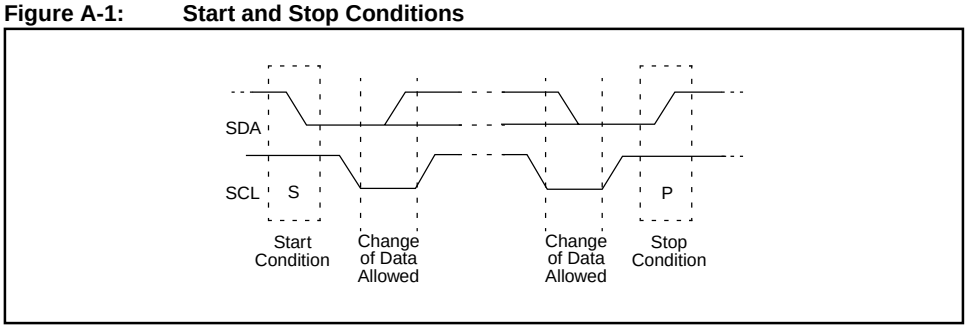


Table A-1: I^2C Bus Terminology

Term	Description
Transmitter	The device that sends the data to the bus.
Receiver	The device that receives the data from the bus.
Master	The device which initiates the transfer, generates the clock and terminates the transfer.
Slave	The device addressed by a master.
Multi-master	More than one master device in a system. These masters can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure that ensures that only one of the master devices will control the bus. This ensure that the transfer data does not get corrupted.
Synchronization	Procedure where the clock signals of two or more devices are synchronized.

A.2 Addressing I²C Devices

There are two address formats. The simplest is the 7-bit address format with a R/$\overline{W}$ bit (Figure A-2). The more complex is the 10-bit address with a R/$\overline{W}$ bit (Figure A-3). For 10-bit address format, two bytes must be transmitted. The first five bits specify this to be a 10-bit address format. The 1st transmitted byte has 5-bits which specify a 10-bit address, the two MSbs of the address, and the R/$\overline{W}$ bit. The second byte is the remaining 8-bits of the address.

Figure A-2: 7-bit Address Format

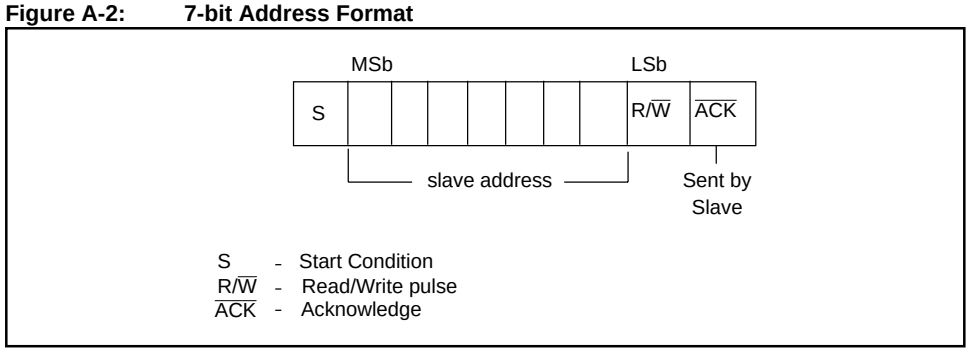
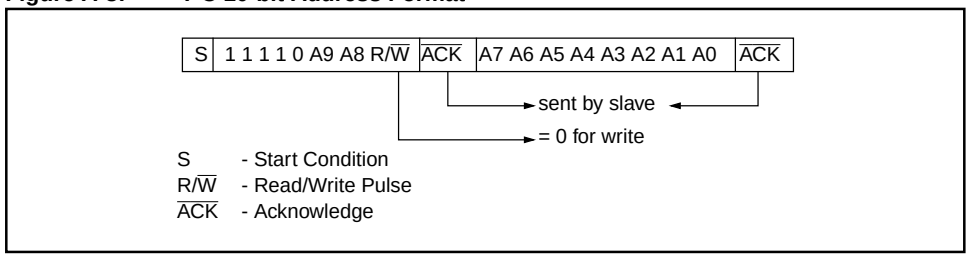


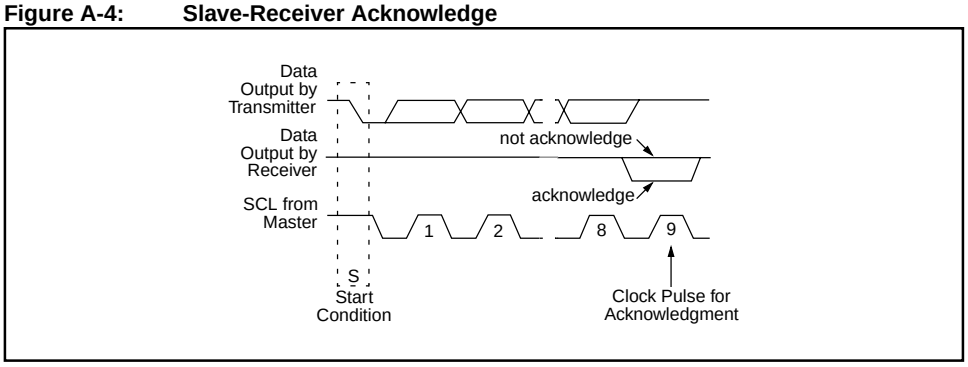
Figure A-3: I²C 10-bit Address Format



A.3 Transfer Acknowledge

All data must be transmitted per byte, with no limit to the number of bytes transmitted per data transfer. After each byte, the slave-receiver generates an acknowledge bit ($\overline{ACK}$) (Figure A-4). When a slave-receiver doesn't acknowledge the slave address or received data, the master must abort the transfer. The slave must leave SDA high so that the master can generate the STOP condition (Figure A-1).

Figure A-4: Slave-Receiver Acknowledge



If the master is receiving the data (master-receiver), it generates an acknowledge signal for each received byte of data, except for the last byte. To signal the end of data to the slave-transmitter, the master does not generate an acknowledge (not acknowledge). The slave then releases the SDA line so the master can generate the STOP condition. The master can also generate the STOP condition during the acknowledge pulse for valid termination of data transfer.

If the slave needs to delay the transmission of the next byte, holding the SCL line low will force the master into a wait state. Data transfer continues when the slave releases the SCL line. This allows the slave to move the received data or fetch the data it needs to transfer before allowing the clock to start. This wait state technique can also be implemented at the bit level, Figure A-5.

Figure A-5: Data Transfer Wait State

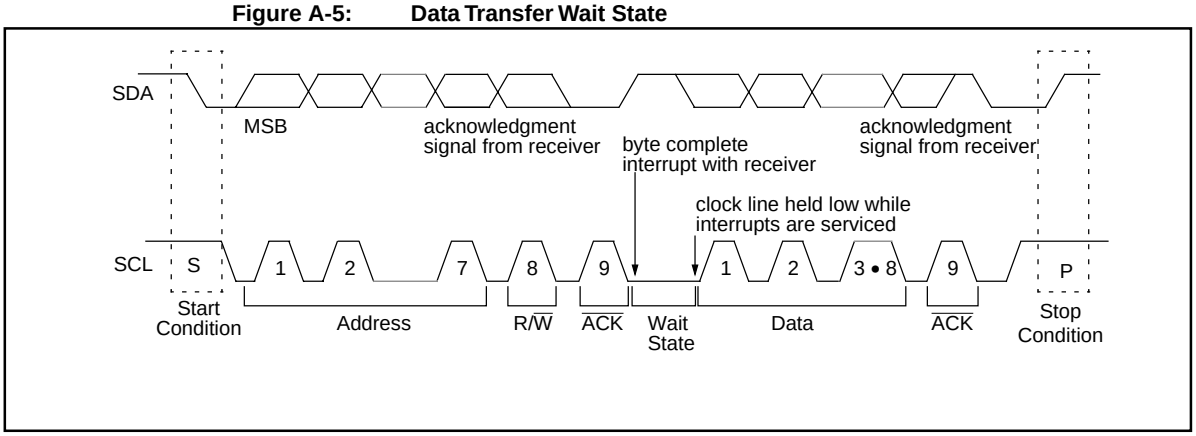


Figure A-6 and Figure A-7 show Master-transmitter and Master-receiver data transfer sequences.

Figure A-6: Master-Transmitter Sequence

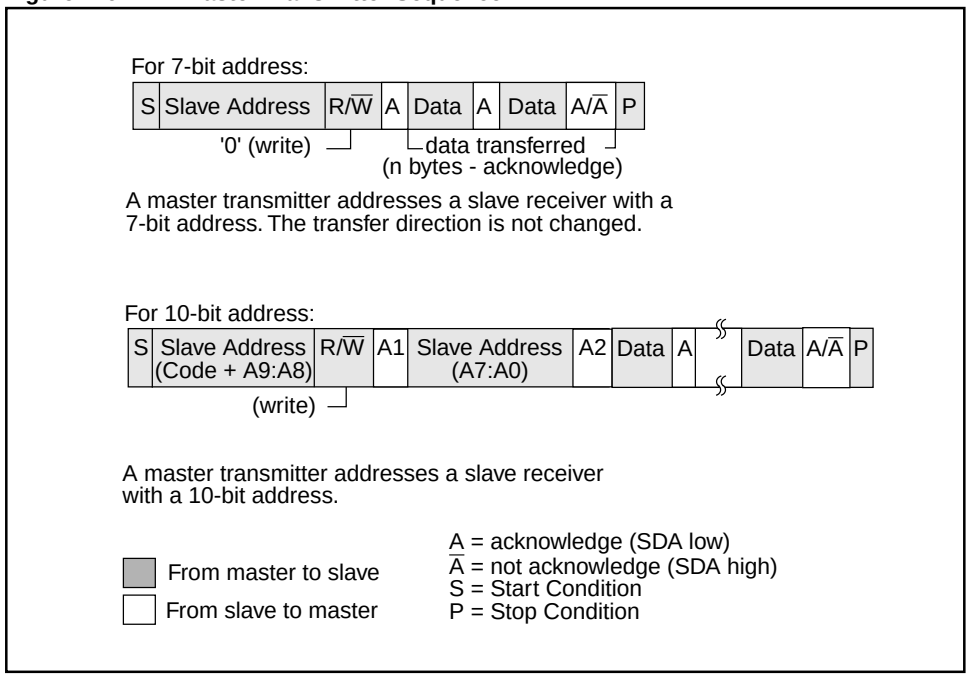
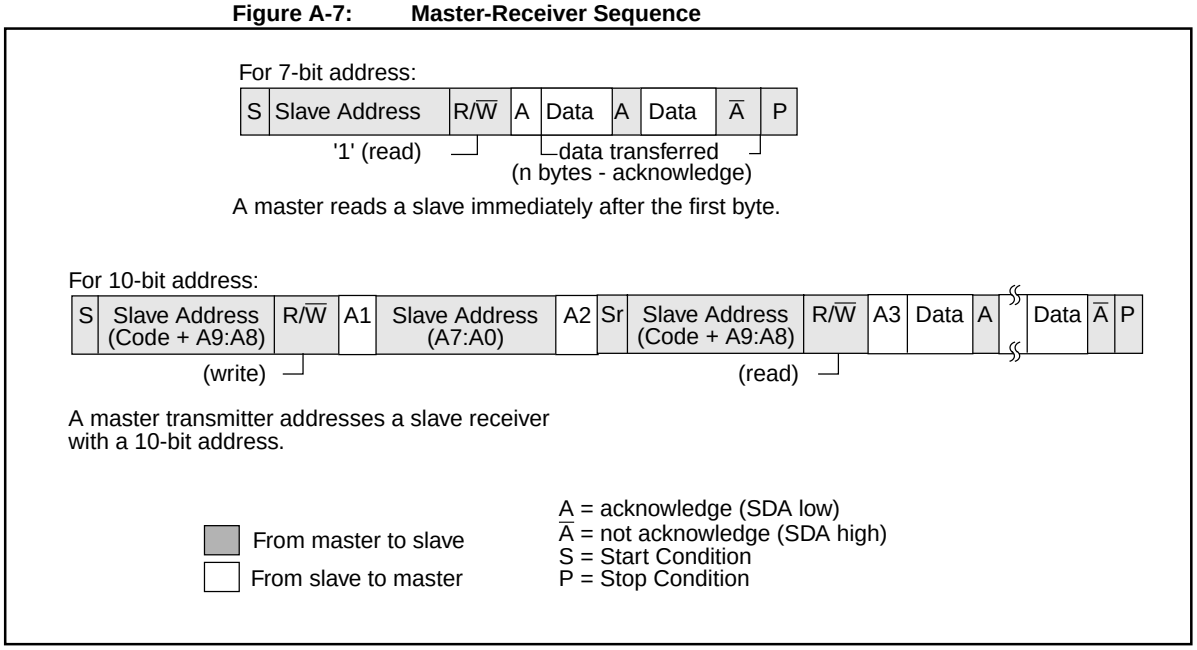
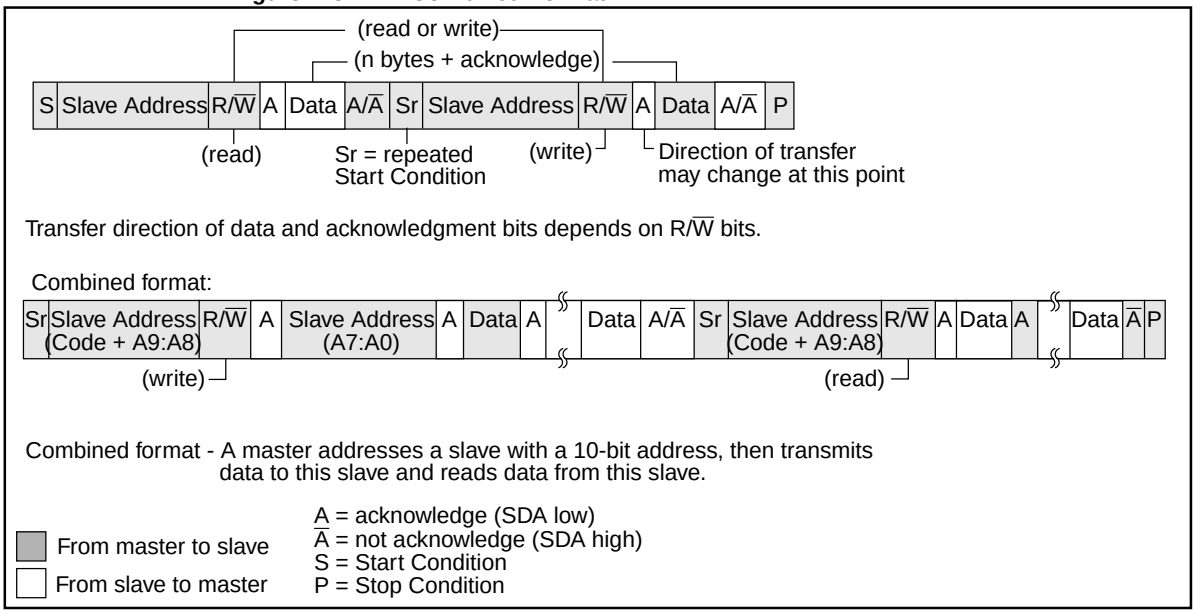


Figure A-7: Master-Receiver Sequence



When a master does not wish to relinquish the bus (which occurs by generating a STOP condition), a repeated START condition (Sr) must be generated. This condition is identical to the start condition (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send “commands” to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure A-8.

Figure A-8: Combined Format



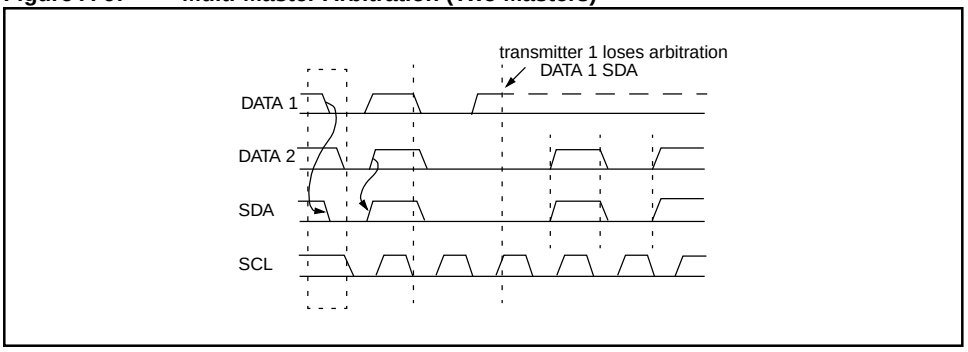
A.4 Multi-master

The I^2C protocol allows a system to have more than one master. This is called multi-master. When two or more masters try to transfer data at the same time, arbitration and synchronization occur.

A.4.1 Arbitration

Arbitration takes place on the SDA line, while the SCL line is high. The master which transmits a high when the other master transmits a low loses arbitration (Figure A-9), and turns off its data output stage. A master which lost arbitration can generate clock pulses until the end of the data byte where it lost arbitration. When the master devices are addressing the same device, arbitration continues into the data.

Figure A-9: Multi-Master Arbitration (Two Masters)



Masters that also incorporate the slave function, and have lost arbitration must immediately switch over to slave-receiver mode. This is because the winning master-transmitter may be addressing it.

Arbitration is not allowed between:

- A repeated START condition
- A STOP condition and a data bit
- A repeated START condition and a STOP condition

Care needs to be taken to ensure that these conditions do not occur.

A.4.2 Clock Synchronization

Clock synchronization occurs after the devices have started arbitration. This is performed using a wired-AND connection to the SCL line. A high to low transition on the SCL line causes the concerned devices to start counting off their low period. Once a device clock has gone low, it will hold the SCL line low until its SCL high state is reached. The low to high transition of this clock may not change the state of the SCL line, if another device clock is still within its low period. The SCL line is held low by the device with the longest low period. Devices with shorter low periods enter a high wait-state, until the SCL line comes high. When the SCL line comes high, all devices start counting off their high periods. The first device to complete its high period will pull the SCL line low. The SCL line high time is determined by the device with the shortest high period, Figure A-10.

Figure A-10: Clock Synchronization

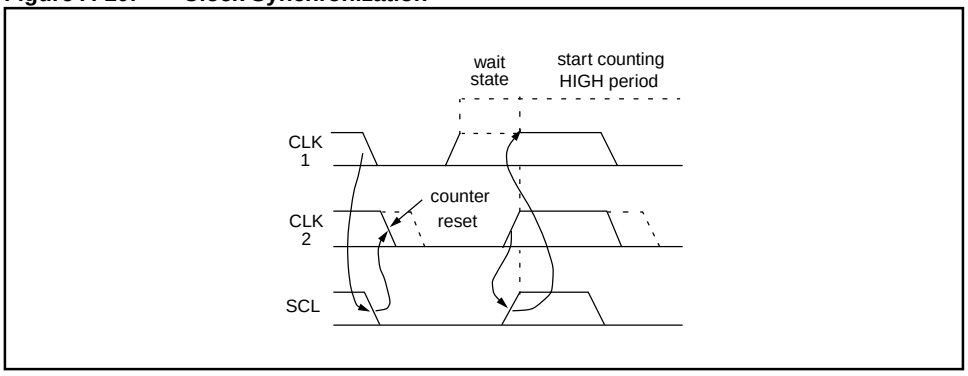


Figure A-11: I^2C Bus Start/Stop Bits Timing Specification

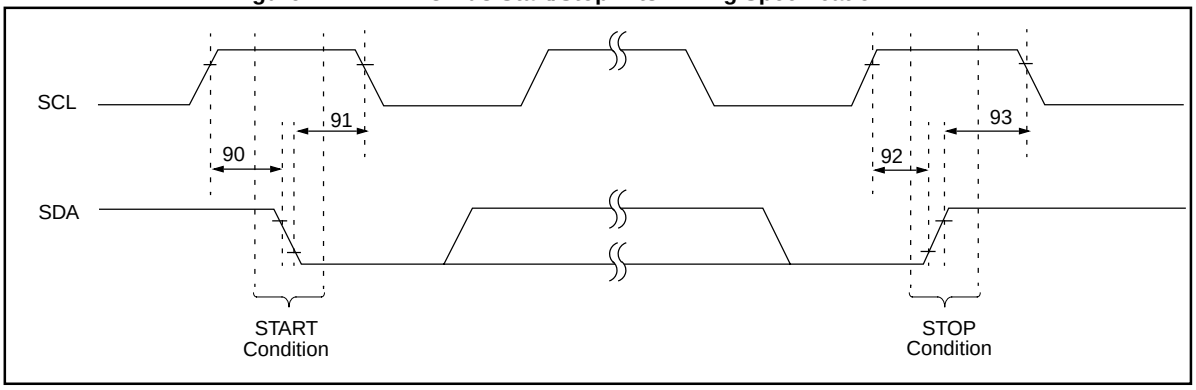


Table A-2: I^2C Bus Start/Stop Bits Timing Specification

Microchip Parameter No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

Figure A-12: I²C Bus Data Timing Specification

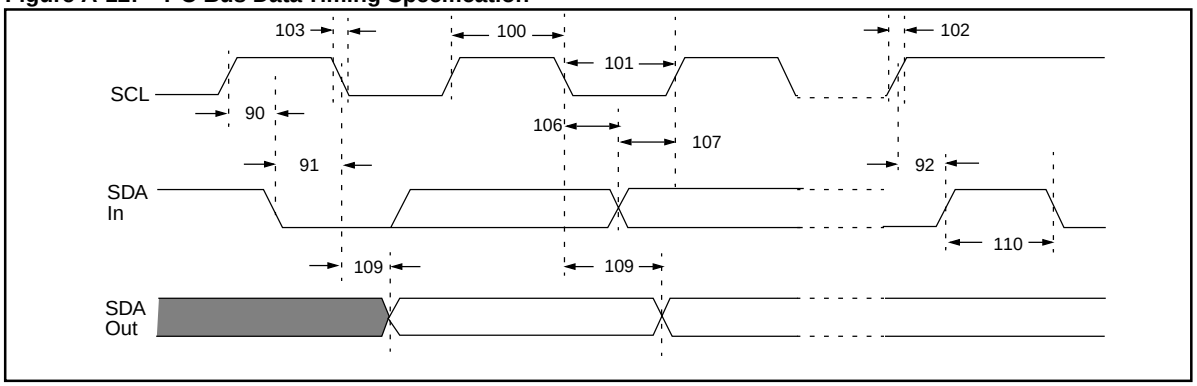


Table A-3: I²C Bus Data Timing Specification

Microchip Parameter No.	Sym	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	
			400 kHz mode	0.6	—	µs	
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	1000	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
D102	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

APPENDIX B: LIST OF LCD GLASS MANUFACTURERS

AEG-MIS
3340 Peachtree Rd. NE Suite 500
Atlanta, GA 30326
TEL: 404-239-0277
FAX: 404-239-0383

All Shore INDS Inc.
1 Edgewater Plaza
Staten Island, NY 10305
TEL: 718-720-0018
FAX: 718-720-0225

Crystaloid
5282 Hudson Drive
Hudson, OH 44236-3769
TEL: 216-655-2429
FAX: 216-655-2176

DCI Inc.
14812 W. 117th St.
Olathe, KS 66062-9304
TEL: 913-782-5672
FAX: 913-782-5766

Excel Technology International Corporation
Unit 5, Bldg. 4, Stryker Lane
Belle Mead, NJ 08502
TEL: 908-874-4747
FAX: 908-874-3278

F-P Electronics/Mark IV Industries
6030 Ambler Drive
Mississauga, ON Canada L4W 2PI
TEL: 905-624-3020
FAX: 905-238-3141

Hunter Components
24800 Chagrin Blvd, Suite 101
Cleveland, OH 44122
TEL: 216-831-1464
FAX: 216-831-1463

Interstate Electronics Corp.
1001 E. Bull Rd.
Anaheim, CA 92805
TEL: 800-854-6979
FAX: 714-758-4111

Kent Display Systems
343 Portage Blvd.
Kent, OH 44240
TEL: 330-673-8784

LCD Planar Optics Corporation
2100-2 Artic Ave.
Bohemia, NY 11716
TEL: 516-567-4100
FAX: 516-567-8516

LXD Inc.
7650 First Place
Oakwood Village, OH 44146
TEL: 216-786-8700
FAX: 216-786-8711

Nippon Sheet Glass
Tomen America Inc.
1285 Avenue of the Americas
New York, NY 10019
TEL: 212-397-4600
FAX: 212-397-3351

OPTREX America
44160 Plymouth Oaks Blvd.
Plymouth, MI 48170
TEL: 313-416-8500
FAX: 313-416-8520

Phillips Components
LCD Business Unit
1273 Lyons Road, Bldg G
Dayton, OH 45459
TEL: 573-436-9500
FAX: 573-436-2230

Satori Electric
23717 Hawthorne Blvd. 3rd Floor
Torrance, CA 90505
TEL: 310-214-1791
FAX: 310-214-1721

Seiko Instruments USA Inc.
Electronic Components Division
2990 West Lomita Blvd.
Torrance, CA 90505
TEL: 213-517-7770
213-517-8113
FAX: 213-517-7792

Standish International
European Technical Center
Am Baümstuck II
65520 Bad Camberg/Erbach
Germany
TEL: 011 49 6434 3324
FAX: 011 49 6434 377238

Standish LCD
W7514 Highway V
Lake Mills, WI 53551
TEL: 414-648-1000
FAX: 414-648-1001

Truly Semiconductors Ltd. (USA)
2620 Concord Ave.
Suite 106
Alhambra, CA 91803
TEL: 818-284-3033
FAX: 818-284-6026

Truly Semiconductor Ltd.
2/F, Chung Shun Knitting Center
1-3 Wing Yip Street,
Kwai Chung, N.T., Hong Kong
TEL: 852 2487 9803
FAX: 852 2480 0126

Varitronix Limited Inc.
3250 Wilshire Blvd. Suite 1901
Los Angeles, CA 90010
TEL: 213-738-8700
FAX: 213-738-5340

Varitronix Limited Inc.
4/F, Liven House
61-63 King Yip Street
Kwun Tong, Kowloon
Hong Kong
TEL: 852 2389 4317
FAX: 852 2343 9555

Varitronix (France) S.A.R.L.
13/15 Chemin De Chilly
91160 Champlain
France
TEL:(33) 1 69 09 7070
FAX:(33) 1 69 09 0535

Varitronix Italia, S.R.L.
Via Bruno Buozzi 90
20099 Sesto San Giovanni
Milano, Italy
TEL:(39) 2 2622 2744
FAX:(39) 2 2622 2745

Varitronix (UK) Limited
Display House, 3 Milbanke Court
Milbanke Way, Bracknell
Berkshire RG12 1BR
United Kingdom
TEL:(44) 1344 30377
FAX(44) 1344 300099

Varitronix (Canada) Limited
18 Crown Steel Drive, Suite 101
Markham, Ontario
Canada L3R 9X8
TEL:(905) 415-0023
FAX:(905) 415-0094

Vikay America Inc.
195 W. Main St.
Avon, CT 06001-3685
TEL: 860-678-7600
FAX: 860-678-7625

APPENDIX C: DEVICE ENHANCEMENT

As the Midrange architecture matured, certain modules and features have been enhanced. They are:

1. The data memory map
2. The SSP module
3. The A/D module
4. Brown-out Reset added to the core
5. $\overline{\text{MCLR}}$ Filter
6. USART
7. Device Oscillator

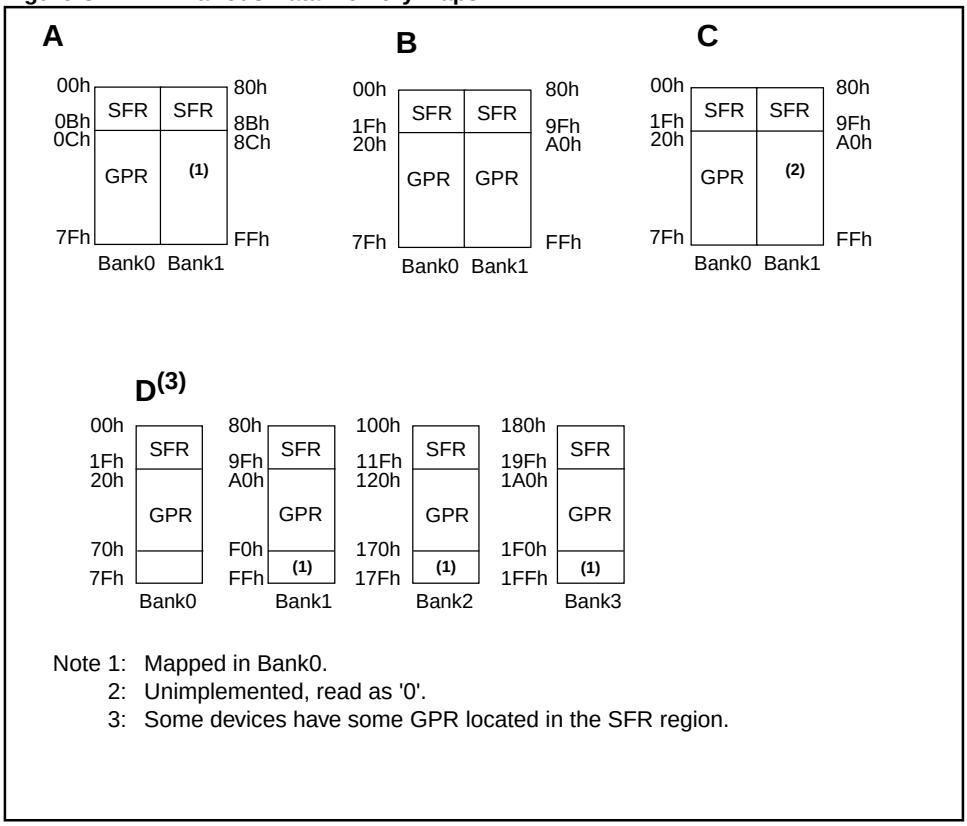
The following subsections discuss the implementations of these enhancements.

C.1 Data Memory Map

The Data Memory Map shows the location of the Special Function Registers (SFRs) and the General Purpose Registers (GPRs). SFRs provide controls and give status on the operation of the device, while the GPRs are the general purpose RAM.

Figure C-1 show the various memory maps that have been implemented in the midrange family. Memory Map **A** was implemented on the first midrange devices. They were 18/20-pin devices that had limited peripheral features. When the product roadmap dictated the requirement for devices with increased I/O, and a richer peripheral set, memory map **B** was implemented. Memory map **C** is actually a subset of memory map **B**, but context saving (due to an interrupt) requires additional software overhead. This is because there is no GPR in Bank1. To minimize the context saving software, memory map **D** was defined. A common RAM memory map will be used for all future devices. See the **"Memory Organization"** section for use and implementation of the Midrange PICmicro's memory.

Figure C-1: Various Data Memory Maps



Note 1: Mapped in Bank0.
2: Unimplemented, read as '0'.
3: Some devices have some GPR located in the SFR region.

C.2 SSP (Synchronous Serial Port) Module

The SSP module has two modes of operation;

- SPI (Serial Peripheral Interface)
- I^2C (Inter-Integrated Circuit).

There are now three different SSP modules that exist in Microchip's design library. The first SSP module (now called Basic SSP) implements two of the four SPI modes, and the I^2C module in slave mode. The second SSP module (called SSP) implements all four SPI modes, and the I^2C module in slave mode. The third SSP module (called Master SSP) implements all four SPI modes, and the I^2C module in master and slave modes. Table C-1 shows the devices that have an SSP module and denotes which version is implemented. As new devices are introduced, either the SSP module or Master SSP module will be implemented (that is, the Basic SSP module is being phased out). Only select devices will be introduced with the Master SSP module due to the size (silicon area => cost) difference in relation to the SSP module. If your application requires I^2C Master mode, then you should also check into Microchip's high-end family, PIC17CXXX.

Table C-1: Devices With an SSP module

Device	Synchronous Serial Port Version		
	SSP	Basic SSP	Master SSP (1)
PIC16C62	—	Yes	—
PIC16C62A	—	Yes	—
PIC16CR62	—	Yes	—
PIC16C63	—	Yes	—
PIC16CR63	—	Yes	—
PIC16C64	—	Yes	—
PIC16C64A	—	Yes	—
PIC16CR64	—	Yes	—
PIC16C65	—	Yes	—
PIC16C65A	—	Yes	—
PIC16CR65	—	Yes	—
PIC16C66	Yes	—	—
PIC16C67	Yes	—	—
PIC16C72	—	Yes	—
PIC16CR72	Yes	—	—
PIC16C73	—	Yes	—
PIC16C73A	—	Yes	—
PIC16C74	—	Yes	—
PIC16C74A	—	Yes	—
PIC16C76	Yes	—	—
PIC16C77	Yes	—	—
PIC16C923	Yes	—	—
PIC16C924	Yes	—	—
Future Devices with SSP module	See Device Data Sheet	—	See Device Data Sheet

Note 1: At present NO midrange devices are available with the Master SSP module. Please refer to Microchip's Web site or BBS for release of Product Briefs. You will be able to find out the details of features for new devices.

This module is available on Microchip's High End family (PIC17CXXX). Please refer to Microchip's Web site, BBS, Regional Sales Office, or Factory Representatives.

C.3 A/D (Analog-to-Digital) Module

There now exists several different versions of the A/D module in Microchip's design library. The first A/D module (now called Basic 8-bit A/D) is an 8-bit A/D with four input channels. The second A/D module (called 8-bit A/D) is an 8-bit A/D with up to 8 input channels. The Third A/D module (called 10-bit A/D) is a 10-bit A/D with up to16 input channels implemented. Table C-2 shows which devices have an A/D module, and the version implemented. As new devices are introduced, either the 8-bit A/D module or 10-bit A/D module will be implemented (that is the Basic 8-bit A/D module is being phased out). If your application requires the 10-bit A/D, you should refer to Microchip's High End Family (PIC17CXXX). This family currently has some devices that have this module implemented.

Table C-2: Devices With A/D modules

Device	8-bit A/D	Basic 8-bit A/D	10-bit A/D (1)	Slope A/D
PIC16C710	—	Yes	—	
PIC16C71	—	Yes	—	
PIC16C711	—	Yes	—	
PIC16C715	—	Yes	—	
PIC16C72	Yes	—	—	
PIC16CR72	Yes	—	—	—
PIC16C73	Yes	—	—	
PIC16C73A	Yes	—	—	
PIC16C74	Yes	—	—	
PIC16C74A	Yes	—	—	
PIC16C76	Yes	—	—	
PIC16C77	Yes	—	—	
PIC16C924	Yes	—	—	
PIC14C000	—	—	—	Yes
Future Devices with A/D module	See Device Data Sheet	See Device Data Sheet	See Device Data Sheet	See Device Data Sheet

Note 1: At present NO midrange devices are available with the 10-bit A/D module. Please refer to Microchip's Web site or BBS for release of Product Briefs. You will be able to find out the details of features for new devices.

This module is available on Microchip's High End family (PIC17CXXX). Please refer to Microchip's Web site, BBS, Regional Sales Office, or Factory Representatives.

C.4 Brown-out Reset

An internal Brown-out Reset (BOR) circuit was added as a special feature. This circuit will be added to most new devices. The exception will be for devices whose target market will require normal operation below the BOR trip point (handheld battery applications). Table C-3 shows the devices that evolved into having the BOR circuitry.

Table C-3: Devices That Were Revised to Include On-chip Brown-out Reset

Base Device No Brown-out Reset	Subsequent Device with Brown-out Reset
PIC16C62	PIC16C62A
PIC16C64	PIC16C64A
PIC16C65	PIC16C65A
PIC16C71	PIC16C711
PIC16C73	PIC16C73A
PIC16C74	PIC16C74A

C.5 Comparator

If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF interrupt flag bit may not get set.

C.6 $\overline{\text{MCLR}}$ Filter

The master clear ($\overline{\text{MCLR}}$) logic has had a filter added. This filter ignores short duration (glitch) low level pulses on the Master Clear pin. Table C-4 shows whether the device has the master clear filter.

Table C-4: Devices With Master Clear Filter

Device	Master Clear	
	No Filter (Fast Reset)	Filter
PIC16C61	Yes	—
PIC16C62	Yes	—
PIC16C62A	—	Yes
PIC16CR62	—	Yes
PIC16C63	—	Yes
PIC16CR63	—	Yes
PIC16C64	Yes	—
PIC16C64A	—	Yes
PIC16CR64	—	Yes
PIC16C65	Yes	—
PIC16C65A	—	Yes
PIC16CR65	—	Yes
PIC16C66	—	Yes
PIC16C67	—	Yes
PIC16C620	—	Yes
PIC16C621	—	Yes
PIC16C622	—	Yes
PIC16C710	—	Yes
PIC16C71	Yes	—
PIC16C711	—	Yes
PIC16C715	—	Yes
PIC16C72	—	Yes
PIC16CR72	—	Yes
PIC16C73	Yes	—
PIC16C73A	—	Yes
PIC16C74	Yes	—
PIC16C74A	—	Yes
PIC16C76	—	Yes
PIC16C77	—	Yes
PIC16C83	Yes	—
PIC16C84	Yes	—
PIC16F83	Yes	—
PIC16F84	Yes	—
PIC16C923	—	Yes
PIC16C924	—	Yes
All New Devices	—	Yes

C.7 USART

The original USART/SCI module that was offered on Midrange devices specified a “high speed” mode (when the BRGH control bit is set). Due to the design of the sampling circuitry, the operation of this mode was not as robust as desired. The sampling circuitry has been changed so that operation now meets Microchip’s requirements. The difference in the sampling is described in the **“USART”** section. Table C-5 shows which devices use the new and old sampling logic.

Table C-5: USART/SCI Sampling Logic

Device	Sampling Logic	
	Old	New
PIC16C63	Yes	—
PIC16CR63	Yes	—
PIC16C65	Yes	—
PIC16C65A	Yes	—
PIC16CR65	Yes	—
PIC16C66	—	Yes
PIC16C67	—	Yes
PIC16C73	Yes	—
PIC16C73A	Yes	—
PIC16C74	Yes	—
PIC16C74A	Yes	—
PIC16C76	—	Yes
PIC16C77	—	Yes
New Devices with USART/SCI module	—	Yes

C.8 Device Oscillator

A new mode has been added into the device oscillator which allows the device to operate from an internal RC. This is specified at time of device programming (configuration word). This mode will be included on many future devices. See the device data sheets configuration word to determine if the device supports this mode.

C.9 Parallel Slave Port

The control pins have changed from level sensitive to edge sensitive.

Table C-6: Parallel Slave Port Change Sensitivity

Device	Sensitivity	
	Level	Edge
PIC16C64	Yes	—
PIC16C64A	—	Yes
PIC16C65	Yes	—
PIC16C65A	—	Yes
PIC16C67	—	Yes
PIC16C74	Yes	—
PIC16C74A	—	Yes
PIC16C77	—	Yes
New Devices with Parallel Slave Port	—	Yes

APPENDIX D: REVISION HISTORY

Revision A

This is the initial released revision of the Reference Guide Appendix.