Section 30. Electrical Specifications

HIGHLIGHTS

30.1 Introduction

This section is intended to show you the electrical specifications that may be specified in a particular device data sheet and what is meant by the specification. This section is **NOT** intended to give the values of these specifications. For the device specific values you **must** refer to the device's data sheet. All values show in this section should be considered as Example Values.

In the description of the device and the functional modules (previous sections), there have been references to electrical specification parameters. These references have been hyperlinked in the electronic version to aid in the use of this manual.

Note: Before starting any design, Microchip HIGHLY recommends that you acquire the most recent copy of the device data sheet and review the electrical specifications to ensure that they will meet your requirements.

Throughout this section, certain terms will be used. Table 30-1 shows the conventions that will be used.

Table 30-1: Term Conventions

Term	Description
PIC16**C**XXX	For devices tested to standard voltage range
PIC16**LC**XXX	For devices tested to extended voltage range
PIC16**F**XXX	For devices tested to standard voltage range
PIC16**LF**XXX	For devices tested to extended voltage range
PIC16**CR**XXX	For devices tested to standard voltage range
PIC16**LCR**XXX	For devices tested to extended voltage range
PIC16XXXX-**04**	For devices that have been tested up to 4 MHz operation
PIC16XXXX-**08**	For devices that have been tested up to 8 MHz operation
PIC16XXXX-**10**	For devices that have been tested up to 10 MHz operation
PIC16XXXX-**20**	For devices that have been tested up to 20 MHz operation
LP osc	For devices configured with the LP device oscillator selected
XT osc	For devices configured with the XT device oscillator selected
HS osc	For devices configured with the HS device oscillator selected
RC osc	For devices configured with the RC device oscillator selected
Commercial	For devices with the commercial temperature range grading ($0^{\circ}C \le T_A \le +70^{\circ}C$)
Industrial	For devices with the industrial temperature range grading ($-40^{\circ}C \le T_A \le +85^{\circ}C$)
Extended	For devices with the extended temperature range grading ($-40^{\circ}C \le T_A \le +125^{\circ}C$)

30.2 Absolute Maximums

The Absolute Maximum Ratings specify the worst case conditions that can be applied to the device. These ratings are not meant as operational specifications, and stresses above the listed values may cause damage to the device. Specifications are not always stand-alone, that is, the specification may have other requirements as well.

An example of this is the "maximum current sourced/sunk by any I/O pin". The number of I/O pins that can be sinking/sourcing current, at any one time, is dependent upon the maximum current sunk/source by the port(s) (combined) and the maximum current into the VDD pin or out of the VSS pin. In this example, the physical reason is the Power and Ground bus width to the I/O ports and internal logic. If these specifications are exceeded, then electromigration may occur on these Power and Ground buses. Over time electromigration would cause these buses to open (be disconnected from the pin), and therefore cause the logic attached to these buses to stop operating. So exceeding the absolute specifications may cause device reliability issues.

Input Clamp Current is defined as the current through the diode to VSS/VDD if pin voltage exceeds specification.

Example Absolute Maximum Ratings†

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to VSS (except VDD, $\overline{MCLR}$, and RA4) ..... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS ..... -0.3 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS **(2)** ..... 0 to +14V

Voltage on RA4 with respect to Vss ..... 0 to +14V

Total power dissipation **(1)** 1.0W

Maximum current out of VSS pin ..... 300 mA

Maximum current into VDD pin ..... 250 mA

Input clamp current, IIK (VI < 0 or VI > VDD) ..... ± 20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ..... ± 20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by PORTA, PORTB, and PORTE (combined) ..... 200 mA

Maximum current sourced by PORTA, PORTB, and PORTE (combined) ..... 200 mA

Maximum current sunk by PORTC and PORTD (combined) ..... 200 mA

Maximum current sourced by PORTC and PORTD (combined) ..... 200 mA

Maximum current sourced by PORTC and PORTD (combined) ..... 200 mA

Maximum current sourced by PORTF and PORTG (combined) ..... 100 mA

Maximum current sourced by PORTF and PORTG (combined) ..... 100 mA

Note 1: Power dissipation is calculated as follows:
Pdis = VDD x {IDD - ∑ IOH} + ∑ {(VDD - VOH) x IOH} + ∑(VOl x IOL)

Note 2: Voltage spikes below VSS at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

30.3 Device Selection Table

This table in the Device Data Sheet is intended to assist you in determining which oscillators are tested for which devices, and some of the specifications that are tested. Any oscillator may be selected at time of programming, but only the specified oscillator is tested by Microchip.

Since the RC and XT oscillators are only rated to 4 MHz, they are only tested on the -04 (4 MHz) devices.

PICmicros rated for 10 MHz or 20 MHz are only tested in HS mode. In Table 30-2 the IPD is grayed out for the HS mode since there is not an IPD test point within the voltage range of the HS oscillator. The value shown is a typical value from characterization.

Battery applications usually require an extended voltage range. Devices marked **LC** have an extended voltage range and have the RC, XT, and LP oscillators tested.

Windowed devices are superset devices and have had the oscillators tested to all the specification ranges of the -04, -20, and LC devices. The temperature range that the device is tested to should be considered commercial, though at a later time they may be tested to industrial or extended temperature levels.

Table 30-2: Example Cross Reference of Device Specifications for Oscillator Configurations and Frequencies of Operation (Commercial Devices)

OSC	PIC16CXXX-04	PIC16CXXX-10	PIC16CXXX-20	PIC16LCXXX-04	Windowed Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5 µA max. at 3V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 5.5V IPD: 16 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications.
It is recommended that the user select the device type that ensures the specifications required.

Note: Devices that are marked with Engineering Sample (ENG SMP) are tested to the current engineering test program at time of the device testing. There is no implied warranty that these devices have been tested to any or all specifications in the Device Data Sheet.

30.4 Device Voltage Specifications

These specifications relate to the device VDD and the device power-up and function.

Supply Voltage is the voltage level that must be applied to the device for the proper functional operation.

Ram Data Retention Voltage is the level that the device voltage may be at and still retain the data value.

VDD Start Voltage to ensure the internal Power-on Reset signal, is the level that VDD must start from to ensure that the POR circuitry will operate properly.

VDD Rise Rate to ensure internal Power-on Reset signal, is the minimum slope that VDD must rise at to cause the POR circuitry to trip.

Brown-out Reset Voltage is the voltage range where the brown-out circuitry may trip. When the BOR circuitry trips, the device will either be in brown-out reset, or just came out of brown-out reset.

Table 30-3: Example DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		PIC16**C**XXX	4.0	—	6.0	V	XT, RC and LP osc mode
		PIC16**LC**XXX	2.5	—	6.0	V	
D001A		PIC16**C**XXX	4.5	—	5.5	V	HS osc mode
D002	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details
	VBOR	**Brown-out Reset Voltage**					
D005			3.7	4.0	4.3	V	BODEN bit in Configuration Word enabled
D005A			3.7	4.0	4.4	V	Extended Temperature Range Devices Only

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

30.5 Device Current Specifications

IDD is the current (I) that the device consumes when the device is in operating mode. This test is taken with all I/O as inputs, either pulled high or low. That is, there are no floating inputs, nor are any pins driving an output (with a load).

IPD is the current (I) that the device consumes when the device is in sleep mode (power-down), referred to as power-down current. These tests are taken with all I/O as inputs, either pulled high or low. That is, there are no floating inputs, nor are any pins driving an output (with a load), weak pull-ups are disabled.

A device may have certain features and modules that can operate while the device is in sleep mode. Some on these modules are:

- Watchdog Timer (WDT)
- Brown-out Reset (BOR) circuitry
- Timer1
- Analog to Digital converter
- LCD module
- Comparators
- Voltage Reference

When all features are disabled, the device will consume the lowest possible current (the leakage current). If any of these features are operating while the device is in sleep, a higher current will occur. The difference between the lowest power mode (everything off) at only that one feature enabled (such as the WDT) is what we call the **Module Differential Current**. If more then one feature is enabled then the expected current can easily be calculated as: the base current (everything disabled and in sleep mode) plus all Module Differential Currents (delta currents). Example 30-1 shows an example of calculating the typical currents for a device at 5V, with the WDT and Timer1 oscillator enabled.

Example 30-1: IPD Calculations with WDT and Timer1 Oscillator Enabled (@ 5V)

Base Current	14 nA	; Device leakage current
WDT Delta Current	14 µA	; 14 µA - 14 nA = 14 µA
Timer1 Delta Current	22 µA	; 22 µA - 14 nA = 22 µA
Total Sleep Current	36 µA	;

Table 30-4: Example DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial and -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	IDD	**Supply Current(2,4,5)**					XT, RC osc configuration (PIC16**C**XXX-**04**)
D010			—	2.7	5	mA	FOSC = 4 MHz, VDD = 5.5V
			—	2.0	3.8	mA	FOSC = 4 MHz, VDD = 3.0V
D010A			—	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D010C			—	7.7	5	mA	INTRC osc configuration, Fosc = 4 MHz, VDD = 5.5V
D013			—	13.5	30	mA	HS osc configuration (PIC16**C**XXX-**20**) Fosc = 20 MHz, VDD = 5.5V
	IPD	**Power-down Current(3,5)**					
D020			—	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
			—	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
			—	1.5	21	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021			—	0.9	13.5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
			—	1.5	24	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021A			—	0.9	18	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D021B			—	1.5	—	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Not Applicable.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

Table 30-5: Example DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0˚C ≤ TA ≤ +70˚C for commercial, -40˚C≤ TA ≤ +85˚C for industrial and -40˚C ≤ TA ≤ +125˚C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Module Differential Current (5)					
D022	ΔIWDT	Watchdog Timer	—	6.0	20	µA	VDD = 4.0V
			—	—	25	µA	-40°C to +125°C
D022A	ΔIBOR	Brown-out Reset	—	350	425	µA	BODEN bit is clear, VDD = 5.0V
D023	ΔICOMP	Comparator (per Comparator)	—	85	100	µA	VDD = 4.0V
D023A	ΔIVREF	Voltage Reference	—	94	300	µA	VDD = 4.0V
D024	ΔILCDRC	LCD internal RC osc enabled	—	6.0	20	µA	VDD = 3.0V
D024A	ΔILCDVG	LCD voltage generation	—	TBD	TBD	µA	VDD = 3.0V
D025	ΔIT1OSC	Timer1 oscillator	—	3.1	6.5	µA	VDD = 3.0V
D026	ΔIAD	A/D Converter	—	1.0	—	µA	A/D on, not converting
D027	ΔISAD	Slope A/D (Total)	—	165 *	250 *	µA	REFOFF = 0
D027A	ΔISADVR	Slope A/D Bandgap Voltage Reference	—	20 *	30 *	µA	REFOFF = 0
D027B	ΔISADCDAC	Slope A/D Programmable Current Source	—	50 *	70 *	µA	ADCON1<7:4> = 1111b
D027C	ΔISADSREF	Slope A/D Reference Voltage Divider	—	55 *	85 *	µA	ADOFF = 0
D027D	ΔISADCMP	Slope A/D Comparator	—	40 *	65 *	µA	ADOFF = 0

† Data in “Typ” column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

30.6 Input Threshold Levels

The **Input Low Voltage** (V_{IL}) is the voltage level that will be read as a logic '0'. An input may not read a '0' at a voltage level above this. All designs should be to the specification since device to device (and to a much lesser extent pin to pin) variations will cause this level to vary.

The **Input High Voltage** (V_{IH}) is the voltage level that will be read as a logic '1'. An input may read a '1' at a voltage level below this. All designs should be to the specification since device to device (and to a much lesser extent pin to pin) variations will cause this level to vary.

The I/O pins with TTL levels are shown with two specifications. One is the industry standard TTL specification, which is specified for the voltage range of 4.5V to 5.5V. The other is a specification that operates over the entire voltage range of the device. The better of these two specifications may be used in the design.

Table 30-6: Example DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range (4)
D030A			—	—	0.8	V	4.5V ≤ VDD ≤ 5.5V (4)
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	For entire VDD range
D032		$\overline{MCLR}$, OSC1 (RC mode)	VSS	—	0.2VDD	V	
D033		OSC1 (XT, HS and LP modes)(1)	VSS	—	0.3VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:					
D040		with TTL buffer	0.25VDD + 0.8V	—	VDD	V	For entire VDD range (4)
D040A			2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V (4)
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS and LP modes)(1)	0.7VDD	—	VDD	V	
D043		OSC1 (RC mode)	0.9VDD	—	VDD	V	
D050	VHYS	Hysteresis of Schmitt Trigger Inputs	TBD	—	—	V	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PICmicro be driven with an external clock while in RC mode.
2: Not Applicable.
3: Not Applicable.
4: The better of the two specifications may be used. For VIL this would be the higher voltage and for VIH this would be the lower voltage.

30.7 I/O Current Specifications

The PORT/GIO **Weak Pull-up Current** is the additional current that the device will draw when the weak pull-ups are enabled.

Leakage Currents are the currents that the device consumes, since the devices are manufactured in the real world and do not adhere to their ideal characteristics. Ideally there should be no current on an input, but due to the real world there is always some parasitic path that consumes negligible current.

Table 30-7: Example DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IIL	**Input Leakage Current(2,3)**					
D060		I/O ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A		CDAC	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		$\overline{MCLR}$	—	—	±5	µA	VSS ≤ VPIN ≤ VDD
D063			—	—	±5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc modes
	IPU	**Weak Pull-up Current**					
D070	IPURB	PORTB weak pull-up current	50	250	400	µA	VDD = 5V, VPIN = VSS
D070A	IPUGIO	GIO weak pull-up current	50	250	400	µA	VDD = 5V, VPIN = VSS
		Programmable Current Source (Slope A/D devices)					CDAC pin = 0V
D160		Output Current	18.75	33.75	48.75	µA	ADCON1<7:4> = 1111b (full-scale)
D160A			1.25	2.25	3.25	µA	ADCON1<7:4> = 0001b (1 LSB)
D160B			-0.5	0	0.5	µA	ADCON1<7:4> = 0000b (zero-scale)

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PICmicro be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

30.8 Output Drive Levels

The **Output Low Voltage** (V_{OL}) of an I/O pin depends on the external connections to that I/O. If an I/O pin is shorted to V_{DD}, no matter the drive capability of the I/O pin, a low level would not be reached (and the device would consume excessive drive current). The V_{OL} is the output voltage that the I/O pin will drive, given the I/O does not need to sink more then the I_{OL} current (at the specified device voltage) as specified in the conditions portion of the specification.

The **Output High Voltage** (V_{OH}) of an I/O pin depends on the external connections to that I/O. If an I/O pin is shorted to V_{SS}, no matter the drive capability of the I/O pin, a high level would not be reached (and the device would consume excessive drive current). The V_{OH} is the output voltage that the I/O pin will drive, given the I/O does not need to source more then the I_{OH} current (at the specified device voltage) as specified in the conditions portion of the specification.

Table 30-8: Example DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	V_{OL}	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	I_{OL} = 8.5 mA, V_{DD} = 4.5V, -40°C to +85°C
D080A			—	—	0.6	V	I_{OL} = 7.0 mA, V_{DD} = 4.5V, -40°C to +125°C
D083		OSC2/CLKOUT (RC mode)	—	—	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, -40°C to +85°C
D083A			—	—	0.6	V	I_{OL} = 1.2 mA, V_{DD} = 4.5V, -40°C to +125°C
	V_{OH}	**Output High Voltage(3)**					
D090		I/O ports	V_{DD} - 0.7	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V, -40°C to +85°C
D090A			V_{DD} - 0.7	—	—	V	I_{OH} = -2.5 mA, V_{DD} = 4.5V, -40°C to +125°C
D092		OSC2/CLKOUT (RC mode)	V_{DD} - 0.7	—	—	V	I_{OH} = -1.3 mA, V_{DD} = 4.5V, -40°C to +85°C
D092A			V_{DD} - 0.7	—	—	V	I_{OH} = -1.0 mA, V_{DD} = 4.5V, -40°C to +125°C
D150	V_{OD}	**Open-drain High Voltage**	—	—	12	V	RA4 pin
		Programmable Current Source					
D170	V_{PCS}	Output Voltage Range	Vss	—	V_{DD} – 1.4	V	CDAC pin
D171	SN_{PCS}	Output Voltage Sensitivity	– 0.1	–0.01	—	%/V	Vss ≤ V_{CDAC} ≤ V_{DD} – 1.4
		Bandgap Reference					
D180	V_{BGR}	Output Voltage Range	1.14	1.19	1.24	V	on AN0 pin when AMUXOE =1 and ADCS3:ADSC0 = 0100b

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PICmicro be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

30.9 I/O Capacitive Loading

These specifications indicate the conditions that the I/O pins have on them from the device tester. These loadings effect the specifications for the timing specifications. If the loading in you application are different, then you will need to determine how this will effect the characteristic of the device in your system. Capacitances less then these specifications should not have effects on a system.

Table 30-9: Example DC Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	To meet the Timing Specifications of the Device
D102	CB	SCL, SDA	—	—	400	pF	In I^2C mode

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PICmicro be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

30.10 Data EEPROM / Flash

Table 30-10: Example Data EEPROM / Flash Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Data EEPROM Memory					
D120	ED	Endurance	1M	10M	—	E/W	25°C at 5V
D121	VDRW	VDD for read/write	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	—	10	ms	
		Program Flash Memory					
D130	EP	Endurance	100	1000	—	E/W	
D131	VPR	VDD for read	VMIN	—	6.0	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for erase/write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	—	10	ms	

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

30.11 LCD

Table 30-11: Example LCD Module Electrical Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D200	VLCD3	LCD Voltage on pin VLCD3	VDD - 0.3	—	Vss + 7.0	V	
D201	VLCD2	LCD Voltage on pin VLCD2	—	—	VLCD3	V	
D202	VLCD1	LCD Voltage on pin VLCD1	—	—	VDD	V	
D210	RCOM	Com Output Source Impedance	—	—	1k	Ω	COM outputs
D211	RSEG	Seg Output Source Impedance	—	—	10k	Ω	SEG outputs
D220	VOH	Output High Voltage	Max (VLCDN) - 0.1	—	Max (VLCDN)	V	COM outputs IOH = 25 µA SEG outputs IOH = 3 µA
D221	VOL	Output Low Voltage	Min (VLCDN)	—	Min (VLCDN) + 0.1	V	COM outputs IOL = 25 µA SEG outputs IOL = 3 µA

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: 0 ohm source impedance at VLCD.

Table 30-12: Example VLCD Charge Pump Electrical Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D250	IVADJ	VLCDADJ Regulated Current Output	—	10	—	µA	
D251	Ivr	VLCDADJ Current Consumption	—	—	20	µA	
D252	$\frac{\Delta I_{VADJ}}{\Delta V_{DD}}$	VLCDADJ Current VDD Rejection	—	—	0.1/1	µA/V	
D253	$\frac{\Delta I_{VADJ}}{\Delta T}$	VLCDADJ Current Variation With Temperature	—	—	0.1/70	µA/°C	
D260(1)	RVADJ	VLCDADJ External Resistor	100	—	230	kΩ	
D265	VVADJ	VLCDADJ Voltage Limits	1.0	—	2.3	V	
D271(1)	CECPC	External Charge Pump Capacitance	—	0.5	—	µF	

Note 1: For design guidance only.

30.12 Comparators and Voltage Reference

Table 30-13: Example Comparator Characteristics

DC CHARACTERISTICS				Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristics**		**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input offset voltage		—	± 5.0	± 10	mV	
D301	VICM	Input common mode voltage		0	—	VDD - 1.5	V	
D302	CMRR	Common Mode Rejection Ratio		35	70	—	db	
300	TRESP	Response Time(1)	PIC16**C**XXX	—	150	400	ns	
300A			PIC16**LC**XXX	—	210	600	ns	
301	TMC2OV	Comparator Mode Change to Output Valid		—	—	10	µs	

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from VSS to VDD.

Table 30-14: Example Voltage Reference Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D310	VRES	Resolution	VDD/32	—	VDD/24	V	
D311	VRAA	Absolute Accuracy	— —	— —	1/4 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
D312	VRUR	Unit Resistor Value (R)	—	2k	—	Ω	
310	TSET	Settling Time(1)	—	—	10	µs	

Note 1: Settling time measured while VRR = 1 and VR3:VR0 transitions from 0000 to 1111.

30.13 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I^2C specifications only)
4. Ts (I^2C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

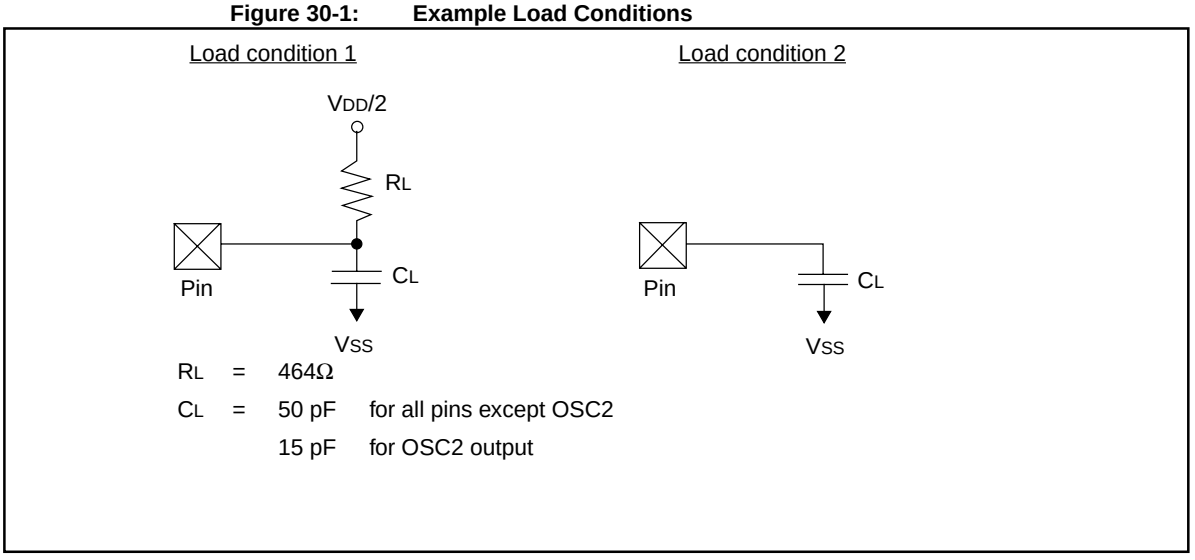
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I^2C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I^2C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

Figure 30-1: Example Load Conditions



30.14 Example External Clock Timing Waveforms and Requirements

Figure 30-2: Example External Clock Timing Waveforms

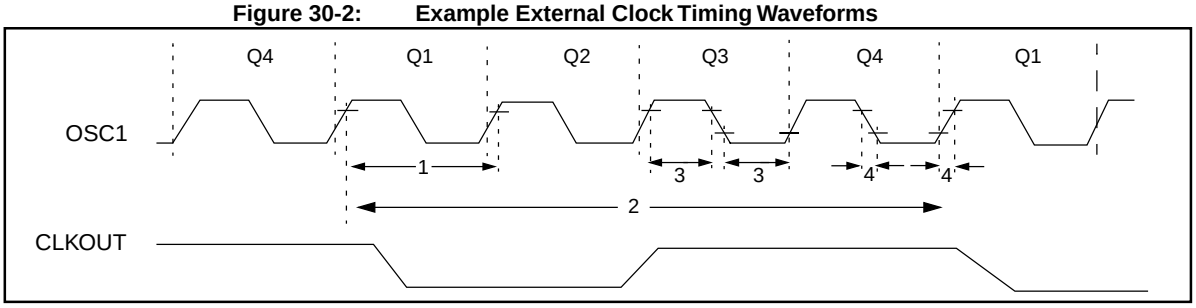


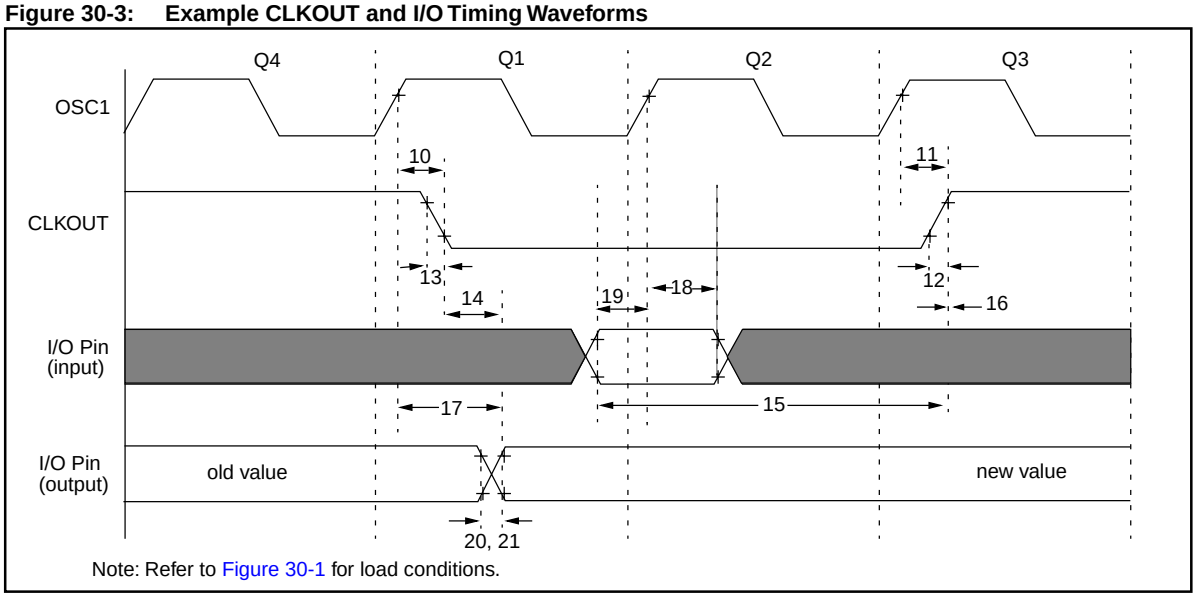
Table 30-15: Example External Clock Timing Requirements

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions	
1A	Fosc	External CLKIN Frequency(1)	DC	—	4	MHz	XT and RC osc	PIC16**C**XXX-**04**
								PIC16**LC**XXX-**04**
			DC	—	10	MHz	HS osc	PIC16**C**XXX-**10**
			DC	—	20	MHz		PIC16**C**XXX-**20**
			DC	—	200	kHz	LP osc	PIC16**LC**XXX-**04**
		Oscillator Frequency(1)	DC	—	4	MHz	RC osc	PIC16**C**XXX-**04**
								PIC16**LC**XXX-**04**
			0.1	—	4	MHz	XT osc	PIC16**C**XXX-**04**
								PIC16**LC**XXX-**04**
			4	—	10	MHz	HS osc	PIC16**C**XXX-**10**
			4	—	20	MHz		PIC16**C**XXX-**20**
			5	—	200	kHz	LP osc mode	PIC16**LC**XXX-**04**
1	Tosc	External CLKIN Period(1)	250	—	—	ns	XT and RC osc	PIC16**C**XXX-**04**
								PIC16**LC**XXX-**04**
			100	—	—	ns	HS osc	PIC16**C**XXX-**10**
			50	—	—	ns		PIC16**C**XXX-**20**
			5	—	—	µs	LP osc	PIC16**LC**XXX-**04**
		Oscillator Period(1)	250	—	—	ns	RC osc	PIC16**C**XXX-**04**
								PIC16**LC**XXX-**04**
			250	—	10,000	ns	XT osc	PIC16**C**XXX-**04**
								PIC16**LC**XXX-**04**
			100	—	250	ns	HS osc	PIC16**C**XXX-**10**
			50	—	250	ns		PIC16**C**XXX-**20**
			5	—	—	µs	LP osc	PIC16**LC**XXX-**04**
2	TCY	Instruction Cycle Time(1)	200	—	DC	ns	TCY = 4/FOSC	
3	TosL, TosH	External Clock in (OSC1) High or Low Time	50	—	—	ns	XT osc	PIC16**C**XXX-**04**
			60	—	—	ns	XT osc	PIC16**LC**XXX-**04**
			2.5	—	—	µs	LP osc	PIC16**LC**XXX-**04**
			15	—	—	ns	HS osc	PIC16**C**XXX-**20**
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT osc	PIC16**C**XXX-**04**
			—	—	50	ns	LP osc	PIC16**LC**XXX-**04**
			—	—	15	ns	HS osc	PIC16**C**XXX-**20**

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Figure 30-3: Example CLKOUT and I/O Timing Waveforms



Note: Refer to Figure 30-1 for load conditions.

Table 30-16: Example CLKOUT and I/O Timing Requirements

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	(1)
11	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	(1)
12	TckR	CLKOUT rise time		—	35	100	ns	(1)
13	TckF	CLKOUT fall time		—	35	100	ns	(1)
14	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	(1)
15	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	(1)
16	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	(1)
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16**C**XXX	100	—	—	ns	
18A			PIC16**LC**XXX	200	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20	TioR	Port output rise time	PIC16**C**XXX	—	10	25	ns	
20A			PIC16**LC**XXX	—	—	60	ns	
21	TioF	Port output fall time	PIC16**C**XXX	—	10	25	ns	
21A			PIC16**LC**XXX	—	—	60	ns	
22††	Tinp	INT pin high or low time		TCY	—	—	ns	
23††	Trbp	RB7:RB4 change INT high or low time		TCY	—	—	ns	
24††	Trcp	RC7:RC4 change INT high or low time		20			ns	

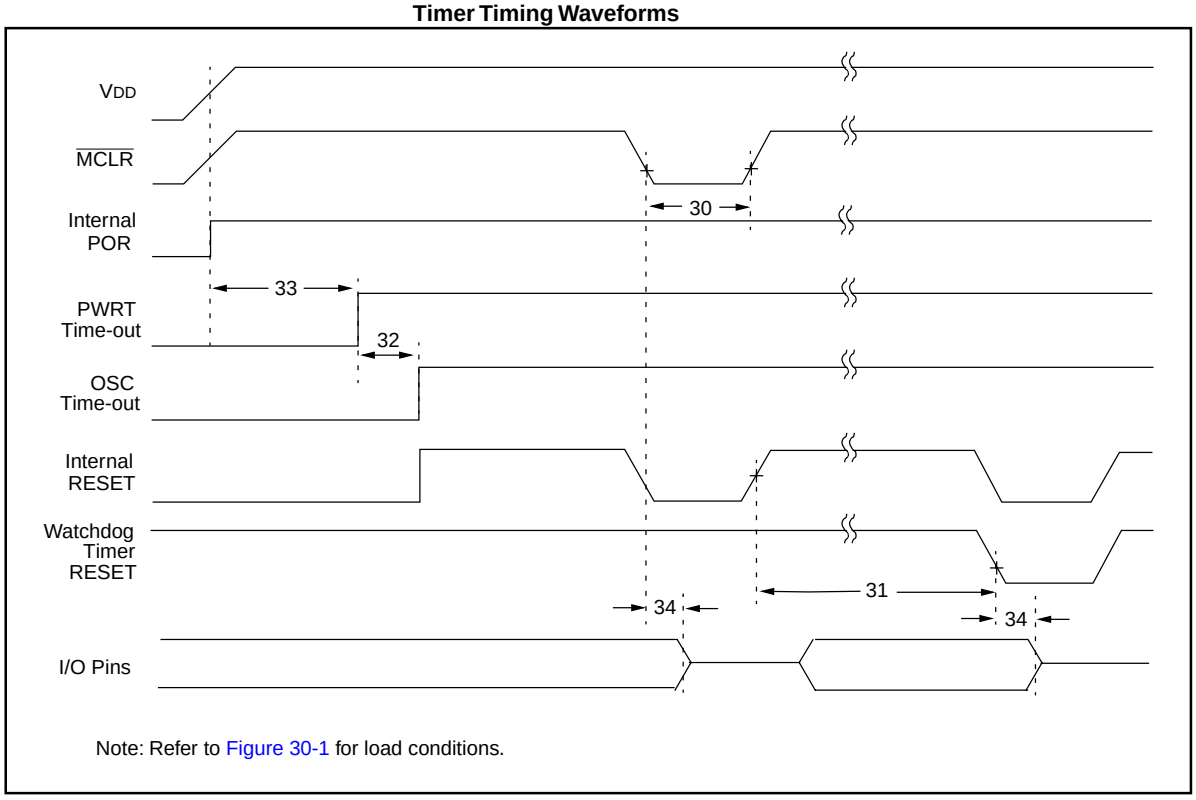
† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

30.15 Example Power-up and Reset Timing Waveforms and Requirements

Figure 30-4: Example Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing Waveforms



Note: Refer to Figure 30-1 for load conditions.

Figure 30-5: Brown-out Reset Timing

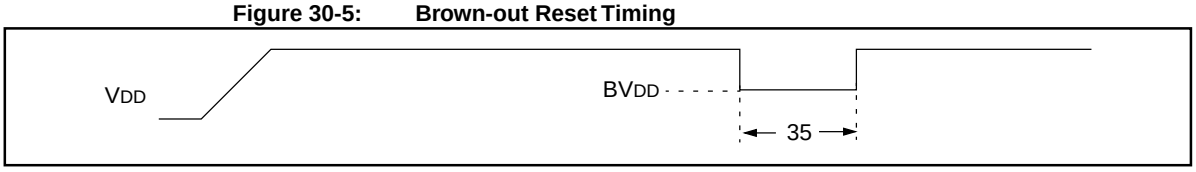


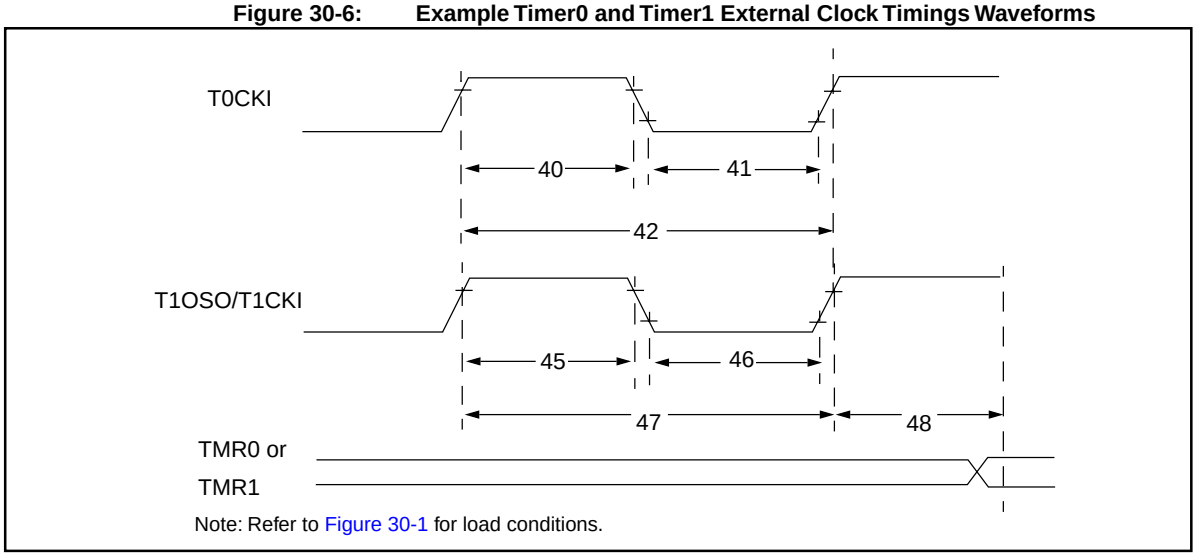
Table 30-17: Example Reset, Watchdog Timer, Oscillator Start-up Timer, Brown-out Reset, and Power-up Timer Requirements

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—	—	µs	VDD = 5V, -40˚C to +125˚C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40˚C to +125˚C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40˚C to +125˚C
34	TIOZ	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	µs	VDD ≤ BVDD (See D005)

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

30.16 Example Timer0 and Timer1 Timing Waveforms and Requirements

Figure 30-6: Example Timer0 and Timer1 External Clock Timings Waveforms



Note: Refer to Figure 30-1 for load conditions.

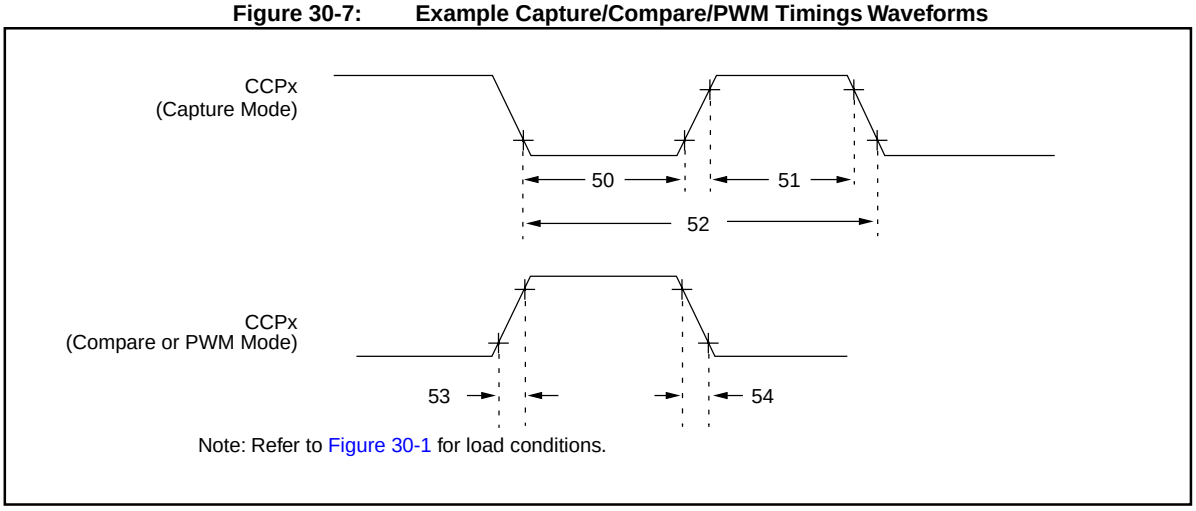
Table 30-18: Example Timer0 and Timer1 External Clock Requirements

Param No.	Symbol	Characteristic			Min	Typ †	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42	Tt0P	T0CKI Period			GREATER OF: 20 µS OR TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4,..., 256)
45	Tt1H	T1CKI High Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16**C**XXX	15	—	—	ns	
				PIC16**LC**XXX	25	—	—	ns	
			Asynchronous	PIC16**C**XXX	30	—	—	ns	
				PIC16**LC**XXX	50	—	—	ns	
46	Tt1L	T1CKI Low Time	Synchronous, no prescaler		0.5TCY + 20	—	—	ns	
			Synchronous, with prescaler	PIC16**C**XXX	15	—	—	ns	
				PIC16**LC**XXX	25	—	—	ns	
			Asynchronous	PIC16**C**XXX	2TCY	—	—	ns	
				PIC16**LC**XXX					
47	Tt1P	T1CKI input period	Synchronous		GREATER OF: 20 µS OR TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		Greater of: 20µS or 4TCY	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting the T1OSCEN bit)			DC	—	200	kHz	
48	Tcke2tmrI	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

30.17 Example CCP Timing Waveforms and Requirements

Figure 30-7: Example Capture/Compare/PWM Timings Waveforms



Note: Refer to Figure 30-1 for load conditions.

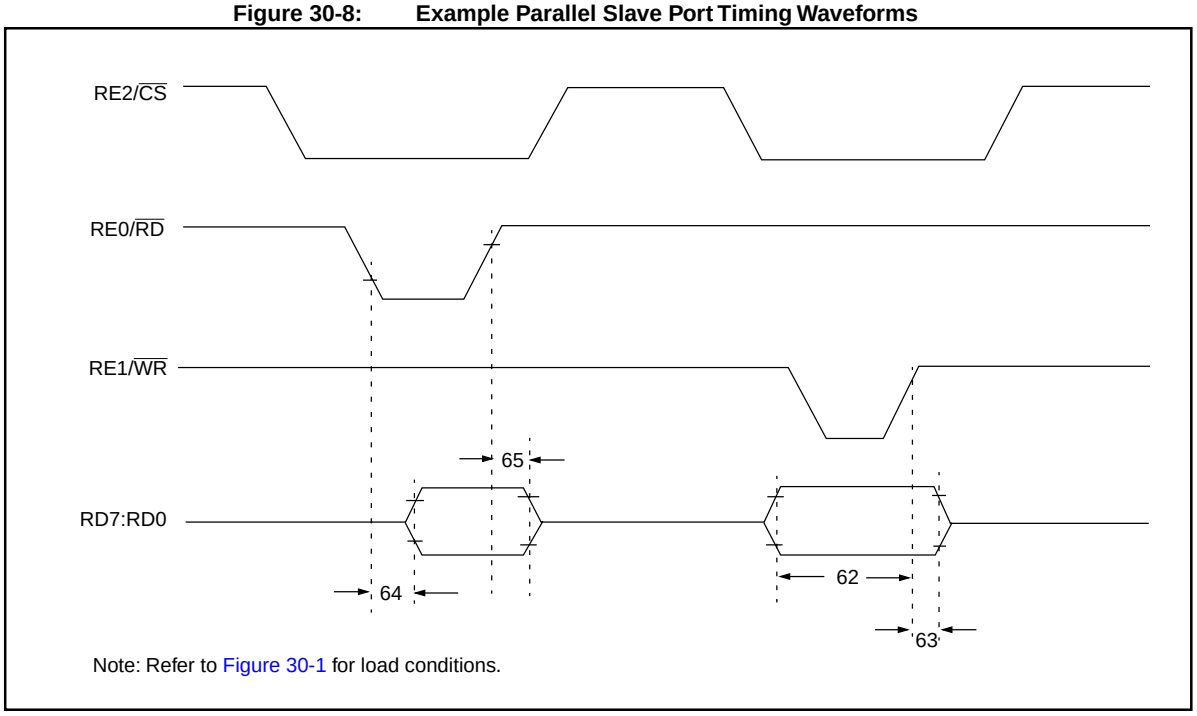
Table 30-19: Example Capture/Compare/PWM Requirements

Param. No.	Symbol	Characteristic			Min	Typ†	Max	Units	Conditions
50	TccL	CCPx input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**XXX	10	—	—	ns	
				PIC16**LC**XXX	20	—	—	ns	
51	TccH	CCPx input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	PIC16**C**XXX	10	—	—	ns	
				PIC16**LC**XXX	20	—	—	ns	
52	TccP	CCPx input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53	TccR	CCPx output fall time		PIC16**C**XXX	—	10	25	ns	
				PIC16**LC**XXX	—	25	45	ns	
54	TccF	CCPx output fall time		PIC16**C**XXX	—	10	25	ns	
				PIC16**LC**XXX	—	25	45	ns	

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

30.18 Example Parallel Slave Port (PSP) Timing Waveforms and Requirements

Figure 30-8: Example Parallel Slave Port Timing Waveforms



Note: Refer to Figure 30-1 for load conditions.

Table 30-20: Example Parallel Slave Port Requirements

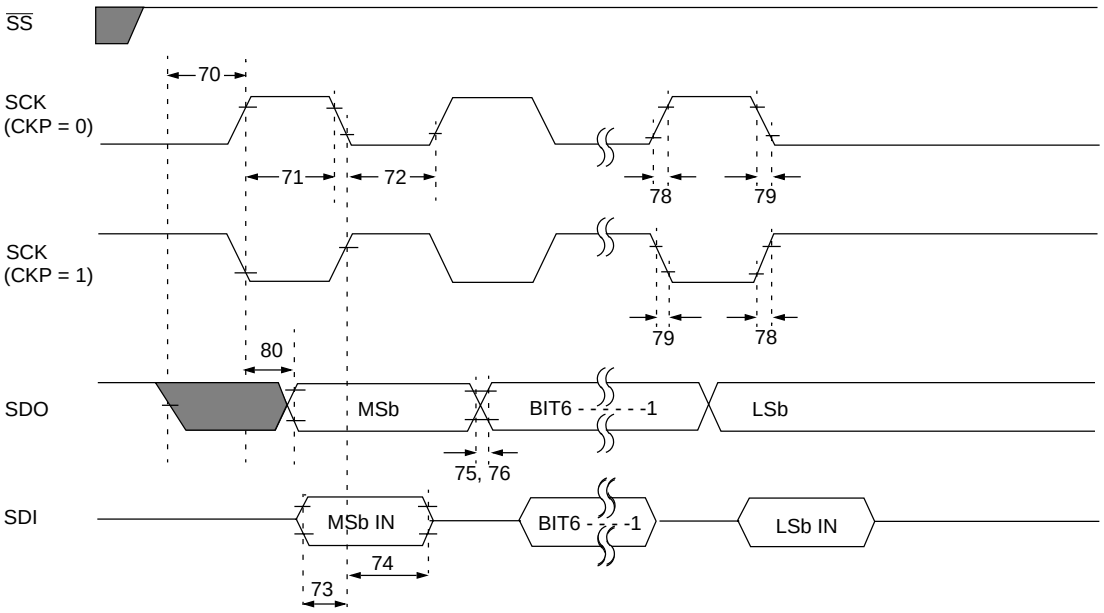
Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ (setup time)		20	—	—	ns	
63	TwrH2dtI	$\overline{WR}\uparrow$ or $\overline{CS}\uparrow$ to data–in invalid (hold time)	PIC16**C**XXX	20	—	—	ns	
			PIC16**LC**XXX	35	—	—	ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data–out valid		—	—	80	ns	
65	TrdH2dtI	$\overline{RD}\uparrow$ or $\overline{CS}\downarrow$ to data–out invalid		10	—	30	ns	
66	TibfINH	Inhibit of the IBF flag bit being cleared from $\overline{WR}\uparrow$ or $\overline{CS}\uparrow$		—	—	3Tcy§		

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

30.19 Example SSP and Master SSP SPI Mode Timing Waveforms and Requirements

Figure 30-9: Example SPI Master Mode Timing (CKE = 0)



Refer to Figure 30-1 for load conditions.

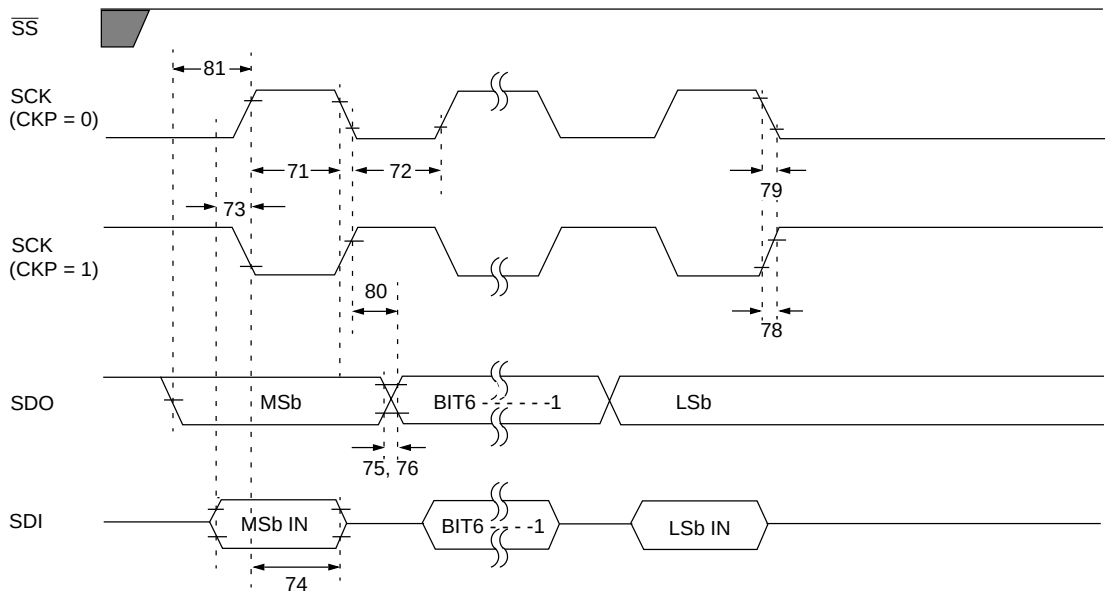
Table 30-21: Example SPI Mode Requirements (Master Mode, CKE = 0)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input		TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX	—	20	45	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
78	TscR	SCK output rise time (master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX	—	20	45	ns	
79	TscF	SCK output fall time (master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX	—	—	100	ns	

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

Figure 30-10: Example SPI Master Mode Timing (CKE = 1)



Refer to Figure 30-1 for load conditions.

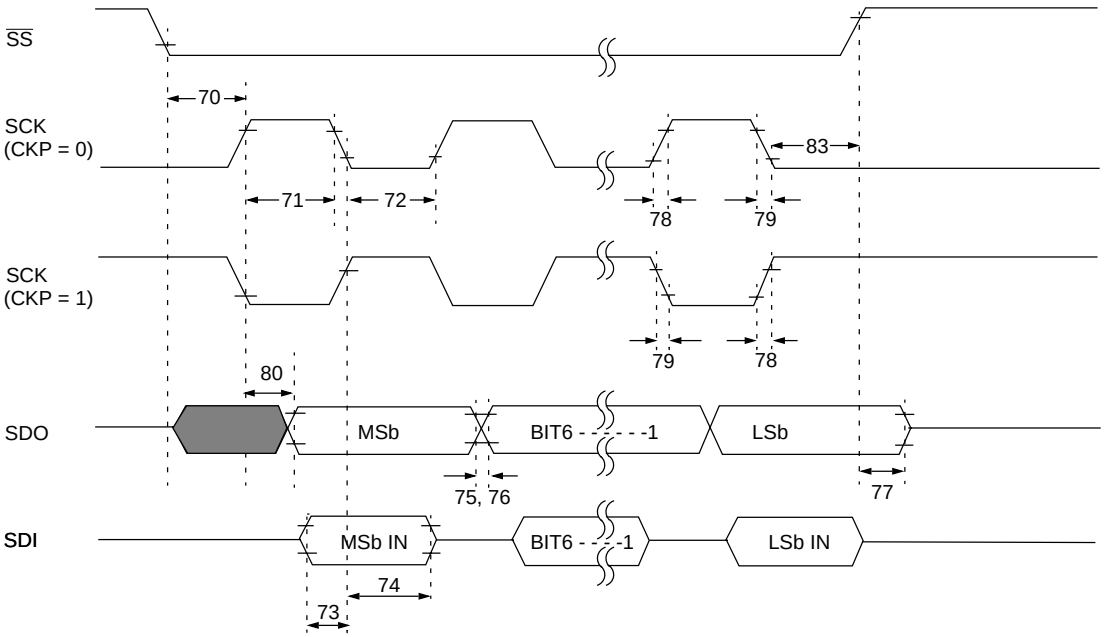
Table 30-22: Example SPI Mode Requirements (Master Mode, CKE = 1)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
78	TscR	SCK output rise time (master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
79	TscF	SCK output fall time (master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX		—	100	ns	
81	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge		TCY	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

Figure 30-11: Example SPI Slave Mode Timing (CKE = 0)



Refer to Figure 30-1 for load conditions.

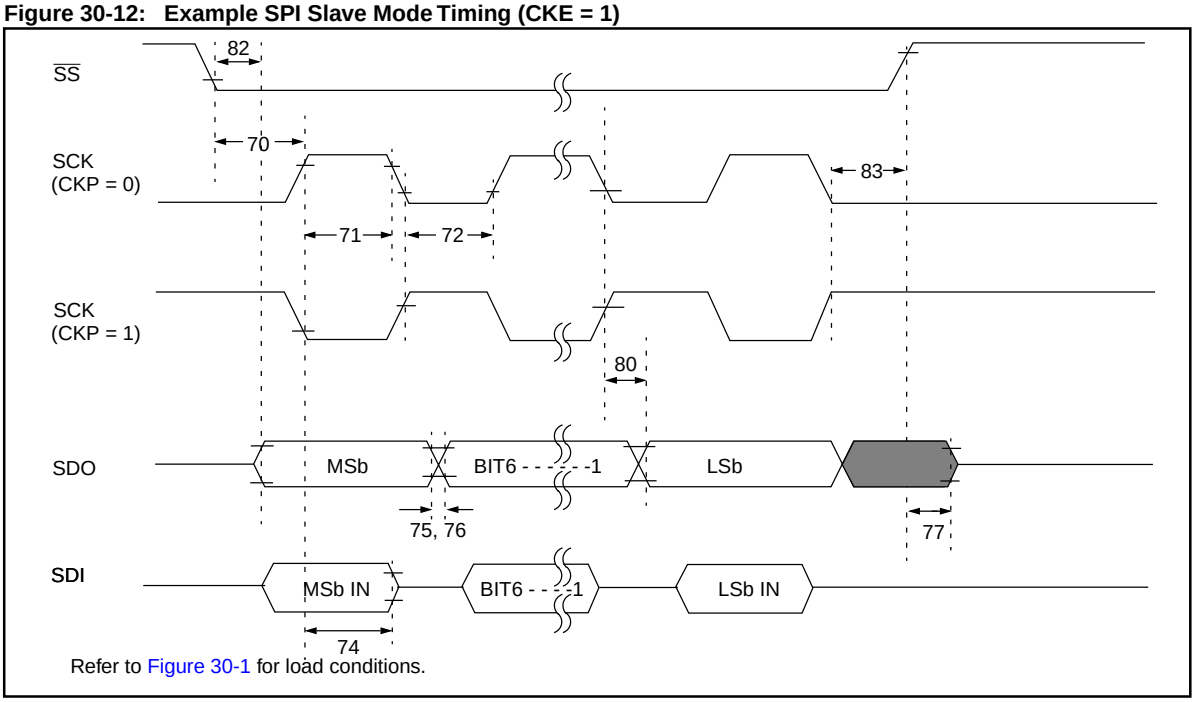
Table 30-23: Example SPI Mode Requirements (Slave Mode Timing (CKE = 0)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input		TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
77	TssH2doZ	$\overline{SS}$↑ to SDO output hi-impedance		10	—	50	ns	
78	TscR	SCK output rise time (master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
79	TscF	SCK output fall time (master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX		—	100	ns	
83	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK edge		1.5TCY + 40	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

Figure 30-12: Example SPI Slave Mode Timing (CKE = 1)



Refer to Figure 30-1 for load conditions.

Table 30-24: Example SPI Slave Mode Mode Requirements (CKE = 1)

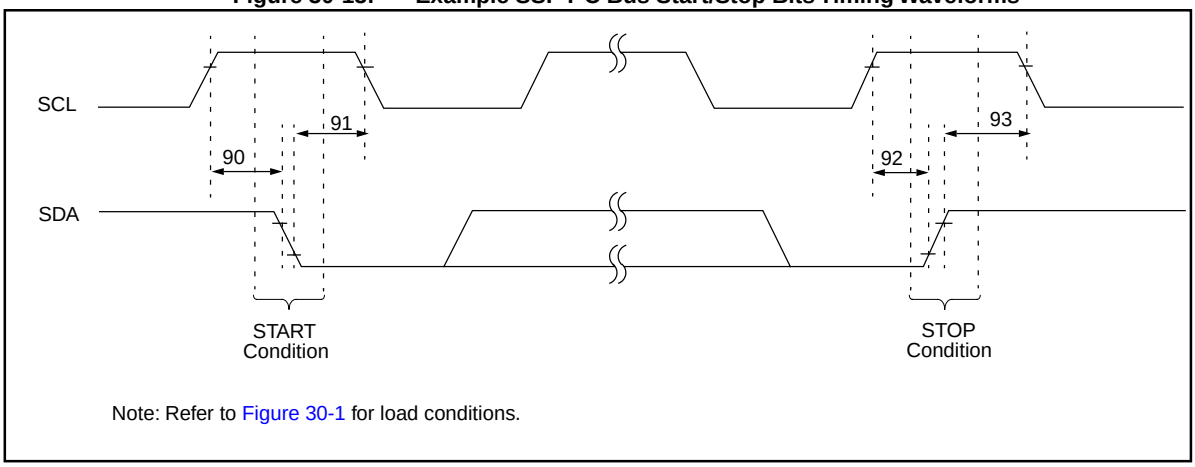
Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input		TCY	—	—	ns	
71	TscH	SCK input high time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	Note 1
72	TscL	SCK input low time (slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	Note 1
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75	TdoR	SDO data output rise time	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX		20	45	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
77	TssH2doZ	$\overline{SS}\uparrow$ to SDO output hi-impedance		10	—	50	ns	
78	TscR	SCK output rise time (master mode)	PIC16**C**XXX	—	10	25	ns	
			PIC16**LC**XXX	—	20	45	ns	
79	TscF	SCK output fall time (master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX	—	—	100	ns	
82	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	PIC16**C**XXX	—	—	50	ns	
			PIC16**LC**XXX	—	—	100	ns	
83	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge		1.5TCY + 40	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

30.20 Example SSP I²C Mode Timing Waveforms and Requirements

Figure 30-13: Example SSP I²C Bus Start/Stop Bits Timing Waveforms

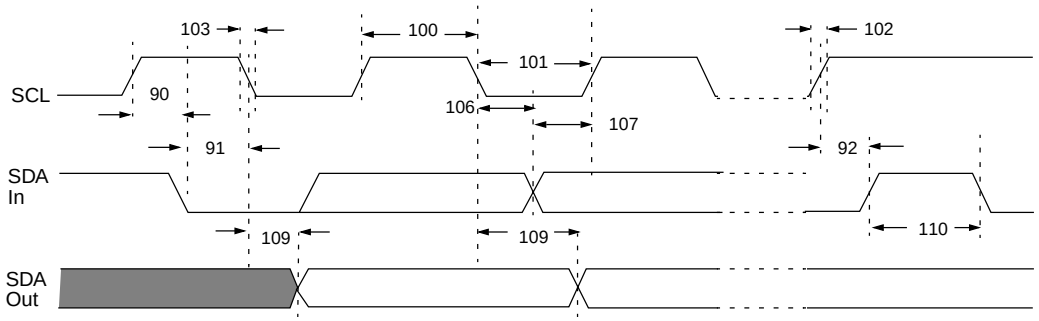


Note: Refer to Figure 30-1 for load conditions.

Table 30-25: Example SSP I²C Bus Start/Stop Bits Requirements

Param. No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	4700	—	—	ns	Only relevant for repeated START condition
		Setup time	400 kHz mode	600	—	—		
91	THD:STA	START condition	100 kHz mode	4000	—	—	ns	After this period the first clock pulse is generated
		Hold time	400 kHz mode	600	—	—		
92	TSU:STO	STOP condition	100 kHz mode	4700	—	—	ns	
		Setup time	400 kHz mode	600	—	—		
93	THD:STO	STOP condition	100 kHz mode	4000	—	—	ns	
		Hold time	400 kHz mode	600	—	—		

Figure 30-14: Example SSP I²C Bus Data Timing Waveforms



Note: Refer to Figure 30-1 for load conditions.

Table 30-26: Example SSP I^2C Bus Data Requirements

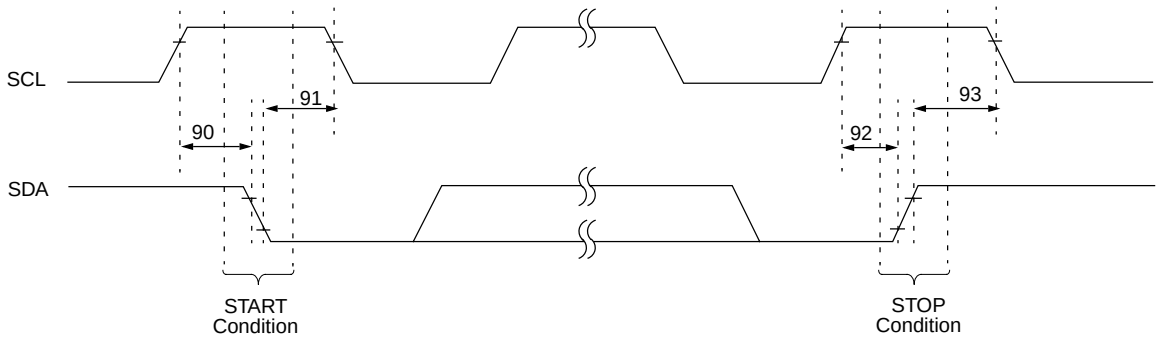
Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	µs	PIC16CXXX must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	PIC16CXXX must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
101	TLOW	Clock low time	100 kHz mode	4.7	—	µs	PIC16CXXX must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	PIC16CXXX must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—		
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition
			400 kHz mode	0.6	—	µs	
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	µs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	Note 1
			400 kHz mode	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
D102	Cb	Bus capacitive loading		—	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement tsu;DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.
TR max. + tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

30.21 Example Master SSP I²C Mode Timing Waveforms and Requirements

Figure 30-15: Example Master SSP I²C Bus Start/Stop Bits Timing Waveforms



Note: Refer to Figure 30-1 for load conditions.

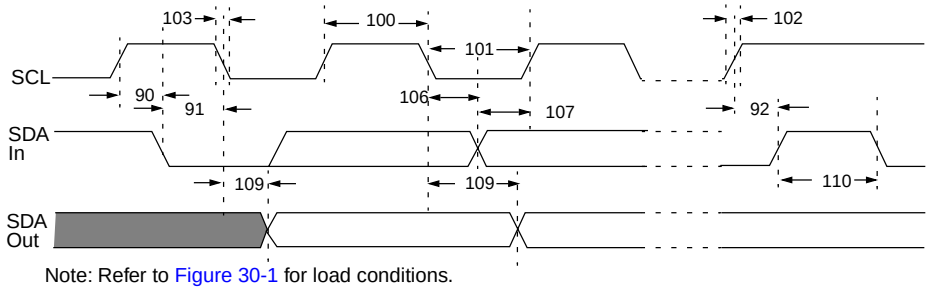
Table 30-27: Example Master SSP I²C Bus Start/Stop Bits Requirements

Param. No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	Only relevant for repeated START condition
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	After this period the first clock pulse is generated
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	2(Tosc)(BRG + 1) §	—	—	ns	
			400 kHz mode	2(Tosc)(BRG + 1) §	—	—		
			1 MHz mode (1)	2(Tosc)(BRG + 1) §	—	—		

§ This specification ensured by design. For the value required by the I²C specification, please refer to Figure A-11 of the **"Appendix."**

Maximum pin capacitance = 10 pF for all I²C pins.

Figure 30-16: Example Master SSP I²C Bus Data Timing



Note: Refer to Figure 30-1 for load conditions.

Table 30-28: Example Master SSP I²C Bus Data Requirements

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			400 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	ms	
101	TLOW	Clock low time	100 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			400 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	ms	
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
			1 MHz mode (1)	—	300	ns	
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1Cb	300	ns	
			1 MHz mode (1)	—	100	ns	
90	TSU:STA	START condition setup time	100 kHz mode	2(TOSC)(BRG + 1) §	—	ms	Only relevant for repeated START condition
			400 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	ms	
91	THD:STA	START condition hold time	100 kHz mode	2(TOSC)(BRG + 1) §	—	ms	After this period the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	ms	
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	ms	
			1 MHz mode (1)	TBD	—	ns	
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
			1 MHz mode (1)	TBD	—	ns	
92	TSU:STO	STOP condition setup time	100 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			400 kHz mode	2(TOSC)(BRG + 1) §	—	ms	
			1 MHz mode (1)	2(TOSC)(BRG + 1) §	—	ms	
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode (1)	—	—	ns	
110	TBUF	Bus free time	100 kHz mode	4.7 ‡	—	ms	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3 ‡	—	ms	
			1 MHz mode (1)	TBD	—	ms	
D102 ‡	Cb	Bus capacitive loading		—	400	pF	

§ This specification ensured by design. For the value required by the I²C specification, please refer to Figure A-11 of the **"Appendix."**

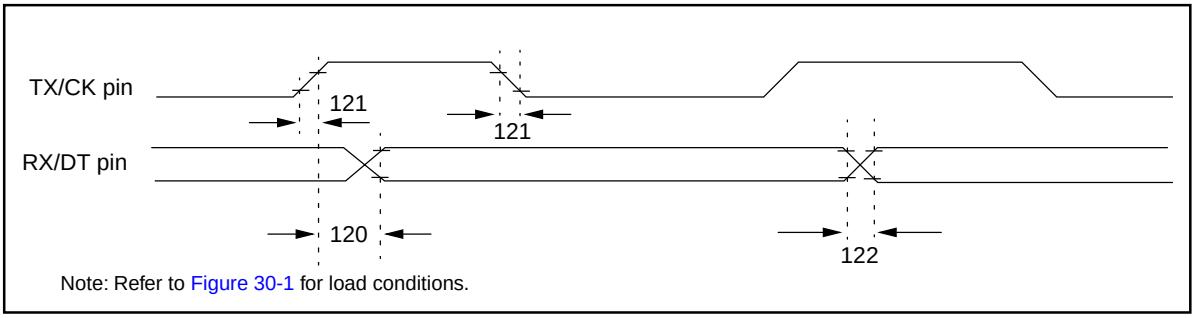
‡ These parameters are for design guidance only and are not tested, nor characterized.

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

2: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but parameter 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line. Parameter 102.+ parameter 107 = 1000 + 250 = 1250 ns (for 100 kHz-mode) before the SCL line is released.

30.22 Example USART/SCI Timing Waveforms and Requirements

Figure 30-17: Example USART Synchronous Transmission (Master/Slave) Timing Waveforms



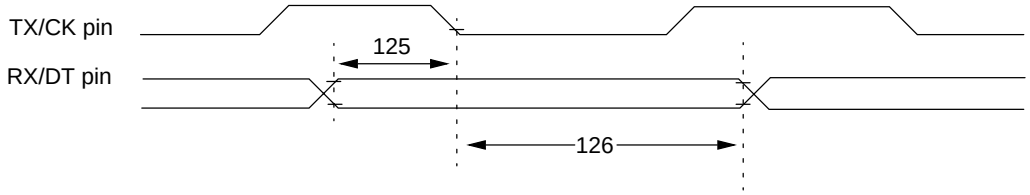
Note: Refer to Figure 30-1 for load conditions.

Table 30-29: Example USART Synchronous Transmission Requirements

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC16**C**XXX	—	—	80	ns	
			PIC16**LC**XXX	—	—	100	ns	
121	Tckrf	Clock out rise time and fall time (Master Mode)	PIC16**C**XXX	—	—	45	ns	
			PIC16**LC**XXX	—	—	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC16**C**XXX	—	—	45	ns	
			PIC16**LC**XXX	—	—	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Figure 30-18: Example USART Synchronous Receive (Master/Slave) Timing Waveforms



Note: Refer to Figure 30-1 for load conditions.

Table 30-2: Example USART Synchronous Receive Requirements

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckl	SYNC RCV (MASTER & SLAVE) Data hold before CK ↓ (DT hold time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

30.23 Example 8-bit A/D Timing Waveforms and Requirements

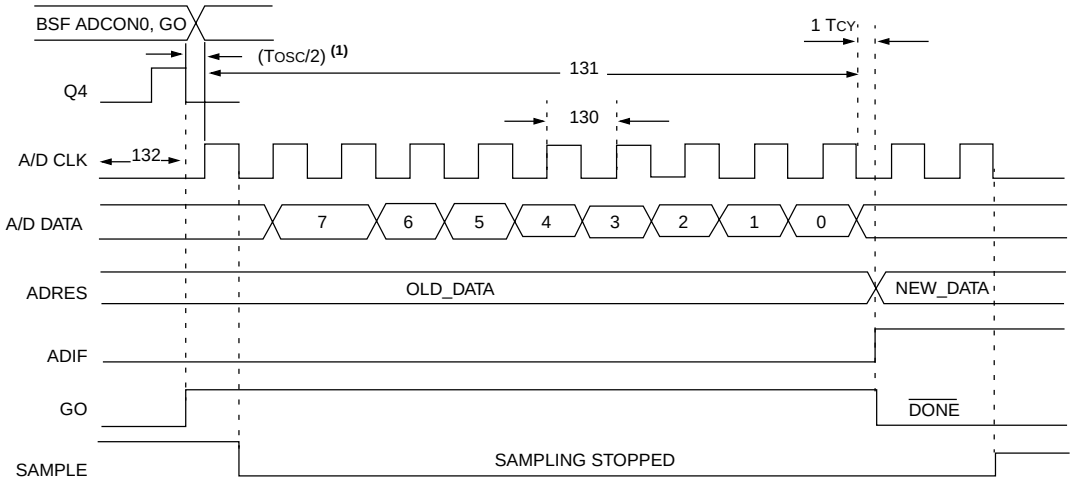
Table 30-30: Example 8-bit A/D Converter Characteristics

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
A01	NR	Resolution		—	—	8-bits	bit	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A02	EABS	Total Absolute error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A03	EIL	Integral linearity error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A04	EDL	Differential linearity error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A05	EFS	Full scale error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A06	EOFF	Offset error		—	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity		—	guaran-teed	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage		3.0V	—	VDD + 0.3	V	
A25	VAIN	Analog input voltage		VSS - 0.3	—	VREF + 0.3	V	
A30	ZAIN	Recommended impedance of analog voltage source		—	—	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	PIC16**C**XXX	—	180	—	µA	Average current consumption when A/D is on**(Note 1)**
			PIC16**LC**XXX	—	90	—	µA	
A50	IREF	VREF input current (Note 2)		10	—	1000	µA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD See the **"8-bit A/D Converter"** section
				—	—	10	µA	During A/D Conversion cycle

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module. VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

Figure 30-19: Example 8-bit A/D Conversion Timing Waveforms



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

Table 30-31: Example 8-bit A/D Conversion Requirements

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16**C**XXX	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16**LC**XXX	2.0	—	—	µs	TOSC based, VREF full range
			PIC16**C**XXX	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16**LC**XXX	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		11	—	11	TAD	
132	TACQ	Acquisition time		Note 2 5	20 —	— —	µs µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D clock start		—	2TOSC §	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
136	TAMP	Amplifier settling time (Note 2)		1	—	—	µs	This may be used if the "new" input voltage has not changed by more than 1LSb (i.e. 5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
135	TSWC	Switching Time from convert → sample		1 §	—	1 §	TAD	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle. See the **"8-bit A/D Converter"** section for minimum requirements.

30.24 Example 10-bit A/D Timing Waveforms and Requirements

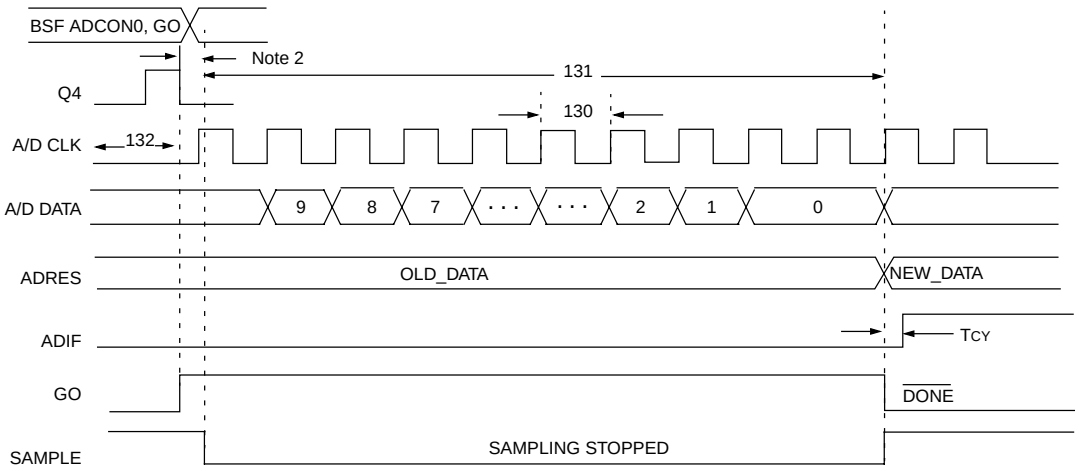
Table 30-32: Example 10-bit A/D Converter Characteristics

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
A01	NR	Resolution		—	—	10	bit	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A02	EABS	Absolute error		—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A03	EIL	Integral linearity error		—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A04	EDL	Differential linearity error		—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A05	EFS	Full scale error		—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A06	EOFF	Offset error		—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity		—	guaran-teed	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage (VREFH - VREFL)		0V	—	—	V	For no latch-up
A20A				3V	—	—	V	For 10-bit resolution
A21	VREFH	Reference voltage High		AVSS	—	AVDD + 0.3V	V	
A22	VREFL	Reference voltage Low		AVSS - 0.3V	—	AVDD	V	
A25	VAIN	Analog input voltage		AVSS - 0.3V	—	VREF + 0.3V	V	
A30	ZAIN	Recommended impedance of analog voltage source		—	—	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	PIC16**C**XXX	—	180	—	µA	Average current consumption when A/D is on. (Note 1)
			PIC16**LC**XXX	—	90	—	µA	
A50	IREF	VREF input current (Note 2)		10	—	1000	µA	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see the **"10-bit A/D Converter"** section.
				—	—	10	µA	During A/D conversion cycle

† Data in "Typ" column is at 5V, 25∞C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.
VREF current is from RG0 and RG1 pins or AVDD and AVSS pins, whichever is selected as reference input.

Figure 30-20: Example 10-bit A/D Conversion Timing Waveforms



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
2: This is a minimal RC delay (typically 100 nS), which also disconnects the holding capacitor from the analog input.

Table 30-33: Example 10-bit A/D Conversion Requirements

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16**C**XXX	1.6	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16**LC**XXX	3.0	—	—	µs	TOSC based, VREF full range
			PIC16**C**XXX	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16**LC**XXX	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including acquisition time) (Note 1)		11 §	—	12 §	TAD	
132	TACQ	Acquisition time (Note 3)		15 10	— —	— —	µs µs	-40°C ≤ Temp ≤ 125°C 0°C ≤ Temp ≤ 125°C
136	TAMP	Amplifier settling time (Note 2)		1	—	—	µs	This may be used if the "new" input voltage has not changed by more than 1LSb (i.e. 5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
135	TSWC	Switching Time from convert → sample		—	—	Note 4		

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
§ This specification ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.
2: See the **"10-bit A/D Converter"** section for minimum conditions when input voltage has changed more than 1 LSb.
3: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (AVDD to AVSS, or AVSS to AVDD). The source impedance (*RS*) on the input channels is 50 Ω.
4: On the next Q4 cycle of the device clock

30.25 Example Slope A/D Timing Waveforms and Requirements

Figure 30-21: Example Slope A/D Conversion Cycle

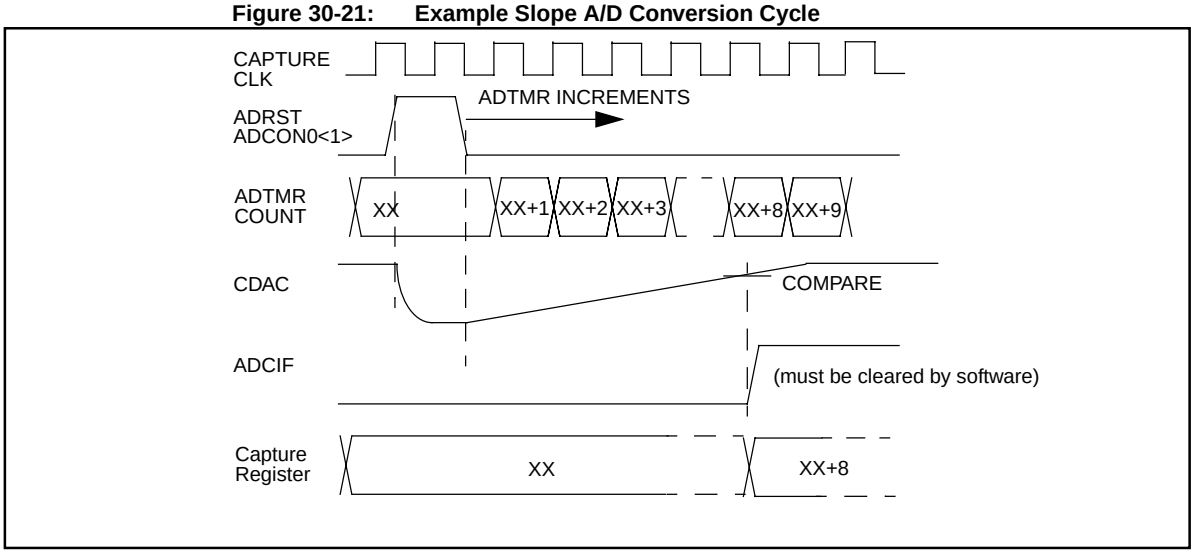


Table 30-34: Example Slope A/D Component Characteristics

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial, -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 30-3.				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
		Slope A/D Comparator					
A100	VAIN	Analog Input Voltage Range	VSS	—	VDD –1.4	V	
A101		Input Offset Voltage	–10	2	10	mV	Measured over common-mode range
A102	GDV	Differential Voltage Gain (Note 1)	—	100	—	dB	
A103	CMRR	Common Mode Rejection Ratio (Note 1)	—	80	—	dB	VDD = 5V, TA = 25°C, over common-mode range
A104	RRadc	Power Supply Rejection Ratio (Note 1)	—	70	—	dB	TA = 25°C, VDDmin ≤ VDD ≤ VDDmax
	TSET	**Turn-on Settling Time**					
140		Band Gap Reference (to < 0.1% (Note 1)	—	1	10	ms	REFOFF bit in SLPCON register 1 → 0
141		Programmable Current Source (to < 0.1%)	—	1	10	ms	Bias generator (reference) turn-on time (REFOFF 1 → 0) (reference start-up) (Note 1)
141A			—	1	10	µs	REFOFF = 0 (constant), ADCON1<7:4> 0000b → 1111b (reference already on and stable) (Note 3)
	TC	**Temperature Coefficient (Note 1)**					
A110	TCBGR	Band Gap Reference	— —	+50 –50	— —	ppm/°C	–40°C ≤ TA ≤ +25°C 25°C ≤ TA ≤ +85°C
A110A			— —	+20 –20	— —	ppm/°C	0°C ≤ TA ≤ +25°C 25°C ≤ TA ≤ +70°C
A111	TCPCS	Programmable Current Source	— —	+0.1 –0.1	— —	%/°C	–40°C ≤ TA ≤ +25°C 25°C ≤ TA ≤ +85°C
A112	TCkref	Slope Reference Divider	—	20	—	ppm/°C	–40°C ≤ TA ≤ +85°C
	CA	**Calibration Accuracy (Note3, 5)**					All parameters calibrated at VDD = 5V and TA = +25°C
A120	CABGR	Band Gap Reference	—	0.01	—	%	
A121	CASRV	Slope Reference Divider	—	0.02	—	%	
	SN	**Supply Sensitivity (Note 1)**					
A130	SNBGR	Band Gap Reference	—	0.04	—	%/V	From VDDmin to VDDmax
A131	SNPCS	Programmable Current Source	—	0.2	—	%/V	From VDDmin to VDDmax
A132	SNkref	Slope Reference Divider	—		—	%/V	From VDDmin to VDDmax
		Programmable Current Source					
A140	IRES	Resolution	1.25	2.25	3.25	µA	1 LSb
A141	EIL	Relative accuracy (linearity error)	–1/2		+1/2	LSb	CDAC = 0V

30.26 Example LCD Timing Waveforms and Requirements

Figure 30-22: Example LCD Voltage Waveform

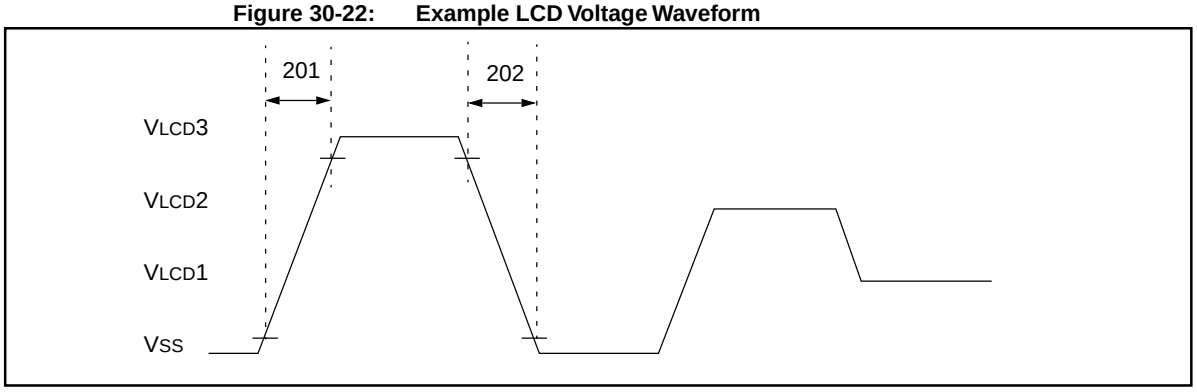


Table 30-35: Example LCD Module Timing Requirements

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
200	FLCDRC	LCDRC Oscillator Frequency	—	14	22	kHz	VDD = 5V, -40˚C to +85˚C
201	TrLCD	Output Rise Time	—	—	200	µs	COM outputs Cload = 5,000 pF SEG outputs Cload = 500 pF VDD = 5.0V, T = 25°C
202	TfLCD	Output Fall Time (Note 1)	TrLCD - 0.05TrLCD	—	TrLCD + 0.05TrLCD	µs	COM outputs Cload = 5,000 pF SEG outputs Cload = 500 pF VDD = 5.0V, T = 25°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: 0Ω source impedance at VLCD.

30.27 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the Electrical Specifications are:

Title	Application Note #
No related Application Notes	

30.28 Revision History

Revision A

This is the initial released revision of the Electrical Specifications description.