Section 25. LCD

HIGHLIGHTS

This section of the manual contains the following major topics:

25.1 Introduction

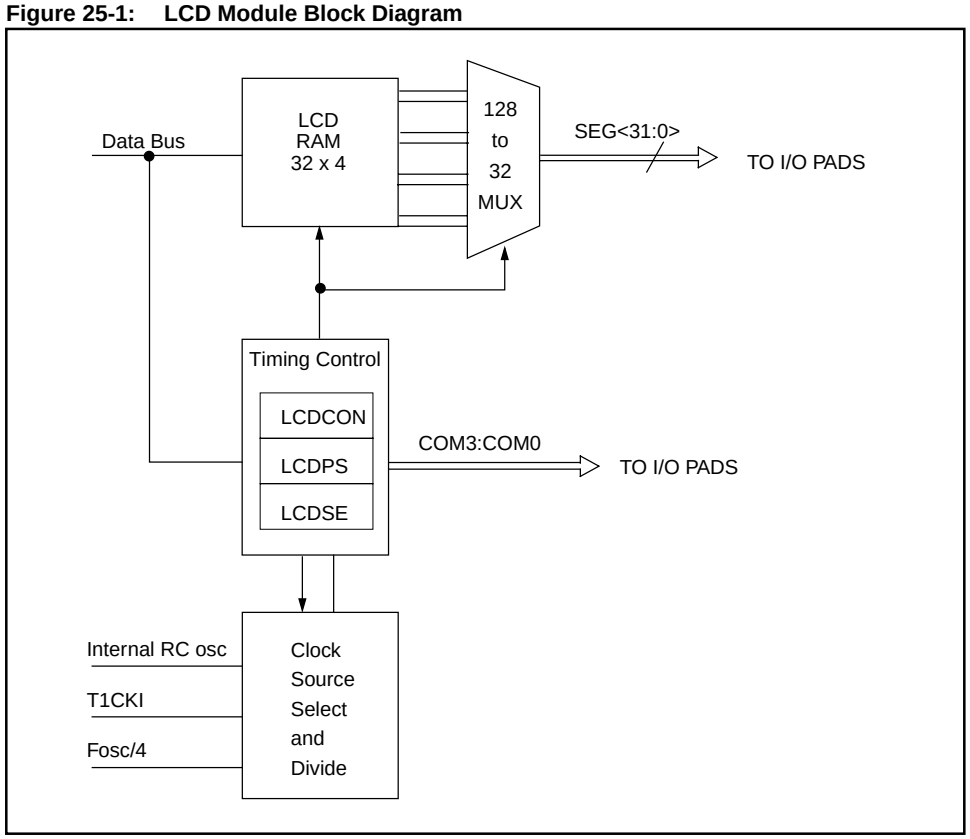
The LCD module generates the timing control to drive a static or multiplexed LCD panel, with support for up to 32 segments multiplexed with up to four commons. It also provides control of the LCD pixel data.

The interface to the module consists of three control registers (LCDCON, LCDSE, and LCDPS) used to define the timing requirements of the LCD panel and up to 16 LCD data registers (LCD00-LCD15) that represent the array of the pixel data. In normal operation, the control registers are configured to match the LCD panel being used. Primarily, the initialization information consists of selecting the number of commons and segments required by the LCD panel, and then specifying the LCD Frame clock rate to be used by the panel.

Once the module is initialized for the LCD panel, the individual bits of the LCD data registers are cleared/set to represent a turned-on pixel respectively.

Once the module is configured, the LCDEN bit (LCDCON<7>) is used to enable or disable the LCD module. The LCD panel can also operate during sleep by clearing the SLPEN bit (LCDCON<6>).

Figure 25-1: LCD Module Block Diagram



25.2 Control Register

Register 25-1: LCDCON Register

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDEN	SLPEN	—	VGEN	CS1	CS0	LMUX1	LMUX0
bit 7							bit 0

bit 7 **LCDEN**: Module Drive Enable bit
1 = LCD drive enabled
0 = LCD drive disabled

bit 6 **SLPEN**: LCD Display Sleep Enable bit
1 = LCD module will stop operating during SLEEP
0 = LCD module will continue to display during SLEEP

bit 5 **Unimplemented**: Read as '0'

bit 4 **VGEN**: Voltage Generator Enable bit
1 = Internal LCD Voltage Generator Enabled, (powered-up)
0 = Internal LCD Voltage Generator powered-down, voltage is expected to be provided externally

bit 3:2 **CS1:CS0**: Clock Source Select bits
00 = Fosc/256
01 = T1CKI (Timer1)
1x = Internal RC oscillator

bit 1:0 **LMUX1:LMUX0**: Common Selection bits
Specifies the number of commons and the bias method

LMUX1:LMUX0	MULTIPLEX		BIAS	Max # of Segments
00	Static	(COM0)	Static	32
01	1/2	(COM0, 1)	1/3	31
10	1/3	(COM0, 1, 2)	1/3	30
11	1/4	(COM0, 1, 2, 3)	1/3	29

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Register 25-2: LCDPS Register

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	LP3	LP2	LP1	LP0
bit 7							bit 0

bit 7:4 **Unimplemented,** read as '0'

bit 3:0 **LP3:LP0**: Frame Clock Prescale Selection bits

LMUX1:LMUX0	Multiplex	Frame Frequency =
00	Static	Clock source / (128 * (LP3:LP0 + 1))
01	1/2	Clock source / (128 * (LP3:LP0 + 1))
10	1/3	Clock source / (96 * (LP3:LP0 + 1))
11	1/4	Clock source / (128 * (LP3:LP0 + 1))

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Register 25-3: Generic LCDD (Pixel Data) Register Layout

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc	SEGs COMc
bit 7							bit 0

bit 7:0 **SEGsCOMc**: Pixel Data bit for segment s and common c

1 = Pixel on (dark)
0 = Pixel off (clear)

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Register 25-4: LCDSE Register

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
SE29	SE27	SE20	SE16	SE12	SE9	SE5	SE0
bit 7							bit 0

bit 7 **SE29**: Pin Function Select bits for COM1/SEG31 - COM3/SEG29
1 = pins have LCD segment driver function
0 = pins have digital Input function

Note: The LMUX1:LMUX0 setting takes precedence over the SE29 bit, causing pins to become common drivers.

bit 6 **SE27**: Pin Function Select for SEG28 and SEG27
1 = pins have LCD segment driver function
0 = pins have digital Input function

bit 5 **SE20**: Pin Function Select bits for SEG26 - SEG20
1 = pins have LCD segment driver function
0 = pins have digital Input function

bit 4 **SE16**: Pin Function Select bits for SEG19 - SEG16
1 = pins have LCD segment driver function
0 = pins have digital Input function

bit 3 **SE12**: Pin Function Select bits for SEG15 - SEG12
1 = pins have LCD segment driver function
0 = pins have digital Input function

bit 2 **SE9**: Pin Function Select bits for SEG11 - SEG09
1 = pins have LCD segment driver function
0 = pins have digital Input function

bit 1 **SE5**: Pin Function Select bits for SEG08 - SEG05
1 = pins have LCD segment driver function
0 = pins have digital Input function

bit 0 **SE0**: Pin Function Select bits for SEG04 - SEG00
1 = pins have LCD segment driver function
0 = pins have digital I/O function

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Note: On a Power-on Reset, the LCD pins are configured for LCD drive function.

25.3 LCD Timing

The LCD module has 3 possible clock source inputs and supports static, 1/2, 1/3, and 1/4 multiplexing.

25.3.1 Timing Clock Source Selection

The clock sources for the LCD timing generation are:

- Internal RC oscillator — used for device low frequency or sleep operation
- Timer1 oscillator — used for device low frequency or sleep operation
- System clock divided by 256

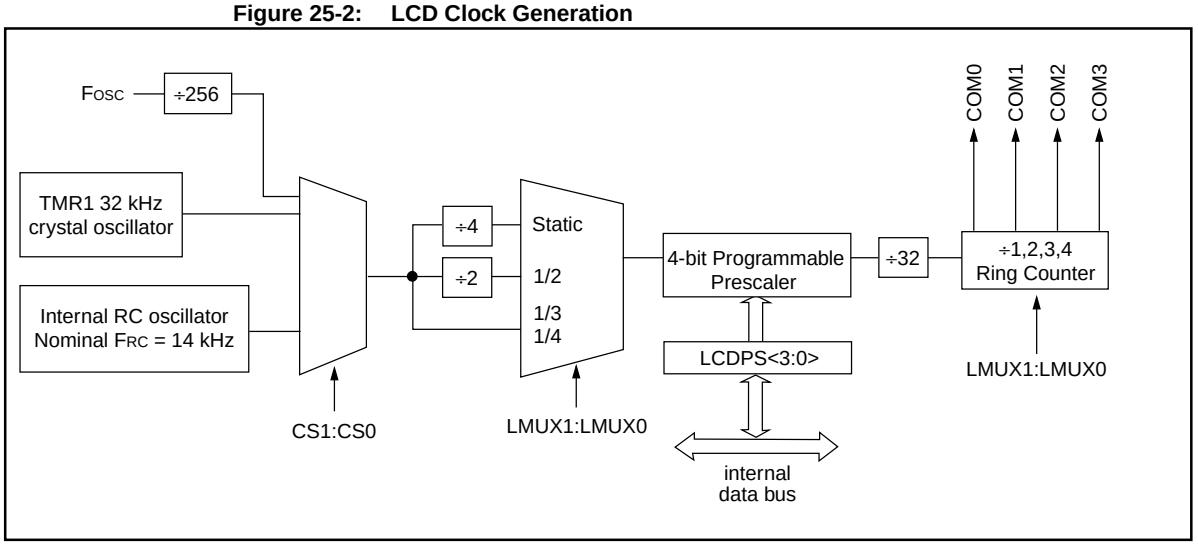
The first timing source is an internal RC oscillator which runs at a nominal frequency of 14 kHz. This oscillator provides a lower speed clock which may be used to continue running the LCD while the processor is in sleep. The RC oscillator will power-down when it is not selected or when the LCD module is disabled.

The second source is the Timer1 external oscillator. This oscillator provides a lower speed clock which may be used to continue running the LCD while the processor is in sleep. It is assumed that the frequency provided on this oscillator will be 32 kHz. To use the Timer1 oscillator as a LCD module clock source, it is only necessary to set the T1OSCEN (T1CON<3>) bit.

The third source is the system clock divided by 256. This divider ratio is chosen to provide about 32 kHz output when the external oscillator is 8 MHz. The divider is not programmable. Instead the LCDPS register is used to set the LCD frame clock rate.

The clock sources are selected with bits CS1:CS0 (LCDCON<3:2>). Refer to Figure 25-1 for details of the register programming.

Figure 25-2: LCD Clock Generation



25.3.2 Multiplex Timing Generation

The timing generation circuitry will generate 1 to 4 common's based on the display mode selected. The mode is specified by bits LMUX1:LMUX0 (LCDCON<1:0>). Table 25-1 shows the formulas for calculating the frame frequency.

Table 25-1: Frame Frequency Formulas

Multiplex	Frame Frequency =
Static	Clock source / (128 * (LP3:LP0 + 1))
1/2	Clock source / (128 * (LP3:LP0 + 1))
1/3	Clock source / (96 * (LP3:LP0 + 1))
1/4	Clock source / (128 * (LP3:LP0 + 1))

Table 25-2: Approximate Frame Frequency in Hz using Timer1 @ 32.768 kHz or Fosc @ 8 MHz

LP3:LP0	Static	1/2	1/3	1/4
2	85	85	114	85
3	64	64	85	64
4	51	51	68	51
5	43	43	57	43
6	37	37	49	37
7	32	32	43	32

Table 25-3: Approximate Frame Frequency in Hz using internal RC osc @ 14 kHz

LP3:LP0	Static	1/2	1/3	1/4
0	109	109	146	109
1	55	55	73	55
2	36	36	49	36
3	27	27	36	27

Figure 25-3: STATIC Waveforms

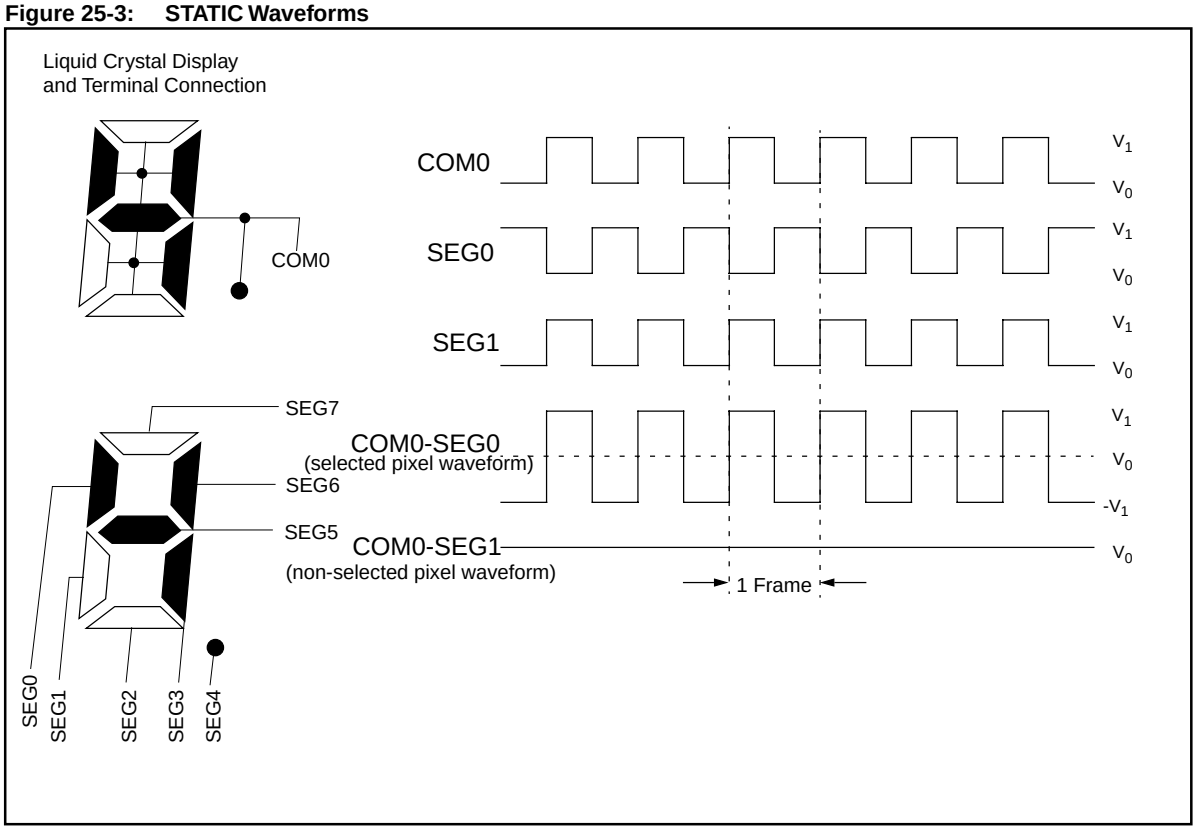


Figure 25-4: 1/2 MUX, 1/3 BIAS Waveform

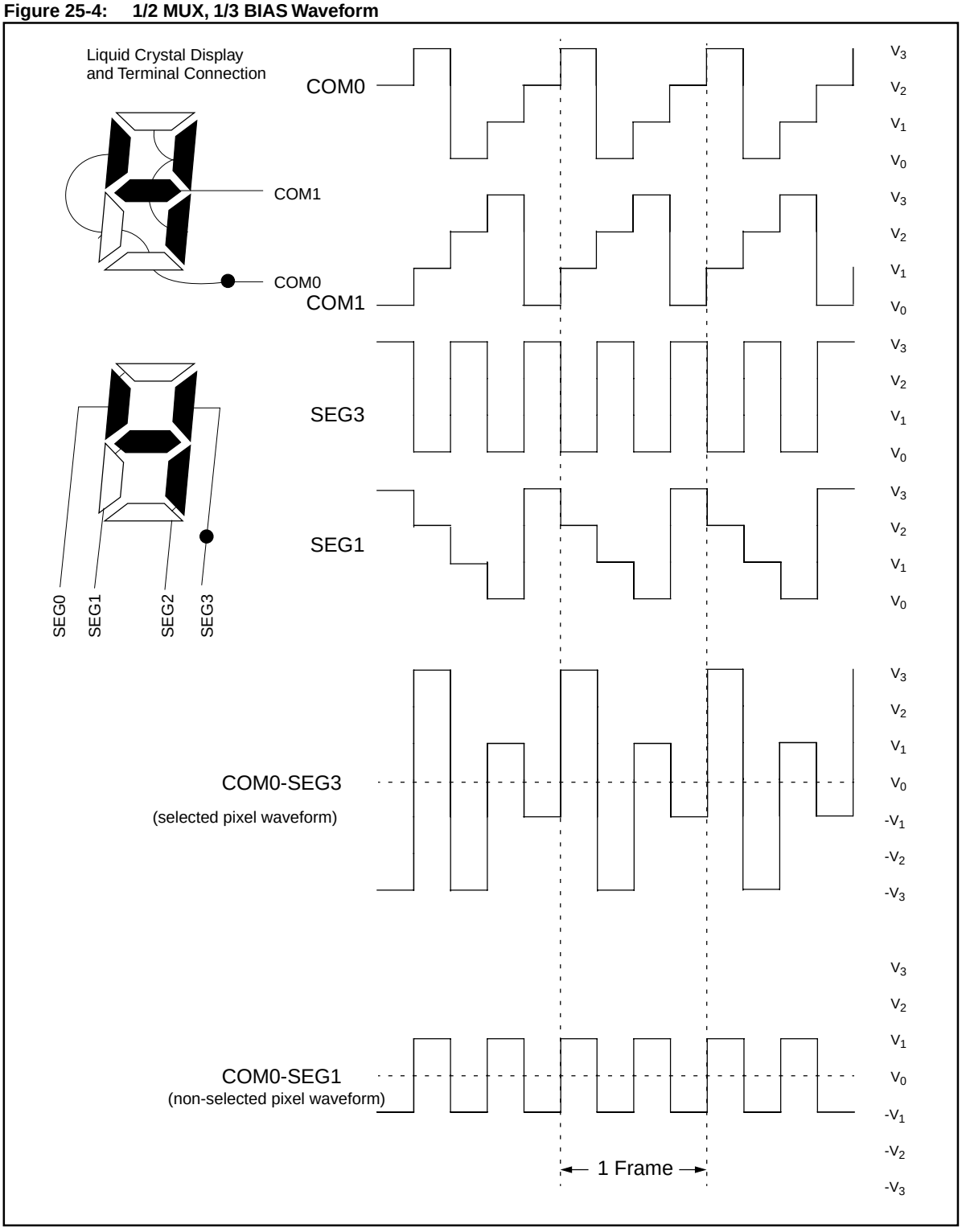


Figure 25-5: 1/3 MUX, 1/3 BIAS Waveform

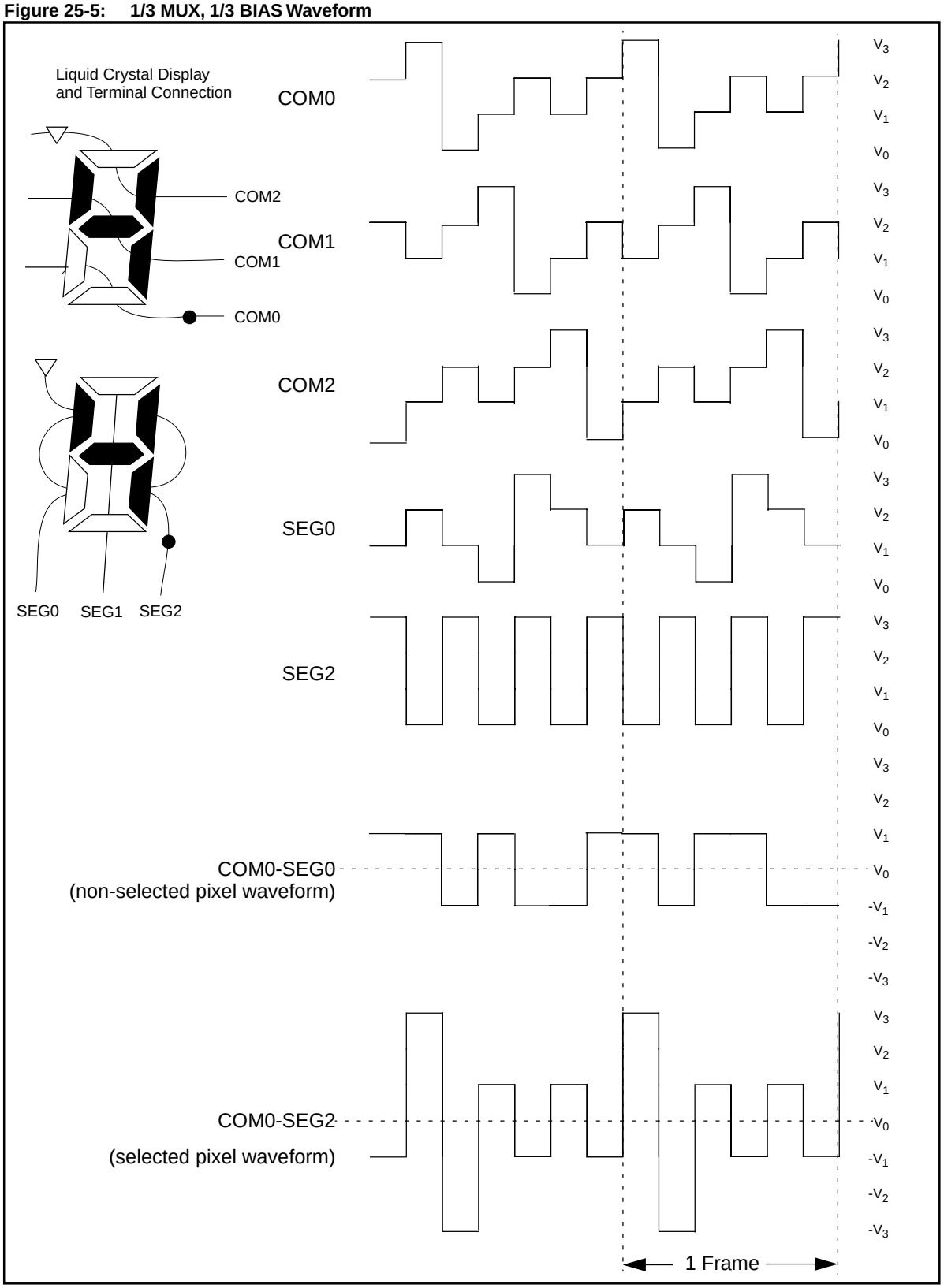
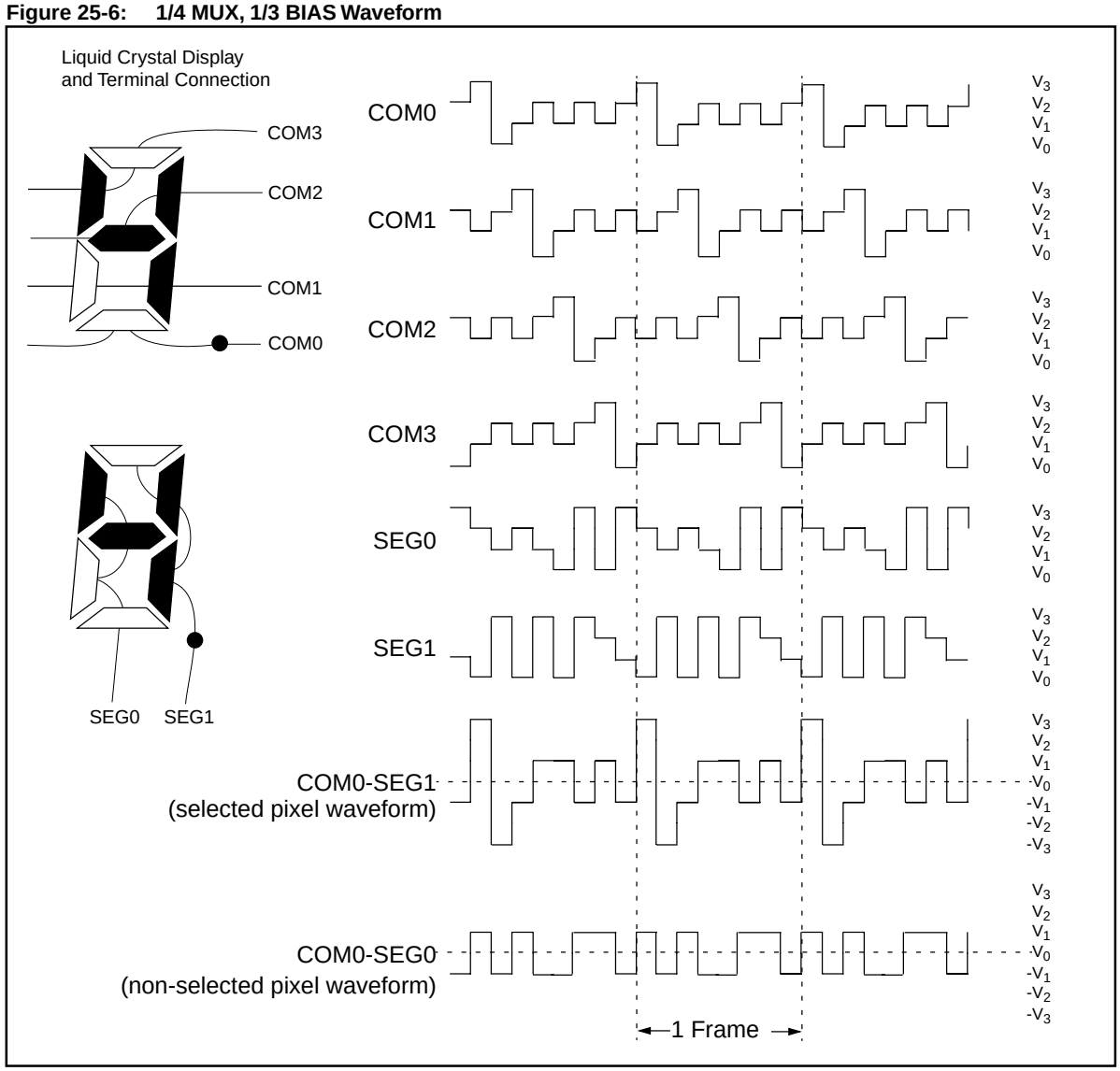


Figure 25-6: 1/4 MUX, 1/3 BIAS Waveform

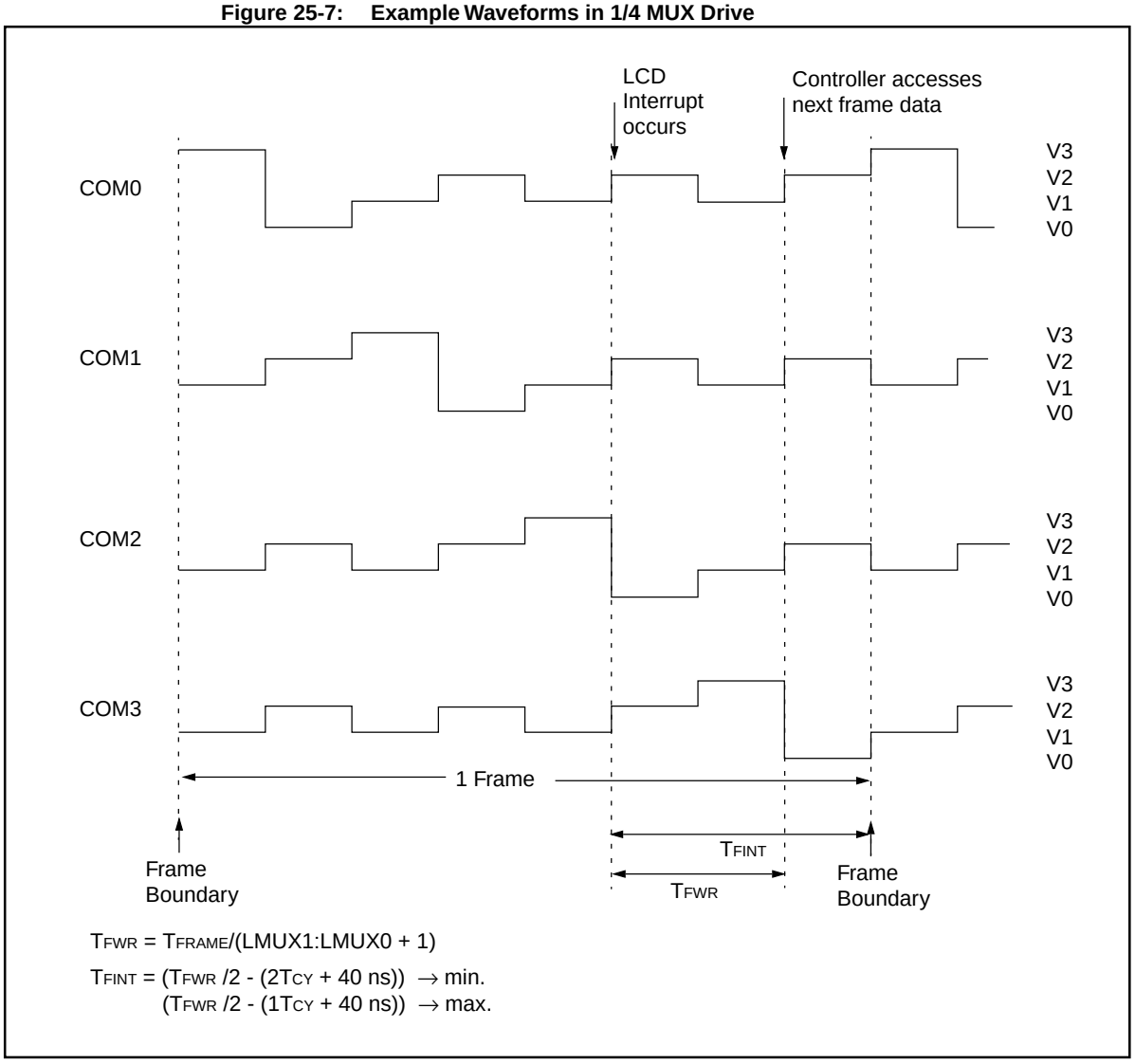


25.4 LCD Interrupts

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame. Writing pixel data at the frame boundary allows a visually crisp transition of the image. This interrupt can also be used to synchronize external events to the LCD. For example, the interface to an external segment driver, such as a Microchip AY0438, can be synchronized for segment data update to the LCD frame.

A new frame is defined to begin at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a certain fixed time before the frame boundary as shown in Figure 25-7. The LCD controller will begin to access data for the next frame within T_{FWR} after the interrupt.

Figure 25-7: Example Waveforms in 1/4 MUX Drive



$T_{FWR} = T_{FRAME}/(LMUX1:LMUX0 + 1)$

$T_{FINT} = (T_{FWR}/2 - (2T_{CY} + 40\ ns)) \rightarrow min.$

$(T_{FWR}/2 - (1T_{CY} + 40\ ns)) \rightarrow max.$

25.5 Pixel Control

25.5.1 LCDD (Pixel Data) Registers

The pixel registers contain bits which define the state of each pixel. Each bit defines one unique pixel.

Table 25-4 shows the correlation of each bit in the LCDD registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

Table 25-4: LCDD Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
LCDD00	SEG07 COM0	SEG06 COM0	SEG05 COM0	SEG04 COM0	SEG03 COM0	SEG02 COM0	SEG01 COM0	SEG00 COM0	xxxx xxxx	xxxx xxxx
LCDD01	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG09 COM0	SEG08 COM0	xxxx xxxx	xxxx xxxx
LCDD02	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0	xxxx xxxx	xxxx xxxx
LCDD03	SEG31 COM0	SEG30 COM0	SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0	xxxx xxxx	xxxx xxxx
LCDD04	SEG07 COM1	SEG06 COM1	SEG05 COM1	SEG04 COM1	SEG03 COM1	SEG02 COM1	SEG01 COM1	SEG00 COM1	xxxx xxxx	xxxx xxxx
LCDD05	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG09 COM1	SEG08 COM1	xxxx xxxx	xxxx xxxx
LCDD06	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1	xxxx xxxx	xxxx xxxx
LCDD07	SEG31 COM**1** (1)	SEG30 COM1	SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1	xxxx xxxx	xxxx xxxx
LCDD08	SEG07 COM2	SEG06 COM2	SEG05 COM2	SEG04 COM2	SEG03 COM2	SEG02 COM2	SEG01 COM2	SEG00 COM2	xxxx xxxx	xxxx xxxx
LCDD09	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG09 COM2	SEG08 COM2	xxxx xxxx	xxxx xxxx
LCDD10	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	xxxx xxxx	xxxx xxxx
LCDD11	SEG31 COM**2** (1)	SEG30 COM**2** (1)	SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2	xxxx xxxx	xxxx xxxx
LCDD12	SEG07 COM3	SEG06 COM3	SEG05 COM3	SEG04 COM3	SEG03 COM3	SEG02 COM3	SEG01 COM3	SEG00 COM3	xxxx xxxx	xxxx xxxx
LCDD13	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG09 COM3	SEG08 COM3	xxxx xxxx	xxxx xxxx
LCDD14	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	xxxx xxxx	xxxx xxxx
LCDD15	SEG31 COM**3** (1)	SEG30 COM**3** (1)	SEG29 COM**3** (1)	SEG28 COM30	SEG27 COM3	SEG26 COM30	SEG25 COM3	SEG24 COM3	xxxx xxxx	xxxx xxxx

Note 1: These pixels do not display, but can be used as general purpose RAM.

25.5.2 Segment Enables

The LCDSE register is used to select the pin function for groups of pins. The selection allows each group of pins to operate as either LCD drivers or digital only pins. To configure the pins as a digital port, the corresponding bits in the LCDSE register must be cleared.

If the pin is a digital input the corresponding TRIS bit controls the data direction. Any bit set in the LCDSE register overrides any bit settings in the corresponding TRIS register.

Note 1: On a Power-on Reset, the LCD pins are configured as LCD drivers.

Note 2: The LMUX1:LMUX0 bits take precedence over the LCDSE bit settings for pins RD7, RD6 and RD5.

Example 25-1: Static MUX with 32 Segments

```
    BCF   STATUS,RP0   ; Select Bank2
    BSF   STATUS,RP1   ;
    BCF   LCDCON,LMUX1 ; Select Static MUX
    BCF   LCDCON,LMUX0 ;
    MOVLW 0xFF         ; Make PortD,E,F,G LCD pins
    MOVWF LCDSE        ; configure rest of LCD
```

Example 25-2: 1/3 MUX with 13 Segments

```
    BCF   STATUS,RP0   ; Select Bank2
    BSF   STATUS,RP1   ;
    BSF   LCDCON,LMUX1 ; Select 1/3 MUX
    BCF   LCDCON,LMUX0 ;
    MOVLW 0x87         ; Make PORTD<7:0> & PORTE<6:0> LCD pins
    MOVWF LCDSE        ; configure rest of LCD
```

25.6 Voltage Generation

There are two methods for LCD voltage generation, internal charge pump, or external resistor ladder.

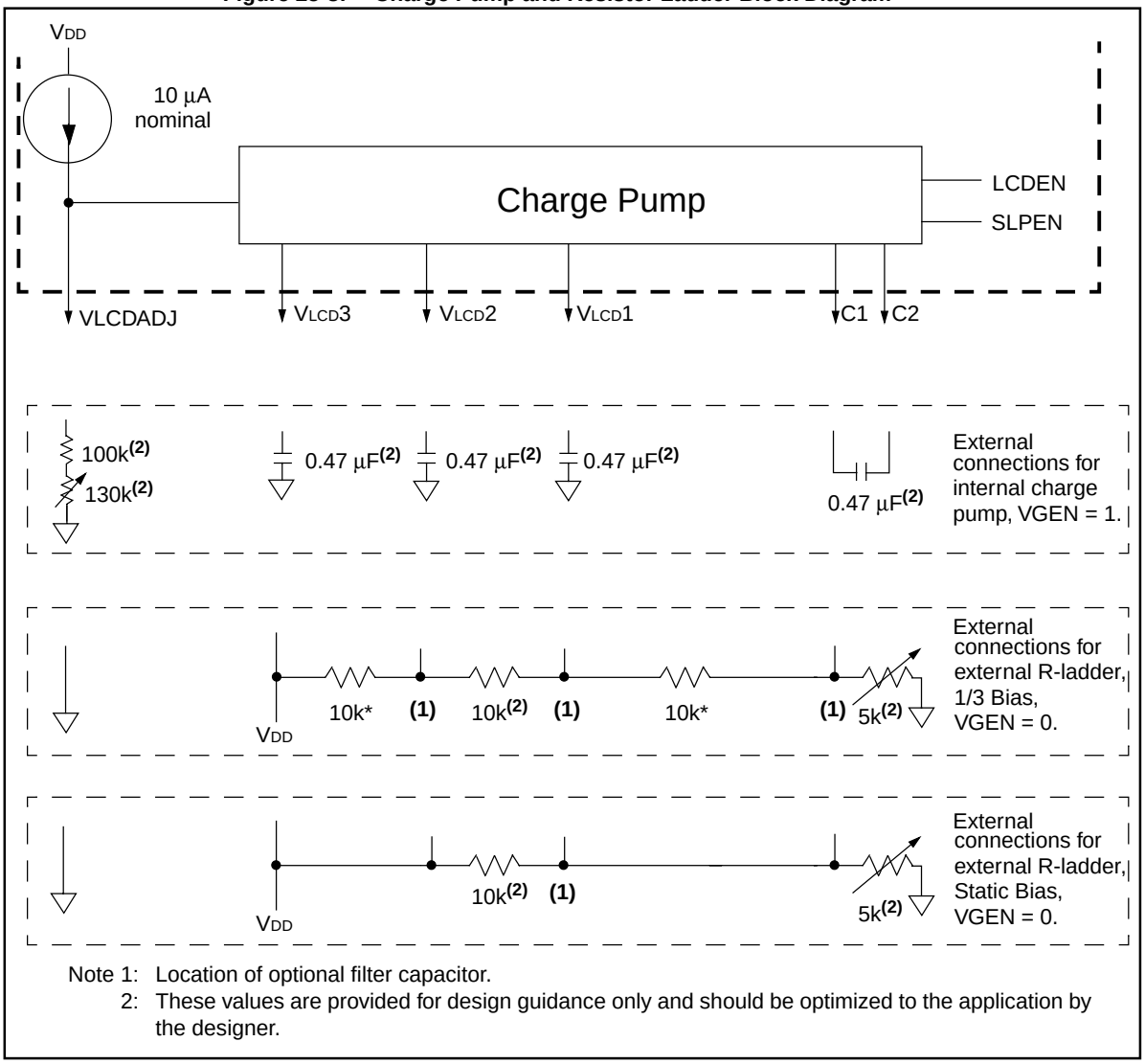
25.6.1 Charge Pump

The LCD charge pump is shown in Figure 25-8. The 1.0V - 2.3V regulator will establish a stable base voltage from the varying battery voltage. This regulator is adjustable through the range by connecting a variable external resistor from VLCDADJ to ground. The potentiometer provides contrast adjustment for the LCD. This base voltage is connected to $V_{LCD}1$ on the charge pump. The charge pump boosts $V_{LCD}1$ into $V_{LCD}2 = 2 * V_{LCD}1$ and $V_{LCD}3 = 3 * V_{LCD}1$. When the charge pump is not operating, $V_{LCD}3$ will be internally tied to V_{DD}. See the Electrical Specifications section for charge pump capacitor and potentiometer values.

25.6.2 External R-Ladder

The LCD module can also use an external resistor ladder (R-Ladder) to generate the LCD voltages. Figure 25-8 shows external connections for static and 1/3 bias. The VGEN (LCDCON<4>) bit must be cleared to use an external R-Ladder.

Figure 25-8: Charge Pump and Resistor Ladder Block Diagram



Note 1: Location of optional filter capacitor.
2: These values are provided for design guidance only and should be optimized to the application by the designer.

25.7 Operation During Sleep

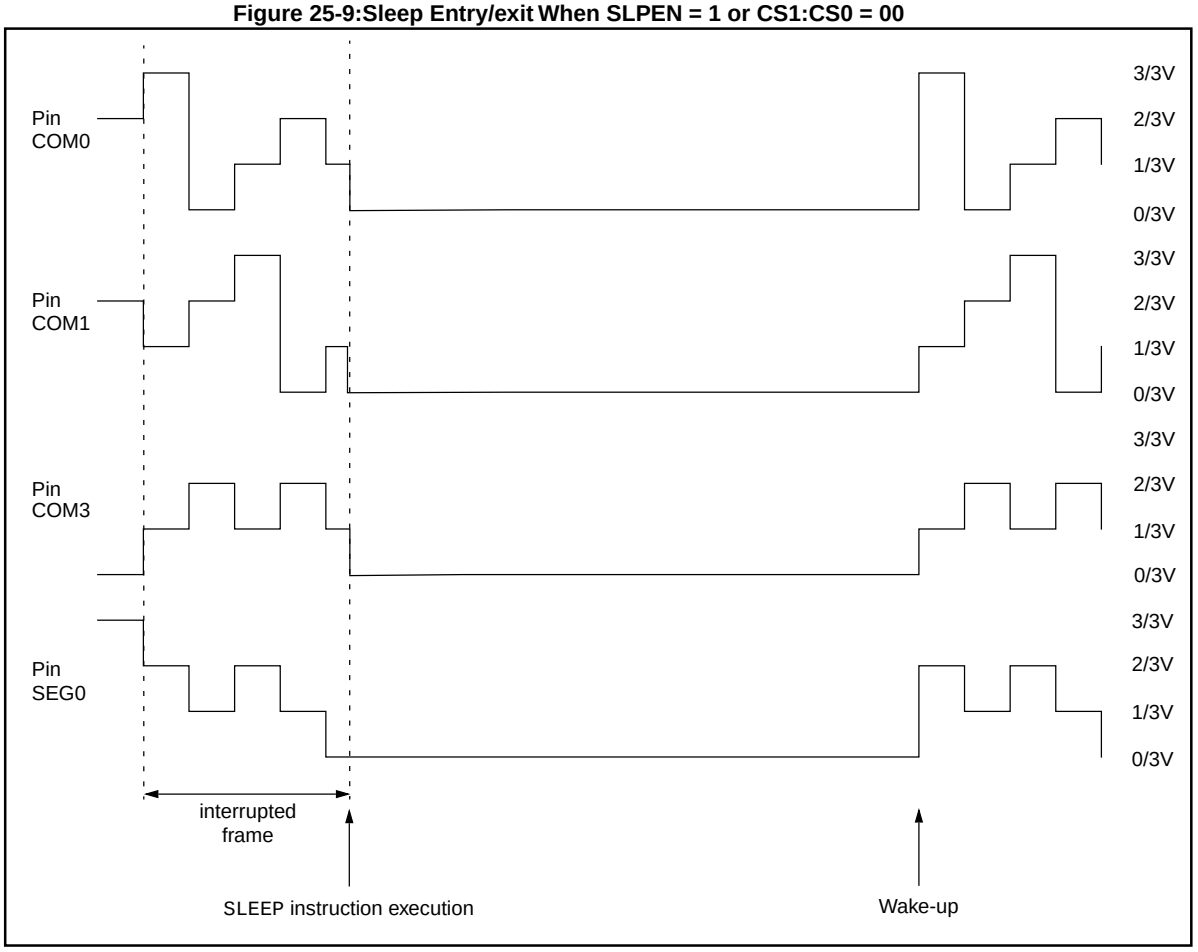
The LCD module can operate during sleep. The selection is controlled by bit SLPEN (LCDCON<6>). Setting the SLPEN bit allows the LCD module to go to sleep. Clearing the SLPEN bit allows the module to continue to operate during sleep.

If a SLEEP instruction is executed and SLPEN = '1', the LCD module will cease all functions and go into a very low current consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 25-9 shows this operation. To ensure that the LCD completes the frame, the SLEEP instruction should be executed immediately after a LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. See **25.4 "LCD Interrupts"** for the formulas to calculate the delay.

If a SLEEP instruction is executed and SLPEN = '0', the module will continue to display the current contents of the LCDD registers. To allow the module to continue operation while in sleep, the clock source must be either the internal RC oscillator or Timer1 external oscillator. While in sleep, the LCD data cannot be changed. The LCD module current consumption will not decrease in this mode, however the overall consumption of the device will be lower due to shutdown of the core and other peripheral functions.

Note:	The internal RC oscillator or external Timer1 oscillator must be used to operate the LCD module during sleep.

Figure 25-9: Sleep Entry/exit When SLPEN = 1 or CS1:CS0 = 00



25.8 Effects of a Reset

The LCD module is disabled, but the LCD pins are configured as LCD drivers. This ensures that the microcontroller does not damage the LCD glass by accidently having a DC voltage across a segment.

25.9 Configuring the LCD Module

The following is the sequence of steps to follow to configure the LCD module.

1. Select the frame clock prescale using the LP3:LP0 bits (LCDPS<3:0>).
2. Configure the appropriate pins to function as segment drivers using the LCDSE register.
3. Configure the LCD module for the following using the LCDCON register.
   - Multiplex mode and Bias, selected by the LMUX1:LMUX0 bits
   - Timing source, selected by the CS1:CS0 bits
   - Voltage generation, enabled by the VGEN bit
   - Sleep mode operation, enabled by the SLPEN bit
4. Write initial values to pixel data registers, LCDD00 through LCDD15.
5. Clear LCD interrupt flag bit, LCDIF, and if desired, enable the interrupt by setting the LCDIE bit.
6. Enable the LCD module, by setting the LCDEN bit (LCDCON<7>).

25.10 Discrimination Ratio

Discrimination ratio is a way to calculate the contrast levels that a panel can achieve. The first example is a static waveform from Figure 25-3. The voltages V_1 and V_0 will be assigned values of 1 and 0. The next step is to construct an equation for one frame to help visualize the DC and RMS voltages present on an individual pixel that is ON and OFF. The rest of the following shows the calculation of the DC, RMS, and Discrimination Ratio.

Example 25-3: Discrimination Ratio Calculation for Static MUX

$$\text{COMx - SEGx [ON]} = 1 - 1, \quad V_{DC} = 0$$

$$\text{COMx - SEGx [OFF]} = 0 + 0, \quad V_{DC} = 0$$

$$V_{RMS}\,[ON] = \Delta V \sqrt{\frac{(1)^2 + (-1)^2}{2}} = 1\Delta V$$

$$V_{RMS}\,[OFF] = \Delta V \sqrt{\frac{(0)^2 + (0)^2}{2}} = 0\Delta V$$

$$D = \frac{V_{RMS}\,[ON]}{V_{RMS}\,[OFF]} = \frac{1\Delta V}{0\Delta V} = \infty$$

See Figure 25-3 for Static waveform.

The next example is for Figure 25-6 which is a 1/4 MUX, 1/3 BIAS waveform. For this example, the values 3, 2, 1 and 0 will be assigned to V_3, V_2, V_1, and V_0 respectively. The frame equation, DC voltage, RMS voltage and discrimination ratio calculations are shown in Example 25-4.

Example 25-4: Discrimination Ratio Calculation 1/4 MUX

COM0 - SEGx [ON] = 3 - 3 + 1 - 1 + 1 - 1 + 1 - 1 $V_{DC} = 0$
COM0 - SEGx [OFF] = 1 - 1 - 1 + 1 - 1 + 1 - 1 + 1 $V_{DC} = 0$

$$V_{RMS}[ON] = \Delta V \sqrt{\frac{(3)^2 + (-3)^2 + (1)^2 + (-1)^2 + (1)^2 + (-1)^2 + (1)^2 + (-1)^2}{8}} = \sqrt{3}\,\Delta V$$

$$V_{RMS}[OFF] = \Delta V \sqrt{\frac{(1)^2 + (-1)^2 + (-1)^2 + (1)^2 + (-1)^2 + (1)^2 + (-1)^2 + (1)^2}{8}} = \Delta V$$

$$D = \frac{V_{RMS}[ON]}{V_{RMS}[OFF]} = \frac{\sqrt{3}\,\Delta V}{1\,\Delta V} = 1.732$$

Note: Refer to Figure 25-6

As shown in these examples, static displays have excellent contrast. The higher the multiplex ratio of the LCD, the lower the discrimination ratio, and therefore, the lower the contrast of the display.

Table 25-5 shows the V_{OFF}, V_{ON} and discrimination ratios of the various combinations of MUX and BIAS.

As the multiplex of the LCD panel increases, the discrimination ratio decreases. The contrast of the panel will also decrease, so to provide better contrast the LCD voltages must be increased to provide greater separation between each level.

Table 25-5: Discrimination Ratio vs. MUX and Bias

	1/3 BIAS		
	V_{OFF}	V_{ON}	D
STATIC	0	1	∞
1/2 MUX	0.333	0.745	2.236
1/3 MUX	0.333	0.638	1.915
1/4 MUX	0.333	0.577	1.732

25.11 LCD Voltage Generation

Among the many ways to generate LCD voltage, two methods stand out above the crowd:

- resistor ladder
- charge pump.

The resistor ladder method, shown in Figure 25-10, is most commonly used for higher VCC voltages. This method uses inexpensive resistors to create the multi-level LCD voltages. Regardless of the number of pixels that are energized the current remains constant. The voltage at point V3 is typically tied to VCC, either internally or externally.

The resistance values are determined by two factors: display quality and power consumption. Display quality is a function of the LCD drive waveforms. Since the LCD panel is a capacitive load, the waveform is distorted due to the charging and discharging currents. This distortion can be reduced by decreasing the value of resistance. However, this change increases the power consumption due to the increased current now flowing through the resistors. As the LCD panel increases in size, the resistance value must be decreased to maintain the image quality of the display.

Sometimes the addition of parallel capacitors to the resistance can reduce the distortion caused by charging/discharging currents. The capacitors act as charge storage to provide current as the display waveform transitions. In general, R is 1 kΩ to 50 kΩ and the potentiometer is 5 kΩ to 200 kΩ.

Figure 25-10: Resistor Ladder

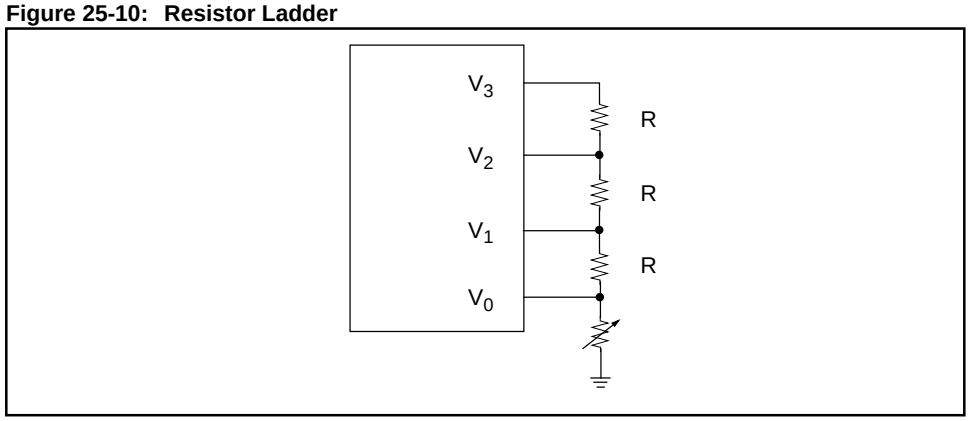
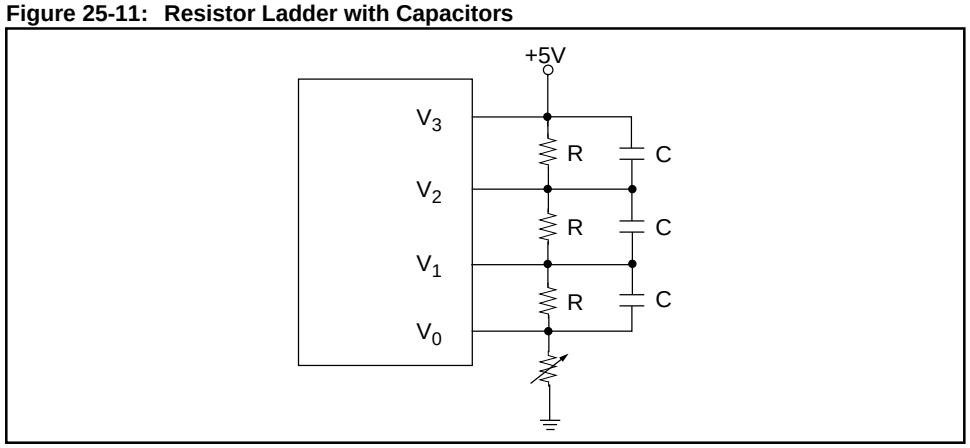
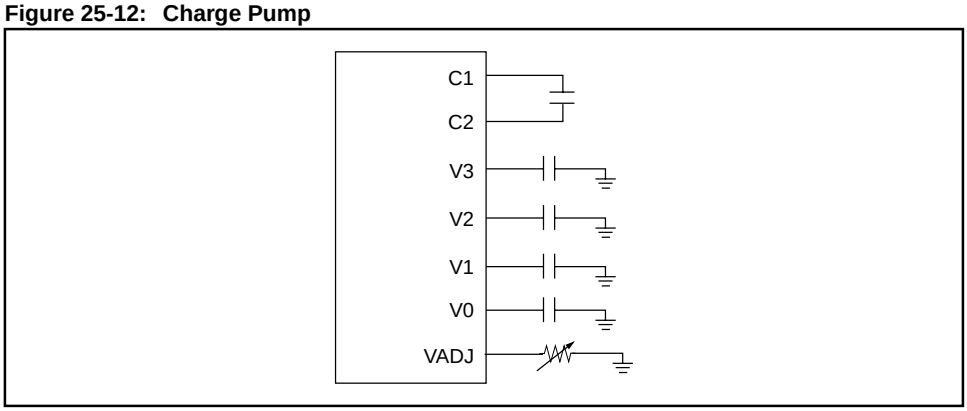


Figure 25-11: Resistor Ladder with Capacitors



A charge pump is ideal for low voltage battery operation because the V_{DD} voltage can be boosted up to drive the LCD panel. The charge pump requires a charging capacitor and filter capacitor for each of the LCD voltages as seen in Figure 25-12. These capacitors are typically low leakage types such as polyester, polypropylene, or polystyrene material. Another feature that makes the charge pump ideal for battery applications is that the current consumption is proportional to the number of pixels that are energized.

Figure 25-12: Charge Pump



25.12 Contrast

Although contrast is heavily dependent on the light source available and the multiplex mode, it also varies with the LCD voltage levels. As previously seen, a potentiometer is used to control the contrast of the LCD panel. The potentiometer sets the separation between each of the LCD voltages. The larger the separation, the better the contrast achievable.

25.13 LCD Glass

The characteristics of the LCD glass vary depending on the materials used. Appendix B gives a list of some LCD manufacturers. Please contact them for the characteristics of your desired glass.

25.14 Initialization

Example 25-5 shows the code for initializing the LCD module with all segments cleared.

Example 25-5: LCD Initialization Code

```
    BCF    PIR1,LCDIF     ; Clear LCD interrupt flag
    BCF    STATUS,RP0     ; Go to Bank2
    BSF    STATUS,RP1
    MOVLW  0x06           ; Set frame freq to ~37Hz
    MOVWF  LCDPS
    MOVLW  0xff           ; Make all pin functions LCD drivers
    MOVWF  LCDSE
    MOVLW  0x17           ; Drive during SLEEP, Charge pump enabled
    MOVWF  LCDCON         ; Timer1 clock source, 1/4 MUX
    CLRF   LCDD00         ; Clear all data registers to turn
    CLRF   LCDD01         ;    all pixels off
    CLRF   LCDD02
    CLRF   LCDD03
    CLRF   LCDD04
    CLRF   LCDD05
    CLRF   LCDD06
    CLRF   LCDD07
    CLRF   LCDD08
    CLRF   LCDD09
    CLRF   LCDD10
    CLRF   LCDD11
    CLRF   LCDD12
    CLRF   LCDD13
    CLRF   LCDD14
    CLRF   LCDD15
    BSF    PIE1,LCDIE      ; Enable LCD interrupts
    BSF    LCDCON,LCDEN    ; Enable LCD Module
    BCF    STATUS,RP1      ; Go to Bank0
```

25.15 Design Tips

Question 1: ***I'm trying to use some of the LCD pins as inputs.***

Answer 1:

Ensure that you have the control bits in the LCDSE properly configured, since these bits override the TRIS bits.

Question 2: ***My LCD panel is flickering.***

Answer 2:

Your frame frequency may be too low. The frame frequency can be changed in the LCDPS register.

Question 3: ***The LCD segments are not very visible.***

Answer 3:

This may be due to misadjusted LCD voltage, some possibilities include:

1. If you are using the R-ladder, try different values of R, vary the R-ladder potentiometer. The VLCDADJ pin should be connected to ground.
2. If you are using the charge pump, adjust the resistance value on the VLCDADJ pin.

25.16 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the LCD drivers are:

Title	Application Note #
Yet Another Clock Using the PIC16C92X	AN649
LCD Fundamentals Using PIC16C92x Microcontrollers	AN658
PICDEM3 Demo Board User's Guide	DS51079

25.17 Revision History

Revision A

This is the initial released revision of the LCD module description.