Section 3. Reset

HIGHLIGHTS

This section of the manual contains the following major topics:

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3.1 Introduction

The reset logic is used to place the device into a known state. The source of the reset can be determined by using the device status bits. The reset logic is designed with features that reduce system cost and increase system reliability.

Devices differentiate between various kinds of reset:

a) Power-on Reset (POR)
b) $\overline{\text{MCLR}}$ reset during normal operation
c) $\overline{\text{MCLR}}$ reset during SLEEP
d) WDT reset during normal operation
e) Brown-out Reset (BOR)
f) Parity Error Reset (PER)

Most registers are unaffected by a reset; their status is unknown on POR and unchanged by all other resets. The other registers are forced to a "reset state" on Power-on Reset, $\overline{\text{MCLR}}$, WDT reset, Brown-out Reset, Parity Error Reset, and on $\overline{\text{MCLR}}$ reset during SLEEP.

The on-chip parity bits that can be used to verify the contents of program memory.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits $\overline{\text{TO}}$, $\overline{\text{PD}}$, $\overline{\text{POR}}$, $\overline{\text{BOR}}$, and $\overline{\text{PER}}$ are set or cleared differently in different reset situations as indicated in Table 3-2. These bits are used in software to determine the nature of the reset. See Table 3-4 for a full description of the reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 3-1. This block diagram is a superset of reset features. To determine the features that are available on a specific device, please refer to the device's Data Sheet.

Note:	While the PICmicro™ is in a reset state, the internal phase clock is held at Q1 (beginning of an instruction cycle).

All new devices will have a noise filter in the $\overline{\text{MCLR}}$ reset path to detect and ignore small pulses. See parameter 30 in the **"Electrical Specifications"** section for pulse width specification.

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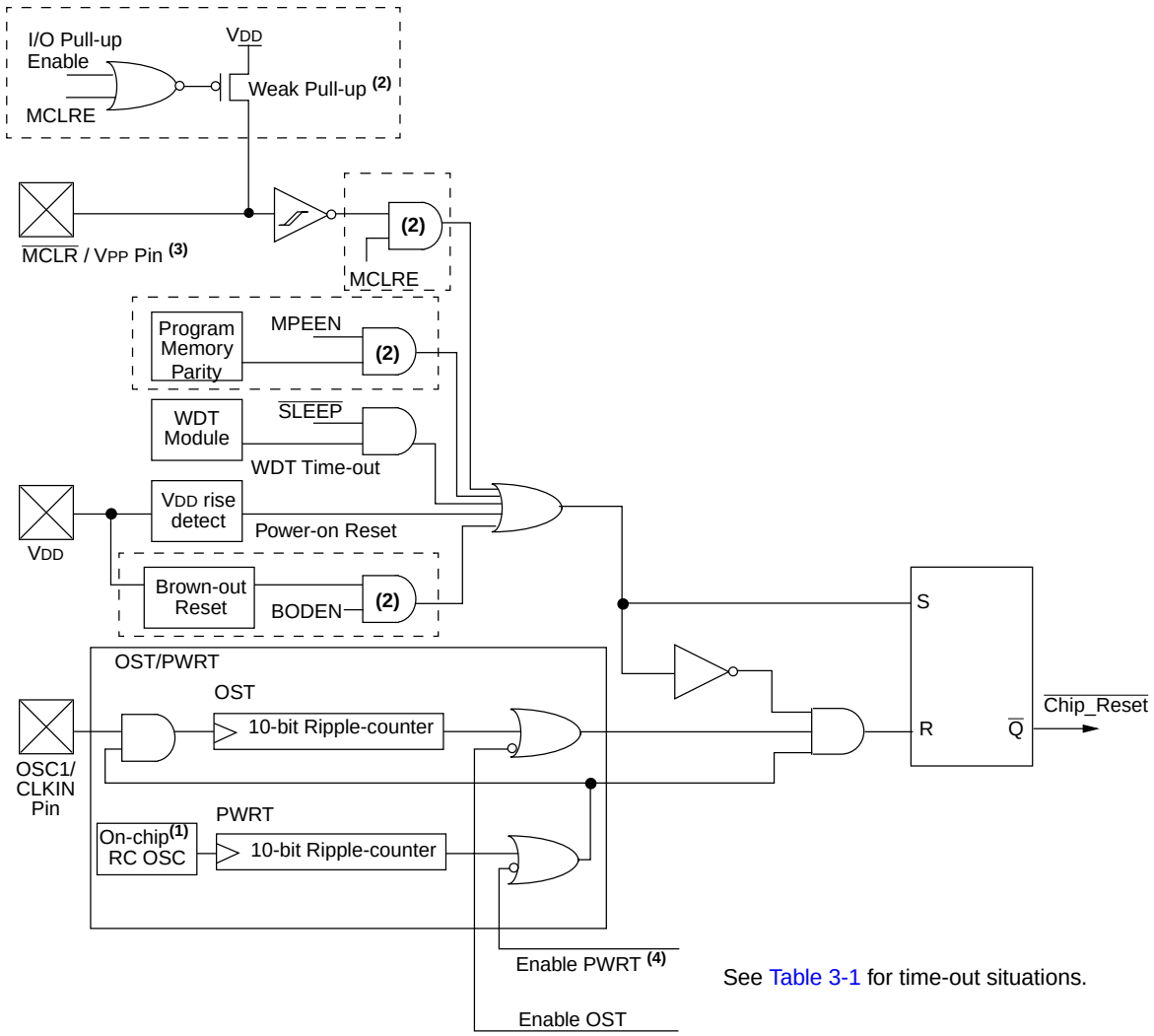
Figure 3-1: Simplified Block Diagram of a Super-set On-chip Reset Circuit



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin or the INTRC oscillator.
2: Features in dashed boxes not available on all devices, see device's Data Sheet.
3: In some devices, this pin may be configured as a general purpose Input.
4: The early PICmicro devices have the configuration bit defined as PWRTE = 1 is enabled, while all other devices the configuration bit is defined as $\overline{PWRTE}$ = 0 is enabled.

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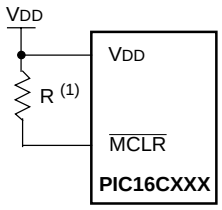
3.2 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST), Brown-out Reset (BOR), and Parity Error Reset (PER)

3.2.1 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected. To take advantage of the POR, just tie the MCLR pin directly (or through a resistor) to VDD as shown in Figure 3-2. This will eliminate external RC components usually needed to create a Power-on Reset. A minimum rise time for VDD is required. See parameter D003 and parameter D004 in the **"Electrical Specifications"** section for details.

Figure 3-2: Using On-Chip POR

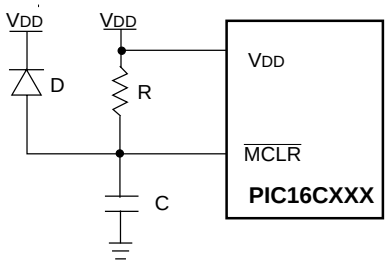


Note: The resistor is optional.

When the device exits the reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges, otherwise the device will not function correctly. Ensure the delay is long enough to get all operating parameters within specification.

Figure 3-3 shows a possible POR circuit for a slow power supply ramp up. The external Power-on Reset circuit is only required if VDD power-up time is too slow. The diode, D, helps discharge the capacitor quickly when VDD powers down.

Figure 3-3: External Power-on Reset Circuit (For Slow VDD Power-up)



Note: R < 40 kΩ is recommended to ensure that the voltage drop across R does not exceed 0.2V. A larger voltage drop will degrade VIH level on the MCLR/VPP pin.

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3.2.2 Power-up Timer (PWRT)

The Power-up Timer provides a nominal 72 ms delay on Power-on Reset (POR) or Brown-out Reset (BOR), see parameter 33 in the **"Electrical Specifications"** section. The Power-up Timer operates on a dedicated internal RC oscillator. The device is kept in reset as long as the PWRT is active. The PWRT delay allows VDD to rise to an acceptable level. The power-up timer enable configuration bit can enable/disable the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled. The polarity of the Power-up Timer configuration bit is now $\overline{\text{PWRTE}}$ = 0 for enabled, while the initial definition of the bit was PWRTE = 1 for enabled. Since all new devices will use the $\overline{\text{PWRTE}}$ = 0 for enabled, the text will describe the operation for such devices. Please refer to the individual Data Sheet to ensure the correct polarity for this bit.

The power-up time delay will vary from device to device due to VDD, temperature, and process variations. See DC parameters for details.

3.2.3 Oscillator Start-up Timer (OST)

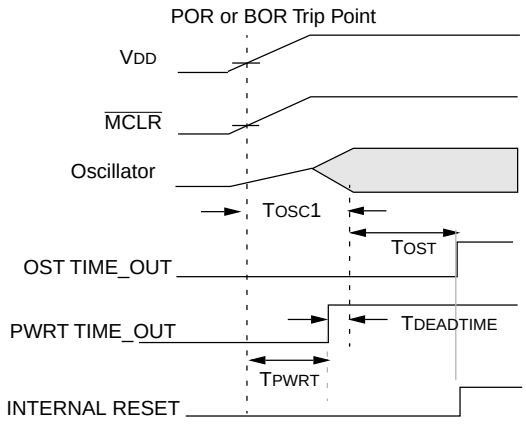
The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and is stable.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset, Brown-out Reset, or wake-up from SLEEP.

The OST counts the oscillator pulses on the OSC1/CLKIN pin. The counter only starts incrementing after the amplitude of the signal reaches the oscillator input thresholds. This delay allows the crystal oscillator or resonator to stabilize before the device exits the OST delay. The length of the time-out is a function of the crystal/resonator frequency.

Figure 3-4 shows the operation of the OST circuit in conjunction with the power-up timer. For low frequency crystals this start-up time can become quite long. That is because the time it takes the low frequency oscillator to start oscillating is longer than the power-up timer's delay. So the time from when the power-up timer times-out, to when the oscillator starts to oscillate is a dead time. There is no minimum or maximum time for this dead time (*TDEADTIME*).

Figure 3-4: Oscillator Start-up Time



Tosc1 = time for the crystal oscillator to react to an oscillation level detectable by the Oscillator Start-up Timer (OST).

TOST = 1024TOSC.

3.2.4 Power-up Sequence

On power-up, the time-out sequence is as follows: First the internal POR is detected, then, if enabled, the PWRT time-out is invoked. After the PWRT time-out is over, the OST is activated. The total time-out will vary based on oscillator configuration and $\overline{PWRTE}$ bit status. For example, in RC mode with the $\overline{PWRTE}$ bit set (PWRT disabled), there will be no time-out at all. Figure 3-5, Figure 3-6 and Figure 3-7 depict time-out sequences.

Since the time-outs occur from the internal POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (Figure 3-7). This is useful for testing purposes or to synchronize more than one device operating in parallel.

If the device voltage is not within the electrical specifications by the end of a time-out, the $\overline{MCLR}$/VPP pin must be held low until the voltage is within the device specification. The use of an external RC delay is sufficient for many of these applications.

Table 3-1 shows the time-outs that occur in various situations, while Figure 3-5 through Figure 3-8 show four different cases that can happen on powering up the device.

Table 3-1: Time-out in Various Situations

Oscillator Configuration	Power-up Timer		Brown-out Reset	Wake-up from SLEEP
	Enabled	Disabled		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024TOSC
RC	72 ms	— (1)	72 ms	— (1)

Note 1: Devices with the Internal/External RC option have a nominal 250 µs delay.

Figure 3-5: Time-out Sequence on Power-up ($\overline{MCLR}$ Tied to VDD)

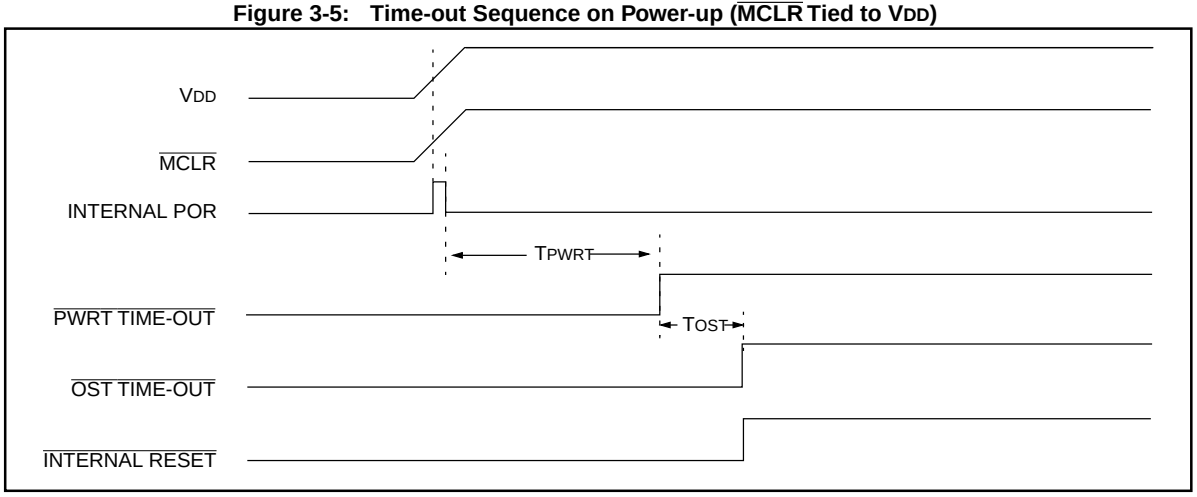


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Figure 3-6: Time-out Sequence on Power-up ($\overline{MCLR}$ not Tied to V_{DD}): Case 1

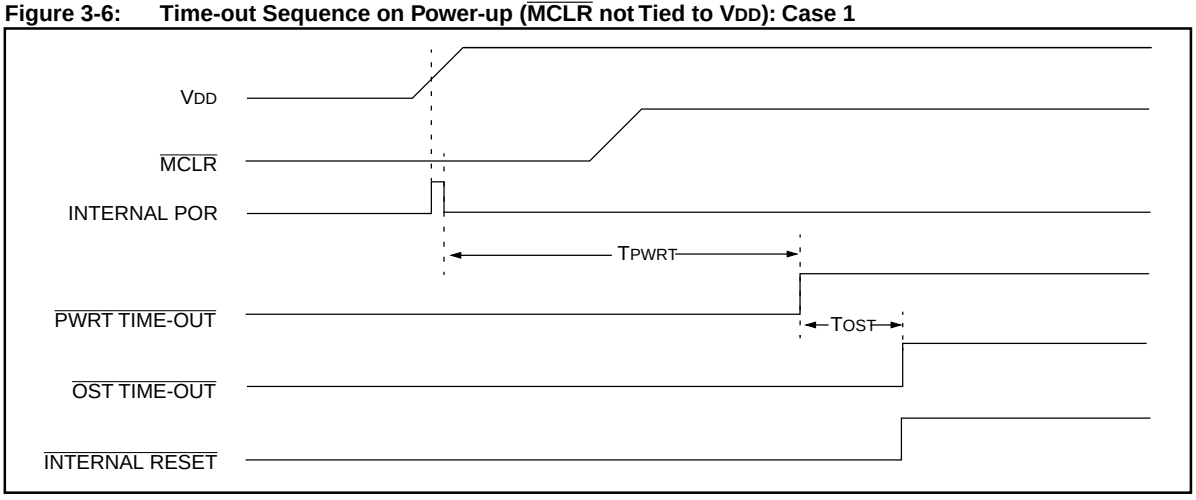


Figure 3-7: Time-out Sequence on Power-up ($\overline{MCLR}$ not Tied to V_{DD}): Case 2

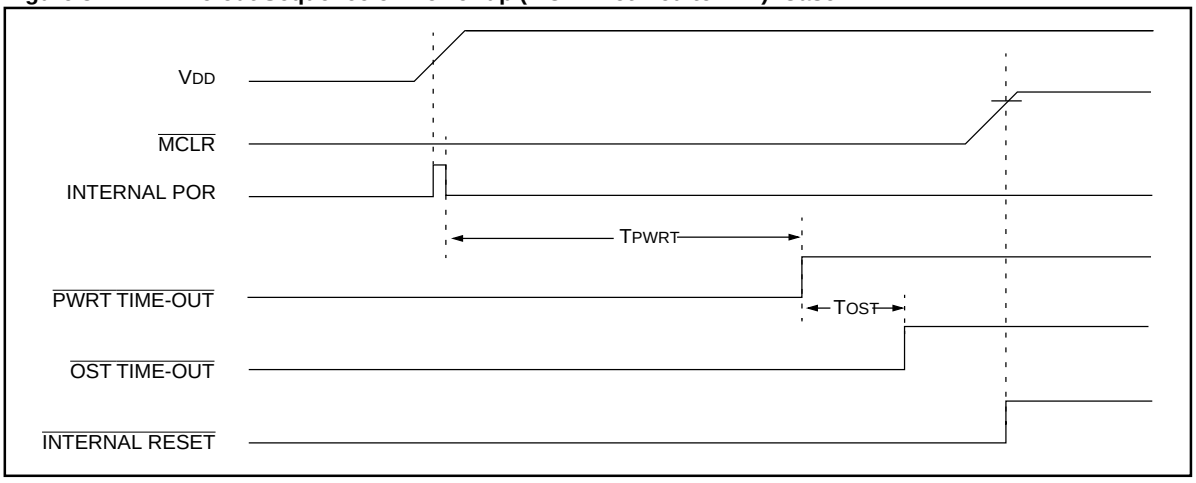
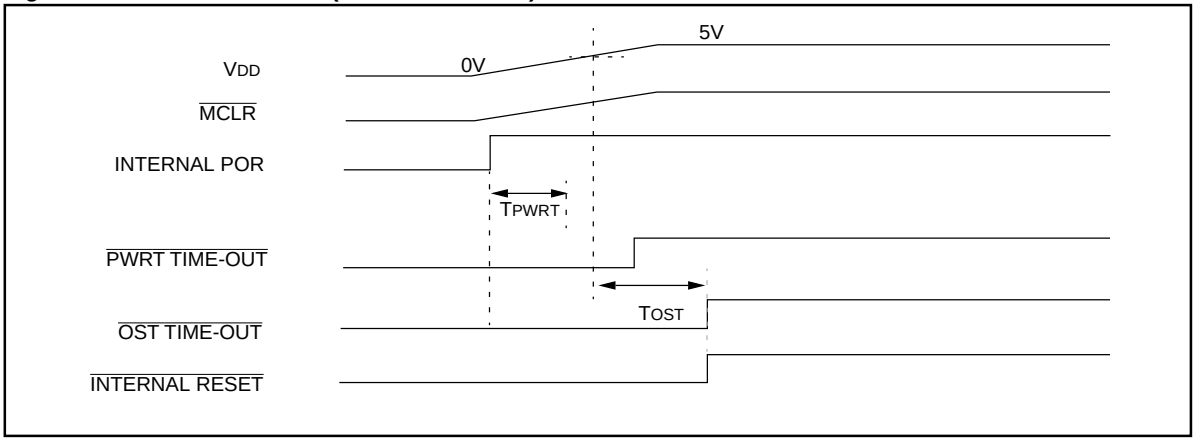


Figure 3-8: Slow Rise Time ($\overline{MCLR}$ Tied to V_{DD})



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3.2.5 Brown-out Reset (BOR)

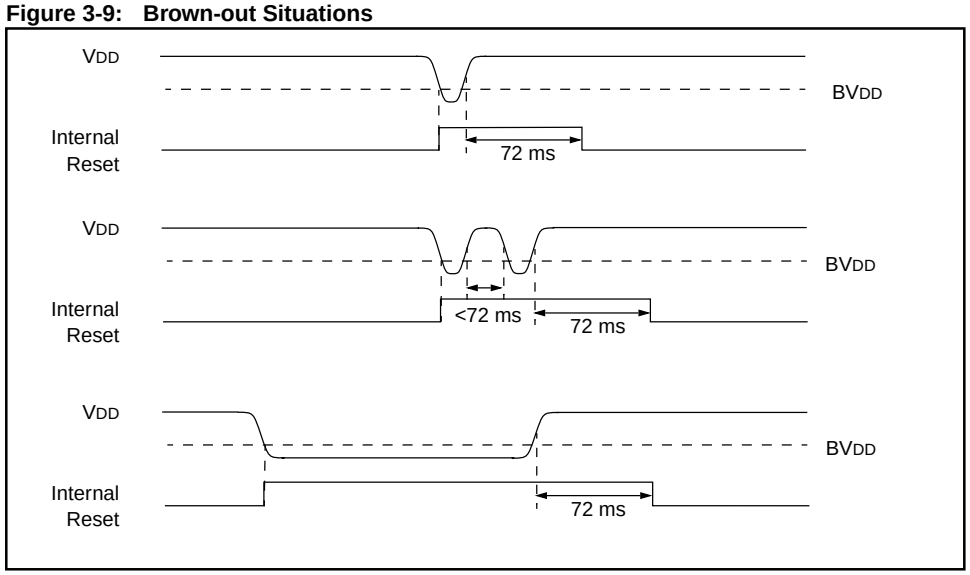
On-chip Brown-out Reset circuitry places the device into reset when the device voltage falls below a trip point (BVDD). This ensures that the device does not continue program execution outside the valid operation range of the device. Brown-out resets are typically used in AC line applications or large battery applications where large loads may be switched in (such as automotive), and cause the device voltage to temporarily fall below the specified operating minimum.

Note:	Before using the on-chip brown-out for a voltage supervisory function (monitor battery decay), please review the electrical specifications to ensure that they meet your requirements.

The BODEN configuration bit can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below BVDD (Typically 4.0V, parameter D005 in the **"Electrical Specifications"** section), for greater than parameter 35, the brown-out situation will reset the chip. A reset is not guaranteed to occur if VDD falls below BVDD for less than parameter 35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in reset an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into Reset and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-up Timer will again start a 72 ms time delay. Figure 3-9 shows typical Brown-out situations.

With the BODEN bit set, all voltages below BVDD will hold the device in the reset state. This includes during the power-up sequence.

Figure 3-9: Brown-out Situations



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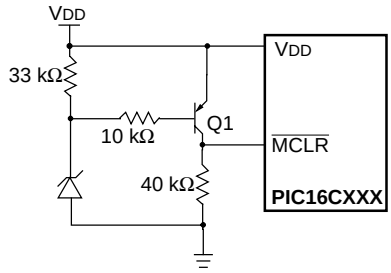
Some devices do not have the on-chip brown-out circuit, and in other cases there are some applications where the Brown-out Reset trip point of the device may not be at the desired level. Figure 3-10 and Figure 3-11 are two examples of external circuitry that may be implemented. Each needs to be evaluated to determine if they match the requirements of the application.

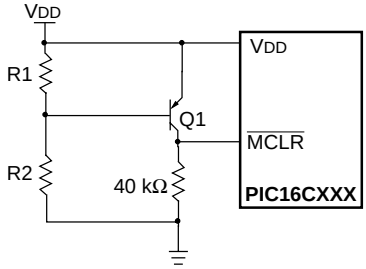
Figure 3-10: External Brown-out Protection Circuit 1



This circuit will activate reset when VDD goes below (Vz + 0.7V)
where Vz = Zener voltage.

Note 1: Internal Brown-out Reset circuitry should be disabled when using this circuit.
2: Resistors should be adjusted for the characteristics of the transistor.

Figure 3-11: External Brown-out Protection Circuit 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Internal Brown-out Reset circuitry should be disabled when using this circuit.
3: Resistors should be adjusted for the characteristics of the transistor.

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3.3 Registers and Status Bit Values

Table 3-2: Status Bits and Their Significance

$\overline{POR}$	$\overline{BOR}^{(1)}$	$\overline{TO}$	$\overline{PD}$	Condition
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1(2)	0	1	1	Brown-out Reset
1(2)	1(2)	0	1	WDT Reset
1(2)	1(2)	0	0	WDT Wake-up
1(2)	1(2)	u	u	$\overline{MCLR}$ reset during normal operation
1(2)	1(2)	1	0	$\overline{MCLR}$ reset during SLEEP

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.
Note 1: Not all devices have BOR circuitry.
2: These bits are unchanged for the given conditions, and when initialized (set) after a POR or a BOR will read as a '1'.

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Table 3-3: Initialization Condition for Special Registers

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	u--- -10x
$\overline{MCLR}$ reset during normal operation	000h	000u uuuu	u--- -uuu
$\overline{MCLR}$ reset during SLEEP	000h	0001 0uuu	u--- -uuu
WDT reset	000h	0000 1uuu	u--- -uuu
WDT Wake-up	PC + 1	uuu0 0uuu	u--- -uuu
Brown-out Reset	000h	0001 1uuu	u--- -uu0
Interrupt Wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	u--- -uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.
Note 1: When the wake-up is due to an interrupt and global enable bit, GIE, is set the PC is loaded with the interrupt vector (0004h) after execution of PC+1.
2: If a status bit is not implemented, that bit will be read as '0'.

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Table 3-4: Initialization Conditions for Special Function Registers

Register	Power-on Reset Brown-out Reset	$\overline{\text{MCLR}}$ Reset during: - normal operation - SLEEP or WDT Reset	Wake-up from SLEEP through: - interrupt - WDT time-out
ADCAPL	0000 0000	0000 0000	uuuu uuuu
ADCAPH	0000 0000	0000 0000	uuuu uuuu
ADCON0	0000 00-0	0000 00-0	uuuu uu-u
ADCON1	---- -000	---- -000	---- -uuu
ADRES	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADTMRL	0000 0000	0000 0000	uuuu uuuu
ADMRH	0000 0000	0000 0000	uuuu uuuu
CCP1CON	--00 0000	--00 0000	--uu uuuu
CCP2CON	0000 0000	0000 0000	uuuu uuuu
CCPR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2L	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2H	xxxx xxxx	uuuu uuuu	uuuu uuuu
CMCON	00-- 0000	00-- 0000	uu-- uuuu
EEADR	xxxx xxxx	uuuu uuuu	uuuu uuuu
EECON1	---0 x000	---0 q000	---0 uuuu
EECON2	-	-	-
EEDATA	xxxx xxxx	uuuu uuuu	uuuu uuuu
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	--xx xxxx	--uu uuuu	--uu uuuu
I2CADD	0000 0000	0000 0000	uuuu uuuu
I2CBUF	xxxx xxxx	uuuu uuuu	uuuu uuuu
I2CCON	0000 0000	0000 0000	uuuu uuuu
I2CSTAT	--00 0000	--00 0000	--uu uuuu
INDF	-	-	-
INTCON	0000 000x	0000 000u	uuuu uuuu(1)
LCDCON	00-0 0000	00-0 0000	uu-u uuuu
LCDD00 to LCDD15	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDPS	---- 0000	---- 0000	---- uuuu
LCDSE	1111 1111	1111 1111	uuuu uuuu
OPTION_REG	1111 1111	1111 1111	uuuu uuuu
OSCCAL	0111 00--	uuuu uu--	uuuu uu--
PCL	0000 0000	0000 0000	PC + 1(2)
PCLATH	---0 0000	---0 0000	---u uuuu
PCON	---- --0u	---- --uu	---- --uu
PIE1	0000 0000	0000 0000	uuuu uuuu
PIE2	---- ---0	---- ---0	---- ---u
PIR1	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 3-3 for reset value for specific condition.

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Table 3-4: Initialization Conditions for Special Function Registers (Cont.'d)

Register	Power-on Reset Brown-out Reset	$\overline{\text{MCLR}}$ Reset during: - normal operation - SLEEP or WDT Reset	Wake-up from SLEEP through: - interrupt - WDT time-out
PIR2	---- ---0	---- ---0	---- ---u
PORTA	--xx xxxx	--uu uuuu	--uu uuuu
PORTB	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	---- -xxx	---- -uuu	---- -uuu
PORTF	0000 0000	0000 0000	uuuu uuuu
PORTG	0000 0000	0000 0000	uuuu uuuu
PR2	1111 1111	1111 1111	1111 1111
PREFA	0000 0000	0000 0000	uuuu uuuu
PREFB	0000 0000	0000 0000	uuuu uuuu
RCSTA	0000 -00x	0000 -00x	uuuu -uuu
RCREG	0000 0000	0000 0000	uuuu uuuu
SLPCON	0011 1111	0011 1111	uuuu uuuu
SPBRG	0000 0000	0000 0000	uuuu uuuu
SSPBUF	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	0000 0000	0000 0000	uuuu uuuu
SSPADD	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	0000 0000	0000 0000	uuuu uuuu
STATUS	0001 1xxx	000q quuu(3)	uuuq quuu(3)
T1CON	--00 0000	--uu uuuu	--uu uuuu
T2CON	-000 0000	-000 0000	-uuu uuuu
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR2	0000 0000	0000 0000	uuuu uuuu
TRIS	--11 1111	--11 1111	--uu uuuu
TRISA	--11 1111	--11 1111	--uu uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
TRISC	1111 1111	1111 1111	uuuu uuuu
TRISD	1111 1111	1111 1111	uuuu uuuu
TRISE	0000 -111	0000 -111	uuuu -uuu
TRISF	1111 1111	1111 1111	uuuu uuuu
TRISG	1111 1111	1111 1111	uuuu uuuu
TXREG	0000 0000	0000 0000	uuuu uuuu
TXSTA	0000 -010	0000 -010	uuuu -uuu
VRCON	000- 0000	000- 0000	uuu- uuuu
W	xxxx xxxx	uuuu uuuu	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 3-3 for reset value for specific condition.

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3.3.1 Power Control (PCON) and STATUS Registers

The Power Control (PCON) register contains a status bit to allow differentiation between a Power-on Reset (POR) to an external $\overline{MCLR}$ Reset or WDT Reset. It also contains a status bit to determine if a Brown-out Reset ($\overline{BOR}$) occurred. The power control/status register, PCON has up to four bits.

The $\overline{BOR}$ (Brown-out Reset) bit, is unknown on a Power-on-reset. It must initially be set by the user and checked on subsequent resets to see if $\overline{BOR}$ = '0' indicating that a Brown-out Reset has occurred. The $\overline{BOR}$ status bit is a “don’t care” bit and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

The $\overline{POR}$ (Power-on Reset) bit, is cleared on a Power-on Reset and is unaffected otherwise. The user sets this bit following a Power-on Reset. On subsequent resets if $\overline{POR}$ is ‘0’, it will indicate that a Power-on Reset must have occurred.

The $\overline{PER}$ (Parity Error Reset) bit, is cleared on a Parity Error Reset and must be set by user software. It will also be set on a Power-on Reset.

The MPEEN (Memory Parity Error Enable) bit, reflects the status of the MPEEN bit in configuration word. It is unaffected by any reset or interrupt.

Note:	$\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

Register 3-1: PCON Register

R-u	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
MPEEN	—	—	—	—	$\overline{PER}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 7 **MPEEN**: Memory Parity Error Circuitry Status bit
This bit reflects the value of the MPEEN configuration bit.

bit 6:3 **Unimplemented:** Read as '0'

bit 2 **$\overline{PER}$**: Memory Parity Error Reset Status bit
1 = No parity error reset occurred
0 = A program memory fetch parity error occurred
(must be set in software after a Power-on Reset or Parity Error Reset occurs)

bit 1 **$\overline{POR}$**: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$**: Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset or Power-on Reset occurs)

Legend		
R = Readable bit	W = Writable bit	u = unchanged bit
U = Unimplemented bit, read as ‘0’		- n = Value at POR reset

Note:	Not all bits may be implemented.

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The STATUS register contains two bits ($\overline{TO}$ and $\overline{PD}$), which when used in conjunction with the PCON register bits provide the user with enough information to determine the cause of the reset.

Register 3-2: STATUS Register

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)

For devices with only Bank0 and Bank1 the IRP bit is reserved, always maintain this bit clear.

bit 6:5 **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)

Each bank is 128 bytes. For devices with only Bank0 and Bank1 the IRP bit is reserved, always maintain this bit clear.

bit 4 **$\overline{TO}$**: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$**: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0 **C**: Carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred

Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

3.4 Design Tips

Question 1: ***When my system is subjected to an environment with ESD and EMI, it operates erratically.***

Answer 1:

If the device you are using does not have filtering to the on-chip master clear circuit (Appendix C), ensure that proper external filtering is placed on the $\overline{\text{MCLR}}$ pin to remove narrow pulses. Electrical Specification parameter 35 specifies the pulse width required to cause a reset.

Question 2: ***With JW (windowed) devices my system resets and operates properly. With an OTP device, my system does not operate properly.***

Answer 2:

The most common reason for this is that the windowed device (JW) has not had its window covered. The background light causes the device to power-up in a different state than would typically be seen in a device where no light is present. In most cases all the General Purpose RAM and Special Function Registers were not initialized properly.

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3.5 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to Resets are:

Title	Application Note #
Power-up Trouble Shooting	AN607
Power-up Considerations	AN522

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3.6 Revision History

Revision A

This is the initial released revision of the Reset description.

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