DIE SUPPORT

Overview of Microchip Die Specifications

INTRODUCTION

This overview is intended to give our customers a better understanding of Microchip's process of die usage and manufacture. This information is not intended as what is needed to manufacture die. It is highly recommended that a manufacturing site that is familiar in die manufacture be used.

A separate document containing device specific information is available from your regional Microchip Sales Office. This information includes the die size, bond pad coordinates, and die diagram for orientation.

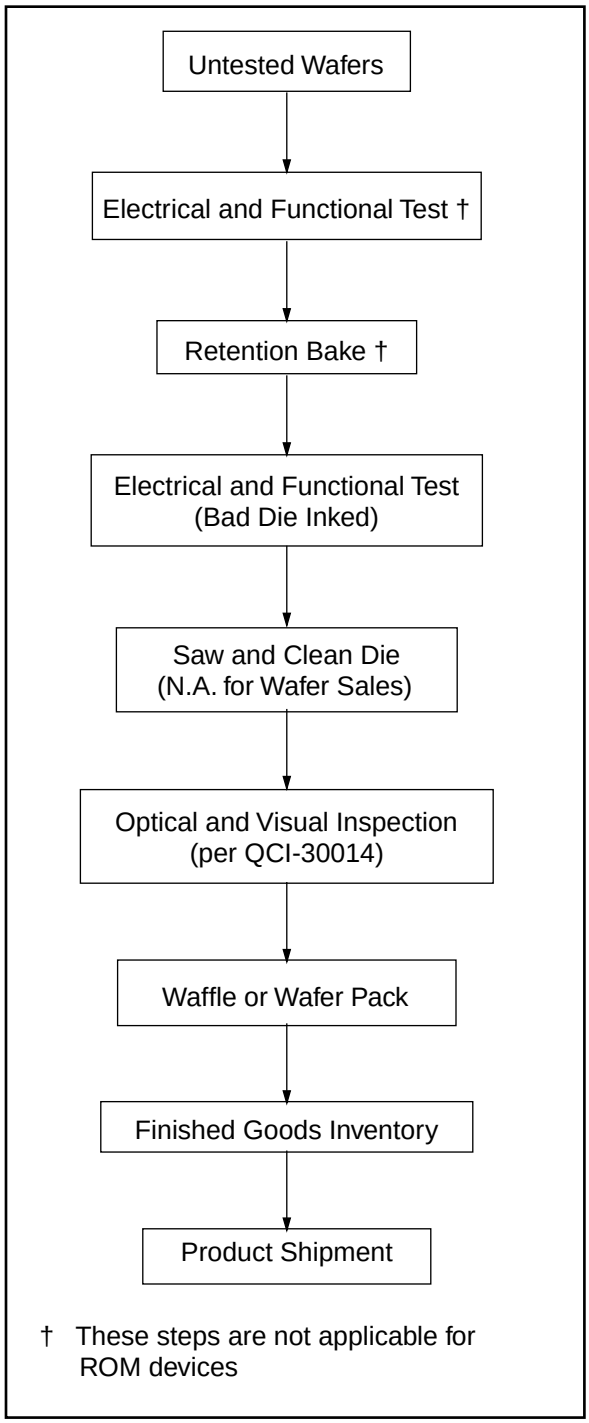
GENERAL DESCRIPTION

In some applications, the size of the product is of critical importance. In these applications it may be required to have the smallest possible size of all components. To support this customer requirement, Microchip offers several small package options including die. If none of the other device package options meet the application device footprint requirement, die offers the smallest size option. This option has some trade-offs.

Board manufacturing with die is more specialized and requires special equipment. This limits the options for manufacturing sites.

The production flow for die product is shown in Figure 1.

FIGURE 1: EEPROM, EEPROM, AND ROM PRODUCTION FLOW



Die Support

TESTING

Die are tested at wafer probe. This testing is not as thorough as packaged devices (due to automatic handling issues). All devices are tested through a reduced temperature range.

For the microcontroller devices:
EPROM and EEPROM devices have all oscillator modes tested.
ROM devices have only the selected oscillator mode tested.

ELECTRICAL SPECIFICATIONS

The functional and electrical specifications of Microchip devices in die form are identical to those of a packaged version. Please refer to individual data sheets for complete details.

QTP

Quick Turnaround Production (QTP) applies only to EPROM and EEPROM microcontrollers.

With QTP devices, the program memory array is only tested against the code provided. This method ensures that the device will operate correctly as programmed, but does not ensure that every program memory bit can be programmed to every state.

Note:	Do not erase QTP devices and program them with a different code.

VISUAL INSPECTIONS

Dice supplied are inspected visually as per Microchip specification (document QCI-30014). Visual inspection criteria includes looking for ink-stains, cracks around the edges of a die or inside a die, metallization defects, passivation defects, particles and bond pad defects. For Microchip's standard die sales specifications please ask for documents QCI-30014 and QCI-30397.

DIE FORM SHIPPING

EPROM devices are supplied as fully erased programmable parts that are UV erasable and re-programmable by the user (except for QTP and SQTP devices).

EEPROM devices may not be supplied in a fully erased state, but are re-programmable by the user (except for QTP and SQTP devices).

ROM devices are supplied as fully programmed parts (program memory only). These are not re-programmable by the user.

Microchip product in die form can be shipped in waffle-pack. The waffle pack has sufficient cavity area to restrain the die, while maintaining their orientation. Lint free paper inserts are placed over the waffle packs, and each pack is secured with a plastic locking clip. Groups of waffle packs are assembled into sets for shipment. A label with lot number, quantity, and part number is attached.

These waffle packs are sealed in hermetic bags with a dry pack.

WAFER SHIPPING

Some products may also be shipped in wafer form (see ordering information). Wafers are shipped in a wafer tub. The tub is padded with non-conductive foam. Lint free paper inserts are placed around each wafer. A label with lot number, quantity, and part number is attached.

STORAGE PROCEDURES

Temperature and humidity greatly affect the storage life of die. It is recommended that the die be used as soon as possible after receipt. While stored by Microchip, these die are kept in a controlled environment.

Upon receipt, the sealed bags should be stored in a cool and dry environment (25°C and 25% relative humidity). In these conditions, sealed bags have a shelf life of 12 months. Temperatures or humidities greater than these will reduce the storage life.

Once a bag containing waffle packs has been opened, the devices should be assembled and encapsulated within 48 hrs (assuming, 25°C and 25% humidity).

DIE HANDLING PROCEDURES

The sealed bags should only be opened when you intend to use the devices.

Once you receive the die, care should be taken in the handling and assembly of the die onto the application board.

Special Pic-n-Place handlers are required to handle the die.

Devices have a passivation covering to protect them during handling and to provide a hermetic seal at the die boundaries.

CAUTION

Some EEPROM devices use EEPROM cells for device configuration. Exposure to ultra-violet light or x-rays must be avoided. Exposure to ultra-violet light or x-rays may cause the device to operate improperly.

Extreme care is urged in the handling and assembly of these products since they are susceptible to damage from electro-static discharge.

SUBSTRATE BONDING

The die is attached to the system board by applying an adhesive to the device substrate. Some devices require that this adhesive be conductive and connect to system ground. For the other devices, this is recommended, but not required. Table 1 shows which devices are required to have the substrate grounded, and for which devices it is recommended. The back sides are back-lapped and are without any gold coating.

TABLE 1: SUBSTRATE BONDING REQUIREMENTS

Device Family	Substrate Bonding to Ground
PIC16C5X †	Required
PIC16C5XA †	Recommended
PIC16CXX †	Recommended
PIC17CXX †	Recommended
PIC14XXX	Recommended
AY0438	Recommended
24XXXX	Recommended
85XXX	Recommended
93XXXX	Recommended
59XXX	Recommended
28XXXX	Recommended
27XXXXX	Recommended

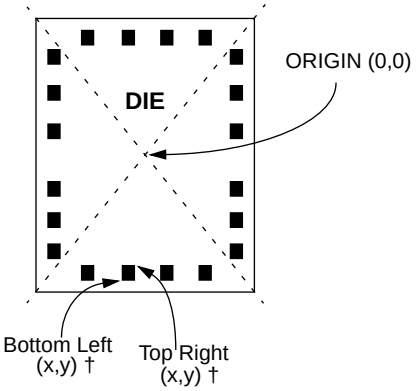
† Device family also includes the wide voltage (LC) and ROM (CR) versions.

BOND PAD COORDINATES

The die figures have associated bond pad coordinates. These coordinates assist in the attaching of the bond wire to the die. All the dimensions of these coordinates are in micrometers (µm) unless otherwise specified. The origin for the coordinates is the center of the die, as shown in Figure 2. These coordinates would be programmed into an auto-wire bonder for automated assembly.

The bond pad size is that of the passivation opening. The passivation overlaps the bond pad metal by at least 0.1 mil. There is a minimum bond pad to bond pad spacing. This spacing is measured from the edges of passivation openings. The device die specification sheet will specify the minimum spacing. Some of the V_{SS} and V_{DD} pad openings are larger then the standard bond pad for double bonding option.

FIGURE 2: DIE COORDINATE ORIGIN



† All dimensions in µm unless specified otherwise.

The die is capable of thermosonic gold or ultrasonic wire bonding. Die meet the minimum conditions of MIL-STD 883, Method 2011 on “Bond Strength (Destructive Bond Pull Test)”. The Bond Pad metallization is silicon doped aluminum.

Die Support

ENCAPSULATION

After the device has been attached and connected to the application board, the die needs to be protected from damage. Encapsulation is the process of protecting the device (and lead wires) from damage. There are two common methods for this encapsulation. These are:

1. Nonconductive potting material
2. Plastic transfer molding

The die should not be exposed to a temperature greater than 180°C.

MECHANICAL SPECIFICATION

The mechanical specifications for the die, excluding die size and bond pad coordinates, are show in Table 2 and Table 3.

ORDERING INFORMATION

Die sales must be conducted by contacting your Microchip Sales Office.

To order or obtain information (on pricing or delivery) for a specific device, use one of the following part numbers:

Devices in Waffle Pack
DEVICE_NUMBER/S

Devices in Wafer form
DEVICE_NUMBER/W

where DEVICE_NUMBER is the device that you require. The S specifies die in a waffle pack while a W specifies wafer sales. Example 1 shows some example part numbers.

Note:	Microcontroller devices (PIC16/17) are NOT offered in wafer shipments

EXAMPLE 1: PART NUMBERS

Device	Product Identification System Number	
	Waffle Pack	**Wafer**
PIC16CR57A	PIC16CR57A/S	N.A.
PIC16C65	PIC16C65/S	N.A.
PIC17C44	PIC17C44/S	N.A.
PIC14000	PIC14000/S	N.A
24AA04	24AA04/S	24AA04/W
85C72	85C72/S	85C72/W
93AA46	93AA46/S	93AA46/W
59C11	59C11/S	59C11/W
28C04A	28C04A/S	28C04A/W
27C64	27C64/S	27C64/W

PRODUCT INFORMATION

For additional information concerning individual die specifications, please contact you local Microchip Technology Incorporated sales office.

TABLE 2: DIE MECHANICAL DIMENSIONS

Specification	Min.	Typ.	Max.	Unit	Comments
Bond pad opening	§	§	—	mil µm	See Individual Die Data Sheet Note 1
Bond pad spacing	§	—	—	mil µm	See Individual Die Data Sheet Note 2
Die thickness					
PIC16/17 (EPROM/EEPROM/ROM)	14 356	15 381	16 406	mil µm	Note 3
Memory Products	14 356	15 381	16 406	mil µm	Note 3
Custom die thickness	N.A. N.A.	— —	22 559	mil µm	Contact Microchip Factory Marketing Note 3, Note 4
Die thickness tolerance (Standard and Custom)	— —	— —	± 1 ± 25.4	mil µm	Note 3

§ Refer to the Individual Device Die Data Sheet for this specification

Note 1: The bond pad size is that of the passivation opening. The passivation overlaps the bond pad metal by at least 0.1 mil. Some of the V_{SS} and V_{DD} pad openings are larger for double bonding option.

2: Bond pads are measured from the edges of passivation openings.

3: This specification is not tested. For design guidance only.

4: Custom die thickness is available (contact the Microchip Sales Office or Microchip Factory Marketing). As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow (up to the standard thickness).

5: The conversion rate is 25.4 µm / mil (a mil is 1/1000 of an inch).

TABLE 3: DIE MECHANICAL SPECIFICATIONS

Die backside preparation	Die backside are backlapped and without any backside gold.
Pad metallization	Pad metallization is silicon doped aluminum.
Bonding techniques	The die shall be capable of making a bond in one of the following ways: a) gold thermosonic b) aluminum ultrasonic
Die attach techniques	The dice are capable of bonding either by using a gold eutectic bond to a gold plated pedestal (containing 60 microinches of gold) or by using an electrically conductive adhesive (e.g. conductive epoxy) to any substrate. The substrate must be tied to V_{SS}.

WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602-786-7200 Fax: 602-786-7277
Technical Support: 602 786-7627
Web: http://www.microchip.com

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508-480-9990 Fax: 508-480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972-991-7177 Fax: 972-991-8588

Dayton
Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714-263-1888 Fax: 714-263-1338

New York
Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 516-273-5305 Fax: 516-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong
Microchip Asia Pacific
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

India
Microchip Technology Inc.
India Liaison Office
No. 6, Legacy, Convent Road
Bangalore 560 025, India
Tel: 91-80-229-0061 Fax: 91-80-229-0062

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai
Microchip Technology
RM 406 Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hong Qiao District
Shanghai, PRC 200335
Tel: 86-21-6275-5700
Fax: 86 21-6275-5060

Singapore
Microchip Technology Taiwan
Singapore Branch
200 Middle Road
#07-02 Prime Centre
Singapore 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C
Microchip Technology Taiwan
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2-717-7175 Fax: 886-2-545-0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-1189-21-5858 Fax: 44-1189-21-5835

France
Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Müchen, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-39-6899939 Fax: 39-39-6899883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa 222 Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

10/31/97

DNV Certification, Inc. USA
ACCREDITED REGISTRAR ANSI-RAB
DNV
DNV MSC The Netherlands Accredited by the RvA
ISO 9001 REGISTERED FIRM