



# 24LCS21A

## 1K 2.5V Dual Mode I<sup>2</sup>C™ Serial EEPROM

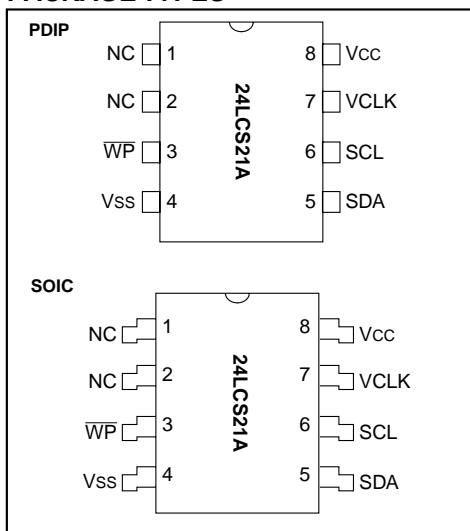
### FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification, including recovery to DDC1
- Low power CMOS technology
  - 1 mA typical active current
  - 10 µA standby current typical at 5.5V
- 2-wire serial interface bus, I<sup>2</sup>C™ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Hardware write-protect pin
- Page-write buffer for up to eight bytes
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- ESD Protection > 4000V
- 8-pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +70°C

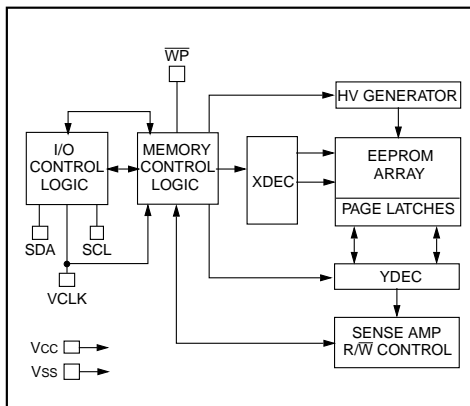
### DESCRIPTION

The Microchip Technology Inc. 24LCS21A is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit-Only Mode and Bi-directional Mode. Upon power-up, the device will be in the Transmit-Only Mode, sending a serial bit stream of the memory array from 00h to 7Fh, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the transition mode, and look for a valid control byte on the I<sup>2</sup>C bus. If it detects a valid control byte from the master, it will switch into Bi-directional Mode, with byte selectable read/write capability of the memory array using SCL. If no control byte is received, the device will revert to the Transmit-Only Mode after it receives 128 consecutive VCLK pulses while the SCL pin is idle. The 24LCS21A also enables the user to write-protect the entire memory array using its write-protect pin. The 24LCS21A is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

### PACKAGE TYPES



### BLOCK DIAGRAM



DDC is a trademark of the Video Electronics Standards Association.  
I<sup>2</sup>C is a trademark of Philips Corporation.

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

V<sub>CC</sub> ..... 7.0V  
 All inputs and outputs w.r.t. V<sub>SS</sub> ..... -0.6V to V<sub>CC</sub> +1.0V  
 Storage temperature ..... -65°C to +150°C  
 Ambient temp. with power applied ..... -65°C to +125°C  
 Soldering temperature of leads (10 seconds) .. +300°C  
 ESD protection on all pins ..... ≥ 4 kV

\***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

| Name            | Function                           |
|-----------------|------------------------------------|
| $\overline{WP}$ | Write Protect (active low)         |
| V <sub>SS</sub> | Ground                             |
| SDA             | Serial Address/Data I/O            |
| SCL             | Serial Clock (Bi-directional Mode) |
| VCLK            | Serial Clock (Transmit-Only Mode)  |
| V <sub>CC</sub> | +2.5V to 5.5V Power Supply         |
| NC              | No Connection                      |

TABLE 1-2: DC CHARACTERISTICS

| V <sub>CC</sub> = +2.5V to 5.5V<br>Commercial (C): T <sub>amb</sub> = 0°C to +70°C<br>Industrial (I): T <sub>amb</sub> = -40°C to +85°C |                                    |                     |                     |       |  |
|---|------------------------------------|---------------------|---------------------|-------|--|
| Parameter   | Symbol                             | Min                 | Max                 | Units | Conditions   |
| SCL and SDA pins:<br>High level input voltage   | V <sub>IH</sub>                    | 0.7 V <sub>CC</sub> | —                   | V     | V <sub>CC</sub> ≥ 2.7V (Note)<br>V <sub>CC</sub> < 2.7V (Note)<br>(Note)           |
| Low level input voltage   | V <sub>IL</sub>                    | —                   | 0.3 V <sub>CC</sub> | V     |  |
| Input levels on VCLK pin:<br>High level input voltage   | V <sub>IH</sub>                    | 2.0                 | —                   | V     |  |
| Low level input voltage   | V <sub>IL</sub>                    | —                   | 0.2 V <sub>CC</sub> | V     |  |
| Hysteresis of Schmitt trigger inputs  | V <sub>HYS</sub>                   | .05 V <sub>CC</sub> | —                   | V     | (Note)   |
| Low level output voltage  | V <sub>OL1</sub>                   | —                   | 0.4                 | V     | I <sub>OL</sub> = 3 mA, V <sub>CC</sub> = 2.5V (Note)                              |
| Low level output voltage  | V <sub>OL2</sub>                   | —                   | 0.6                 | V     | I <sub>OL</sub> = 6 mA, V <sub>CC</sub> = 2.5V                                     |
| Input leakage current   | I <sub>LI</sub>                    | -10                 | 10                  | μA    | V <sub>IN</sub> = 0.1V to V <sub>CC</sub>  |
| Output leakage current  | I <sub>LO</sub>                    | -10                 | 10                  | μA    | V <sub>OUT</sub> = 0.1V to V <sub>CC</sub>   |
| Pin capacitance (all inputs/outputs)  | C <sub>in</sub> , C <sub>out</sub> | —                   | 10                  | pF    | V <sub>CC</sub> = 5.0V (Note)<br>T <sub>amb</sub> = 25°C, F <sub>CLK</sub> = 1 MHz |
| Operating current   | I <sub>CC</sub> Write              | —                   | 3                   | mA    | V <sub>CC</sub> = 5.5V   |
|   | I <sub>CC</sub> Read               | —                   | 1                   | mA    | V <sub>CC</sub> = 5.5V, SCL = 400 kHz  |
| Standby current   | I <sub>CCS</sub>                   | —                   | 30                  | μA    | V <sub>CC</sub> = 3.0V, SDA = SCL = V <sub>CC</sub>                                |
|   |                                    | —                   | 100                 | μA    | V <sub>CC</sub> = 5.5V, SDA = SCL = V <sub>CC</sub><br>VCLK = V <sub>SS</sub>      |

Note: This parameter is periodically sampled and not 100% tested.

**TABLE 1-3: AC CHARACTERISTICS**

| Parameter   | Symbol  | Vcc= 2.5-4.5V<br>Standard Mode |      | Vcc= 4.5 - 5.5V<br>Fast Mode |      | Units  | Remarks   |
|---|---------|--------------------------------|------|------------------------------|------|--------|---|
|   |         | Min                            | Max  | Min                          | Max  |        |   |
| Clock frequency                                   | FCLK    | —                              | 100  | —                            | 400  | kHz    |   |
| Clock high time                                   | THIGH   | 4000                           | —    | 600                          | —    | ns     |   |
| Clock low time                                    | TLOW    | 4700                           | —    | 1300                         | —    | ns     |   |
| SDA and SCL rise time                             | TR      | —                              | 1000 | —                            | 300  | ns     | (Note 1)  |
| SDA and SCL fall time                             | TF      | —                              | 300  | —                            | 300  | ns     | (Note 1)  |
| START condition hold time                         | THD:STA | 4000                           | —    | 600                          | —    | ns     | After this period the first clock pulse is generated          |
| START condition setup time                        | TSU:STA | 4700                           | —    | 600                          | —    | ns     | Only relevant for repeated START condition                    |
| Data input hold time                              | THD:DAT | 0                              | —    | 0                            | —    | ns     | (Note 2)  |
| Data input setup time                             | TSU:DAT | 250                            | —    | 100                          | —    | ns     |   |
| STOP condition setup time                         | TSU:STO | 4000                           | —    | 600                          | —    | ns     |   |
| Output valid from clock                           | TAA     | —                              | 3500 | —                            | 900  | ns     | (Note 2)  |
| Bus free time                                     | TBUF    | 4700                           | —    | 1300                         | —    | ns     | Time the bus must be free before a new transmission can start |
| Output fall time from VIH minimum to VIL maximum  | TOF     | —                              | 250  | 20 + 0.1 CB                  | 250  | ns     | (Note 1), CB ≤ 100 pF   |
| Input filter spike suppression (SDA and SCL pins) | TSP     | —                              | 50   | —                            | 50   | ns     | (Note 3)  |
| Write cycle time                                  | TWR     | —                              | 10   | —                            | 10   | ms     | Byte or Page mode   |
| <b>Transmit-Only Mode Parameters</b>              |         |                                |      |                              |      |        |   |
| Output valid from VCLK                            | TVAA    | —                              | 2000 | —                            | 1000 | ns     |   |
| VCLK high time                                    | TVHIGH  | 4000                           | —    | 600                          | —    | ns     |   |
| VCLK low time                                     | TVLOW   | 4700                           | —    | 1300                         | —    | ns     |   |
| VCLK setup time                                   | TVHST   | 0                              | —    | 0                            | —    | ns     |   |
| VCLK hold time                                    | TSPVL   | 4000                           | —    | 600                          | —    | ns     |   |
| Mode transition time                              | TVHZ    | —                              | 1000 | —                            | 500  | ns     |   |
| Transmit-Only power up time                       | TVPU    | 0                              | —    | 0                            | —    | ns     |   |
| Input filter spike suppression (VCLK pin)         | TSPV    | —                              | 100  | —                            | 100  | ns     |   |
| Endurance   | —       | 1M                             | —    | 1M                           | —    | cycles | 25°C, Vcc = 5.0V, Block Mode (Note 4)                         |

Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

- As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide noise and spike suppression. This eliminates the need for a TI specification for standard operation.
- This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

## 2.0 FUNCTIONAL DESCRIPTION

The 24LCS21A is designed to comply to the DDC Standard proposed by VESA (Figure 3-3) with the exception that it is not Access.bus capable. It operates in two modes, the Transmit-Only Mode and the Bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input but sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bi-directional Mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bi-directional Mode. Otherwise, it will revert to the Transmit-Only Mode after it sees 128 VCLK pulses.

### 2.1 Transmit-Only Mode

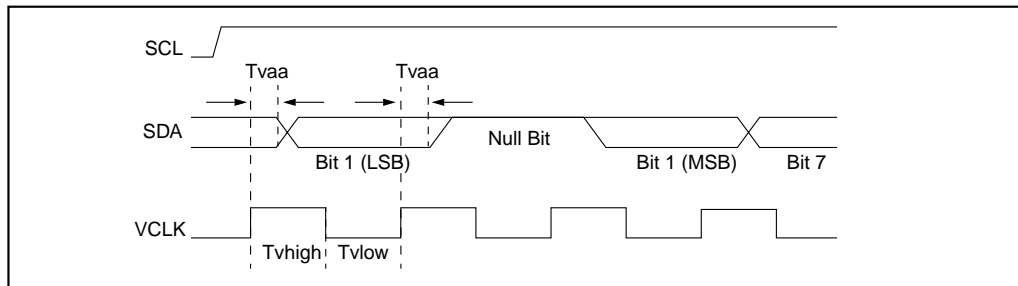
The device will power up in the Transmit-Only Mode at address 00h. This mode supports a unidirectional 2-wire protocol for continuous transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the

Transmit-Only Mode (Section 2.2). In this mode, data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. After address 7Fh in the memory array is transmitted, the internal address pointers will wrap around to the first memory location (00h) and continue. The Bi-directional Mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only Mode.

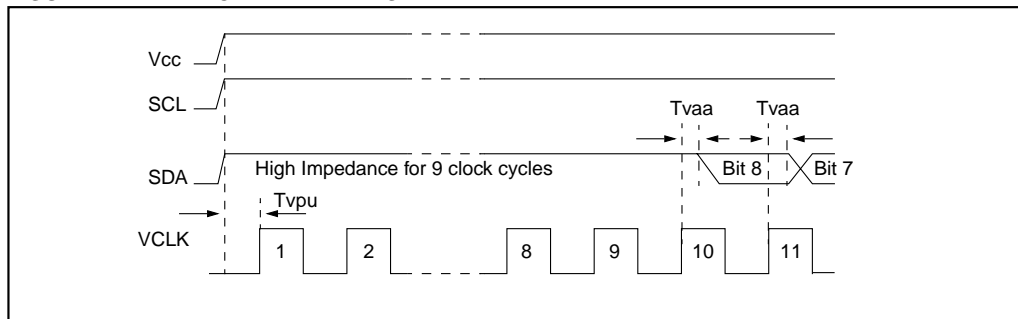
### 2.2 Initialization Procedure

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal synchronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit in address 00h. (Figure 2-2).

**FIGURE 2-1: TRANSMIT-ONLY MODE**



**FIGURE 2-2: DEVICE INITIALIZATION**

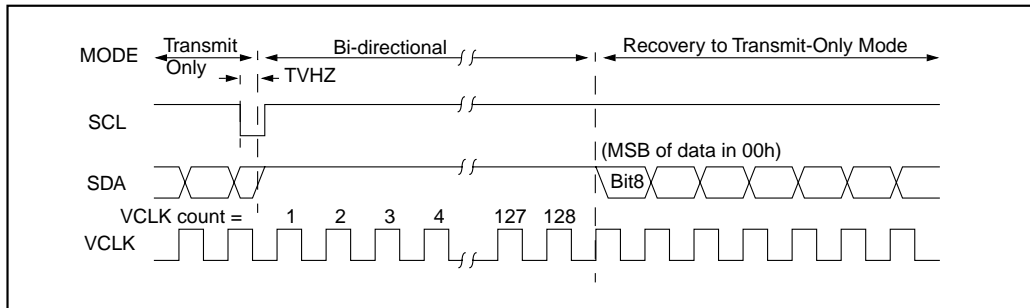


## 3.0 BI-DIRECTIONAL MODE

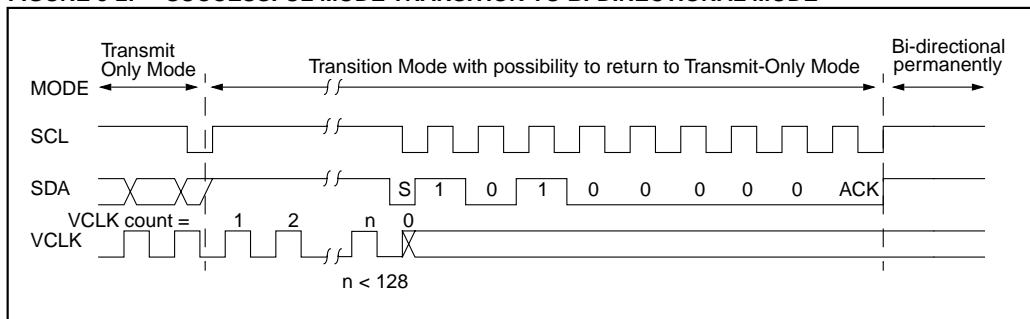
Before the 24LCS21A can be switched into the Bi-directional Mode (Figure 3-1), it must enter the transition mode, which is done by applying a valid high to low transition on the Bi-directional Mode Clock (SCL). As soon it enters the transition mode, it looks for a control byte 1010 000X on the I<sup>2</sup>C™ bus, and starts to count pulses on VCLK. Any high to low transition on the SCL line will reset the count. If it sees a pulse count of 128 on VCLK while the SCL line is idle, it will revert back to the Transmit-Only Mode, and transmit its contents starting with the most significant bit in address 00h. However, if it detects the control byte on the I<sup>2</sup>C™ bus, (Figure 3-2) it will switch to the in the Bi-directional Mode. Once the device has made the transition to the Bi-directional mode, the only way to switch the device back to the Transmit-Only Mode is to remove power from the device. The mode transition process is shown in detail in Figure 3-3.

Once the device has switched into the Bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire Bi-directional data transmission protocol (I<sup>2</sup>C™). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the 24LCS21A acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bi-directional mode, the 24LCS21A only responds to commands for device 1010 000X.

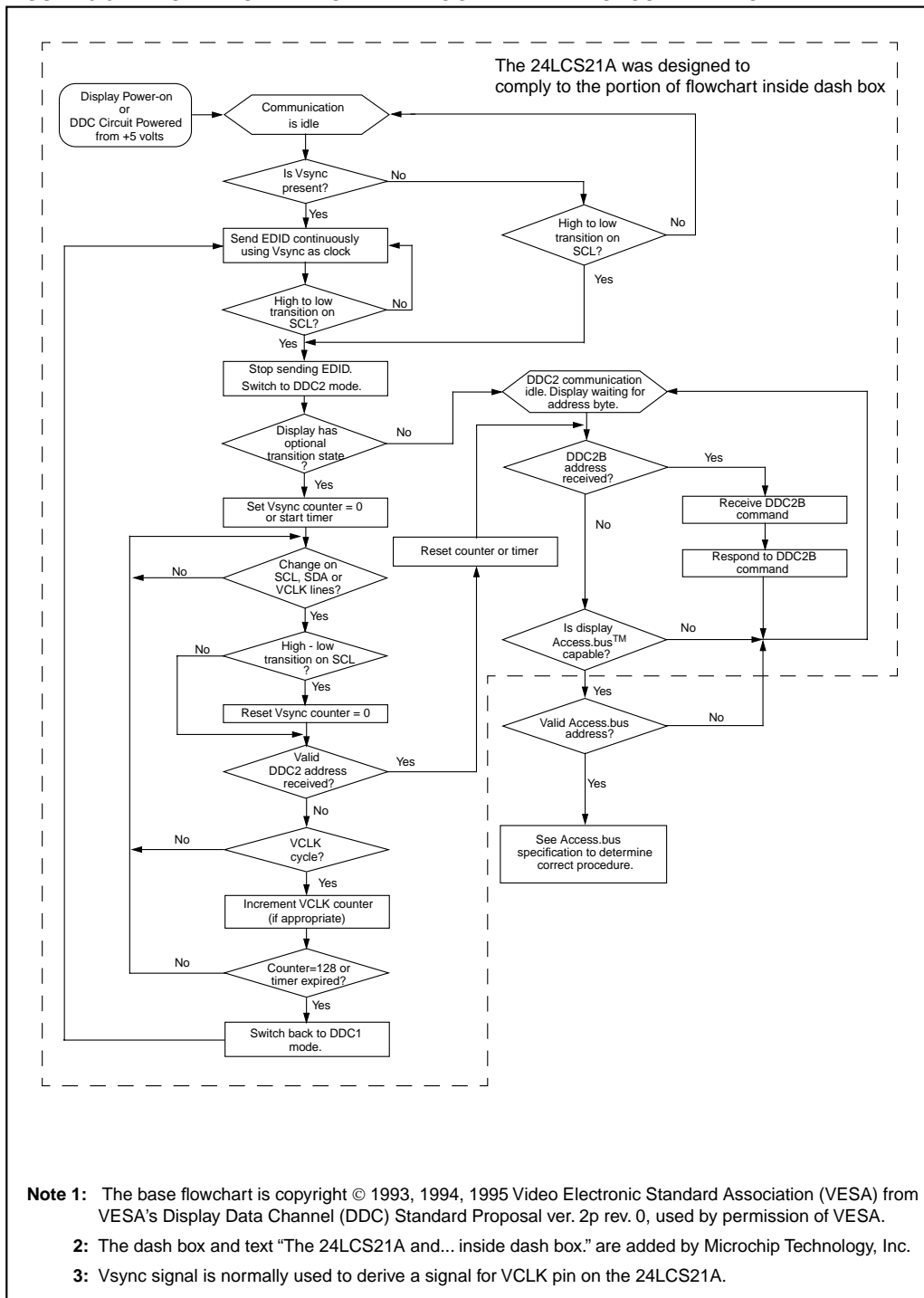
**FIGURE 3-1: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE**



**FIGURE 3-2: SUCCESSFUL MODE TRANSITION TO BI-DIRECTIONAL MODE**



**FIGURE 3-3: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA**



## 3.1 Bi-directional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-4).

### 3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

### 3.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

### 3.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

### 3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and

STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

**Note:** Once switched into Bi-directional Mode, the 24LCS21A will remain in that mode until power is removed. Removing power is the only way to reset the 24LCS21A into the Transmit-only mode.

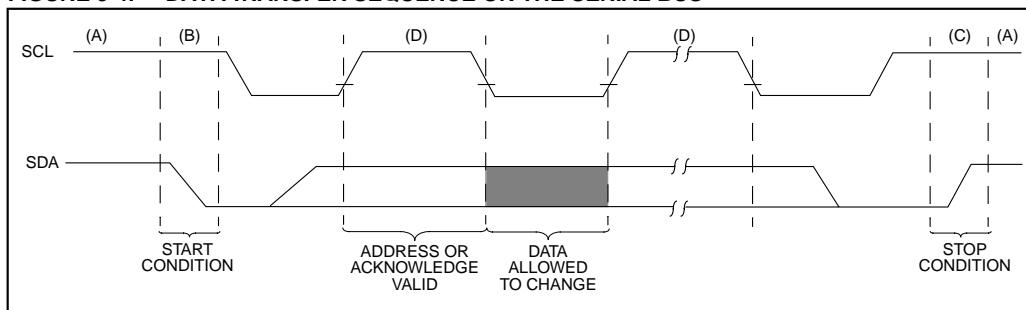
### 3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

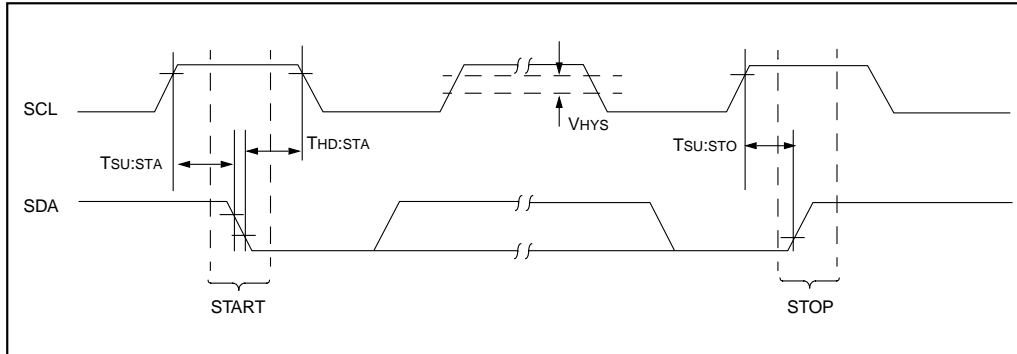
**Note:** The 24LCS21A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

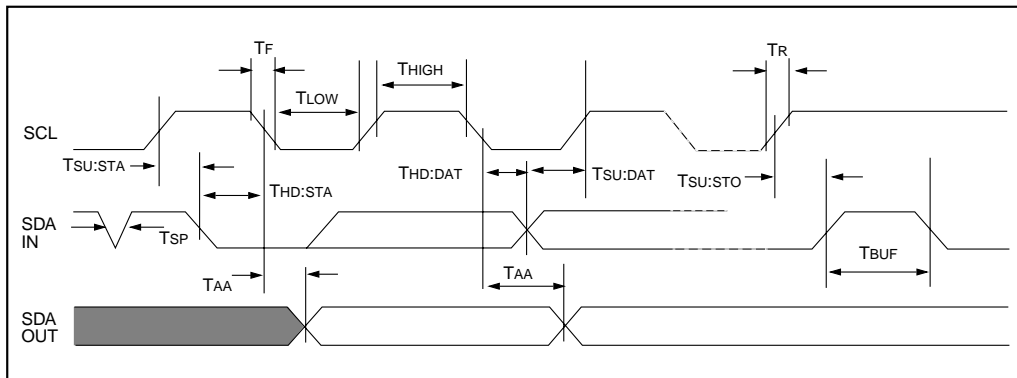
**FIGURE 3-4: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**



**FIGURE 3-5: BUS TIMING START/STOP**



**FIGURE 3-6: BUS TIMING DATA**



## 3.1.6 SLAVE ADDRESS

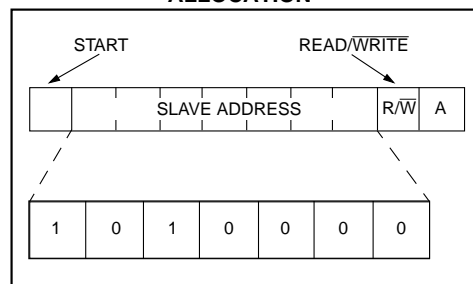
After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010000) for the 24LCS21A.

The eighth bit of slave address determines whether the master device wants to read or write to the 24LCS21A (Figure 3-7).

The 24LCS21A monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

| Operation | Slave Address | R/W |
|-----------|---------------|-----|
| Read      | 1010000       | 1   |
| Write     | 1010000       | 0   |

**FIGURE 3-7: CONTROL BYTE ALLOCATION**





## 4.0 WRITE OPERATION

### 4.1 Byte Write

Following the start signal from the master, the slave address (four bits), three zero bits (000) and the R/W bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LCS21A. After receiving another acknowledge signal from the 24LCS21A the master device will transmit the data word to be written into the addressed memory location. The 24LCS21A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LCS21A will not generate acknowledge signals (Figure 4-1).

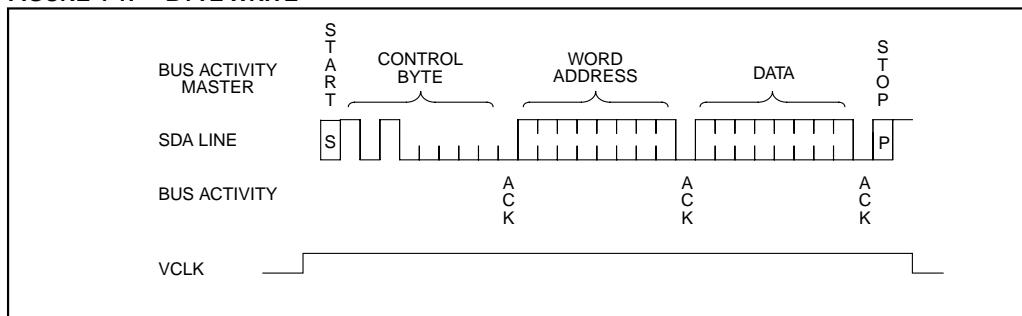
It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

### 4.2 Page Write

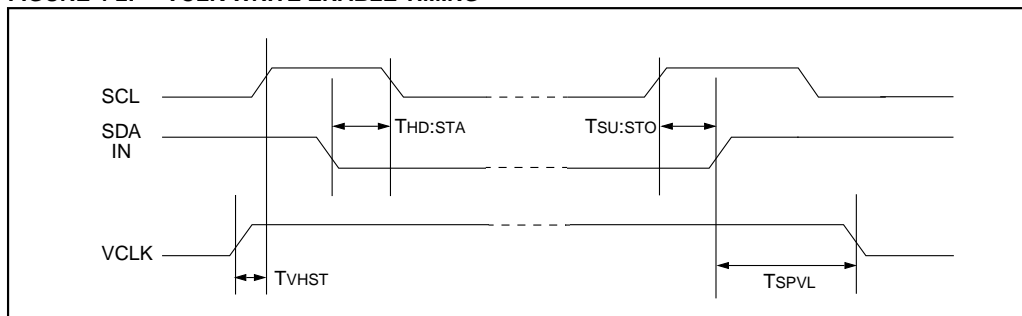
The write control byte, word address and the first data byte are transmitted to the 24LCS21A in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LCS21A which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 5-2).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

**FIGURE 4-1: BYTE WRITE**



**FIGURE 4-2: VCLK WRITE ENABLE TIMING**



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ( $R/\overline{W} = 0$ ). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW

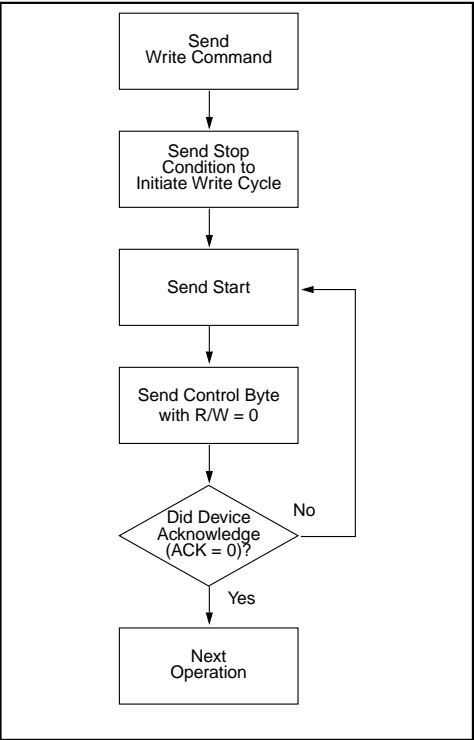
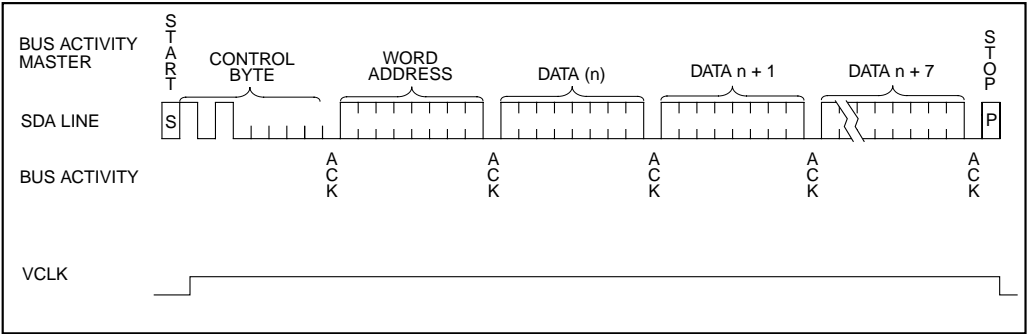


FIGURE 5-2: PAGE WRITE



## 6.0 WRITE PROTECTION

When using the 24LCS21A in the Bi-directional Mode, the VCLK pin can be used as a write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the 24LCS21A to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

Additionally, Pin three performs a flexible write protect function. The 24LCS21A contains a write-protection control fuse whose factory default state is cleared. Writing any data to address 7Fh (normally the checksum in DDC applications) sets the fuse which enables the  $\overline{WP}$  pin. Until this fuse is set, the 24LCS21A is always write enabled (if VCLK = 1). After the fuse is set, the write capability of the 24LCS21A is determined by both VCLK and  $\overline{WP}$  pins (Table 6-1).

**TABLE 6-1: WRITE PROTECT TRUTH TABLE**

| VCLK | $\overline{WP}$ | Address 7Fh Written | Mode for 00h - 7Fh |
|------|-----------------|---------------------|--------------------|
| 0    | X               | X                   | Read Only          |
| 1    | X               | No                  | R/W                |
| 1    | 1/open          | X                   | R/W                |
| 1    | 0               | Yes                 | Read Only          |

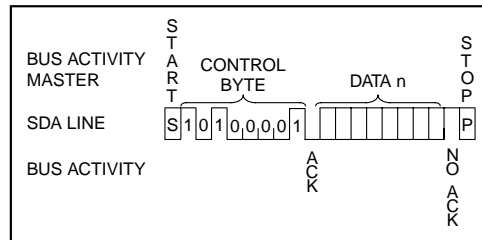
## 7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

### 7.1 Current Address Read

The 24LCS21A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the 24LCS21A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21A discontinues transmission (Figure 7-1).

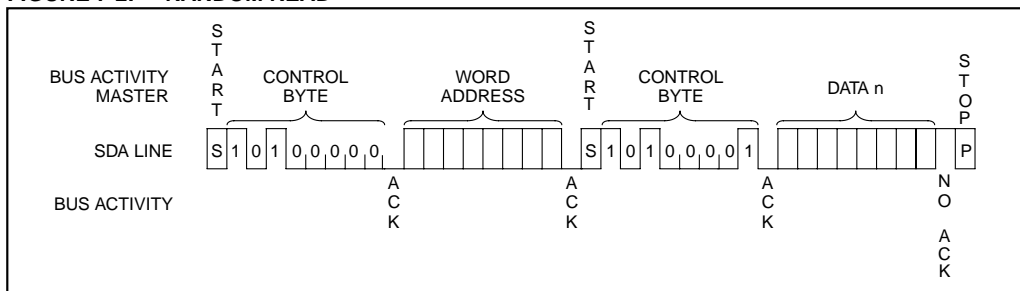
**FIGURE 7-1: CURRENT ADDRESS READ**



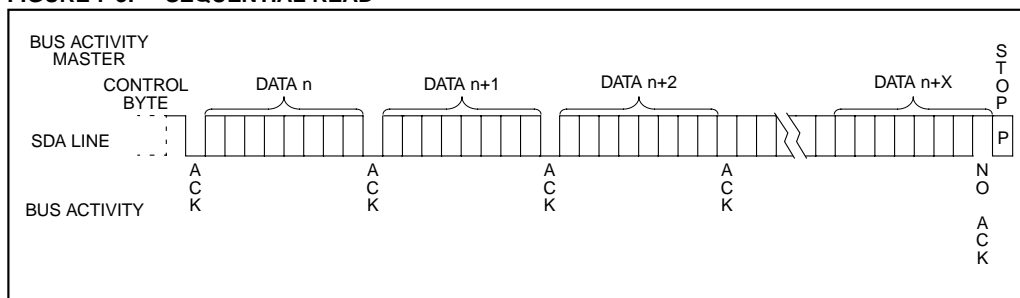
### 7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LCS21A as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The 24LCS21A will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21A discontinues transmission (Figure 7-2).

**FIGURE 7-2: RANDOM READ**



**FIGURE 7-3: SEQUENTIAL READ**



## 7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LCS21A transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LCS21A to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LCS21A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

## 7.4 Noise Protection

The 24LCS21A employs a V<sub>CC</sub> threshold detector circuit which disables the internal erase/write logic if the V<sub>CC</sub> is below 1.5 volts at nominal conditions.

The SDA, SCL and VCLK inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

## 8.0 PIN DESCRIPTIONS

### 8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pullup resistor to V<sub>CC</sub> (typical 10 K $\Omega$  for 100 kHz, 1 K $\Omega$  for 400 kHz).

For normal data transfer in the Bi-directional Mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

### 8.2 SCL

This pin is the clock input for the Bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the Bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

## 8.3 VCLK

This pin is the clock input for the Transmit-Only Mode (DDC1). In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-directional Mode, a high logic level is required on this pin to enable write capability.

## 8.4 WP

This pin is used for flexible write protection of the 24LCS21A. When the last memory location (7Fh) is written with any data, this pin is enabled and determines the write capability of the 24LCS21A (Table 6-1).

The  $\overline{\text{WP}}$  pin has an internal pull up resistor which will allow write capability (assuming VCLK = 1) at all times if this pin is floated.

# 24LCS21A

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NOTES:

## 24LCS21A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.

|                 |   |           |  |
|-----------------|---|-----------|--|
| <b>24LCS21A</b> | - | <b>/P</b> |  |
|                 |   |           | <b>Package:</b>  |
|                 |   |           | P = Plastic DIP (300 mil Body), 8-lead                             |
|                 |   |           | SN = Plastic SOIC (150 mil Body), 8-lead                           |
|                 |   |           | <b>Temperature</b>   |
|                 |   |           | Blank = 0°C to +70°C   |
|                 |   |           | <b>Range:</b>  |
|                 |   |           | I = -40°C to +85°C   |
|                 |   |           | <b>Device:</b>   |
|                 |   |           | 24LCS21A Dual Mode I <sup>2</sup> C Serial EEPROM                  |
|                 |   |           | 24LCS21AT Dual Mode I <sup>2</sup> C Serial EEPROM (Tape and Reel) |

## Sales and Support

### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site ([www.microchip.com](http://www.microchip.com))

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6/11/98



*Microchip received ISO 9001 Quality System certification for its worldwide headquarters, design, and wafer fabrication facilities in January, 1997. Our field-programmable PICmicro™ 8-bit MCUs, Serial EEPROMs, related specialty memory products and development systems conform to the stringent quality standards of the International Standard Organization (ISO).*

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