MICROCHIP

Product Reliability

OVERVIEW

Microchip Technology Inc.'s products provide competitive leadership in quality and reliability, with demonstrated performance of less than 100 FITs (Failures in Time) operating life for most products. The designed-in reliability of Microchip's products are supported by ongoing reliability data monitors. This document presents current data for your use - to provide you with results you can count on.

The test descriptions included in this document explain Microchip's quality and reliability system. The product data demonstrates its results.

The customer's quality requirements are Microchip's top priority. Ongoing customer feedback and device performance monitoring drive Microchip, leading to continuing improvements in the long-term quality and reliability.

FAILURE RATE CALCULATION

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip Technology agree closely with those published in the literature. For complex CMOS devices in production at Microchip Technology, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. This activation energy also applies to some of our retention bake failures, though most are 1.2eV. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55˚C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink, or air flow by convection is used.

Environment	Typical Failure Mechanism
Operating Life	Process parameter drift/shift Metal electromigration Internal leakage path Lifted bond/ball bond chip-out
Temperature Cycle	Lifted bond/ball chip-out Cracked die or surface cracks Bond pad corrosion
Autoclave	Inter-pin leakage Charge loss
High Temp. Bake	Charge loss
High Temp. Reverse Bias	Charge gain, Parameter drift/shift

DEFINITIONS

FIT (Failure In Time): Expresses the estimated field failure rate in number of failures per billion power-on device-hours. 100 FITS equals 0.01% fail per 1,000 device-hours.

Operating Life Test: The device is dynamically exercised at a high ambient temperature (usually 125˚C) to quickly simulate field life. Derating from high temperature, an ambient use condition failure rate can be calculated.

Temperature Cycle: The devices are exposed to severe extremes of temperature in an alternating fashion (-65˚C for 15 minutes, 150˚C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

Autoclave (pressure cooker): Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121˚C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Thermal Shock: Exposes devices to extreme temperatures from -55˚C to +125˚C by alternate immersion in liquid media.

Retention Bake: A 150˚C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

HAST: Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 Volts and ground on alternating pins.

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system ensures that released products are designed, processed, packaged and tested to meet both design functionality and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability.

RELIABILITY DATA SUMMARY

Introduction

This section provides a reliability summary of Microchip Technology's product. Included is reliability data and packaging information obtained over the recent past.

Plastic Package Characteristics and Codes

As part of an on going product program, Microchip Technology will apply its Quality and Reliability process in evaluating the latest developments in plastic packaging technology, and implement the highest reliability materials and assembly techniques. The plastic packages that are currently available from Microchip are listed in the table below.

Package Description Identification Code

Package Description	Identification Code
Plastic Leadless Chip Carrier	L
Plastic Dual In Line (600)	P
Plastic Dual In Line (300)	SP
Plastic SOIC (.150)	SL/SN
Plastic SOIC (.207)	SM
Plastic SOIC (.300)	SO
Plastic TSOP (8 x 20mm)	TS
Plastic SSOP (.207)	SS

FIGURE 1: RELIABILITY CONTROL SYSTEM DIAGRAM

DESIGN AND DEVELOPMENT → QUALIFICATION → RELIABILITY CONTROL

DESIGN AND DEVELOPMENT

Specify:

- Design objectives/specifications
- Testability goals
- Reliability requirements
- Process/packaging requirements
- Design guidelines

Design:

- Functional models
- Logic design & verification
- Circuit design & verification
- Layout design & verification
- Prototype verification
- Performance characterization

Develop (as required):

- Wafer fabrication processes
- Package/packaging technology

QUALIFICATION

Confirm design objectives using qualification tests:

- Operating life, 125°C ambient
- Temp-cycle, -65°/150°C
- Thermal shock, -65°/150˚C
- ESD, ± 4000 V HBM
- ESD, ± 400 V MM
- Latch-up (CMOS devices)
- Autoclave (pressure cooker) retention bake

RELIABILITY CONTROL

Assure Outgoing Quality Level:

- Design release document
- Baseline wafer fabrication process
- Baseline assembly process
- Qualification release
- Enter device to specification system
- Wafer-level reliability controls
- Assembly reliability controls
- Early failure rate sampling
- Reliability monitoring
- Statistical process control feedback
- Audit specifications
- Analyze returned failures
- Requalify devices as needed for major changes such as ESD resistance enhancement, cost reduction/die shrink, process improvement, and new package types.

HIGH TEMPERATURE (125˚C) DYNAMIC LIFE TEST

Graph set for EEPROM, PIC16/17 and EPROM for all conditions

High temperature dynamic life testing accelerates random failure modes which would occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems.

FIGURE 2: EEPROM DYNAMIC LIFE

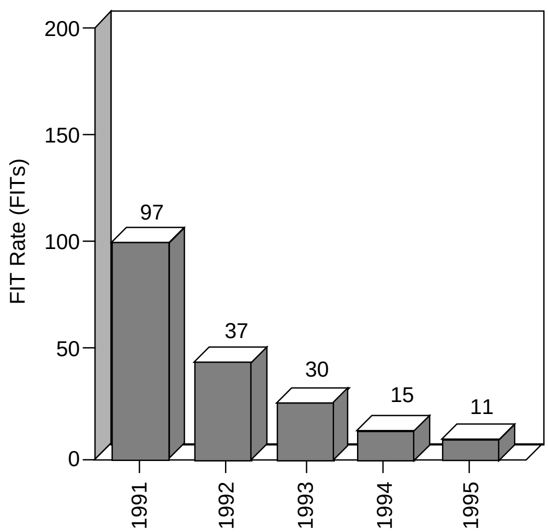


FIGURE 3: EPROM DYNAMIC LIFE

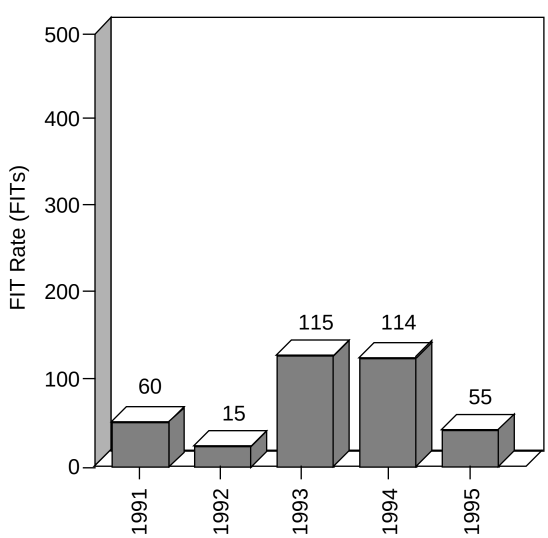
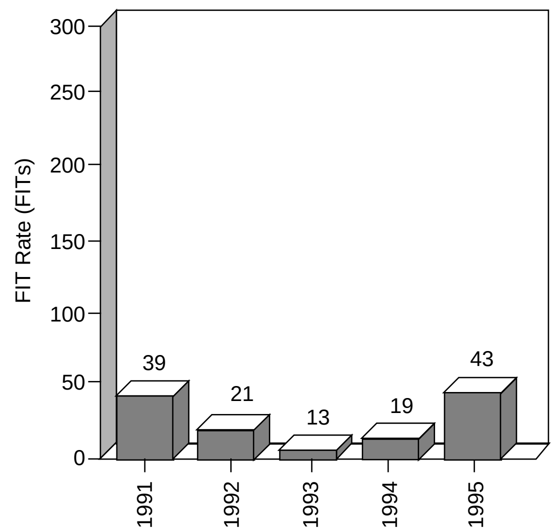


FIGURE 4: PIC16/17 MICROCONTROLLER DYNAMIC LIFE



DATA RETENTION BAKE

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of zeroes to ones. In order to evaluate the level of this type of failure, devices are subjected to a 150˚C bake. This bake accelerates charge loss in the memory cell and 168 hours at 150°C is equivalent to greater than 250 years in the field at 55°C.

FIGURE 5: EEPROM RETENTION BAKE

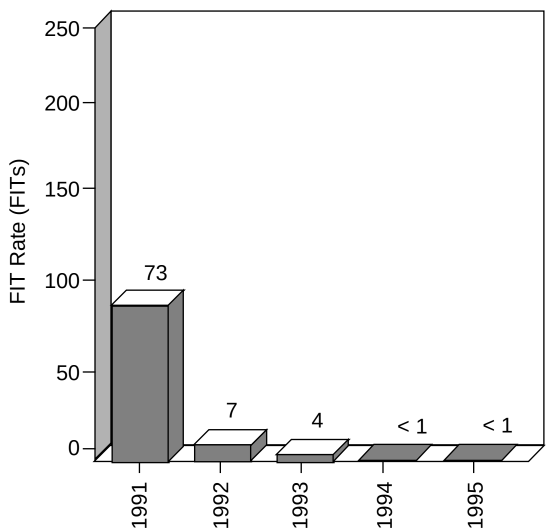


FIGURE 6: EPROM RETENTION BAKE

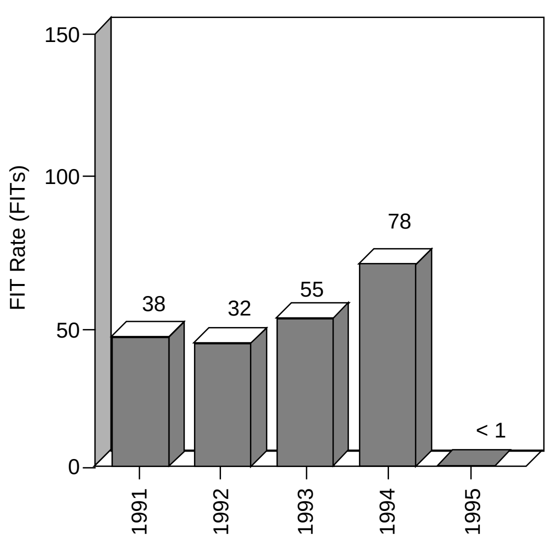
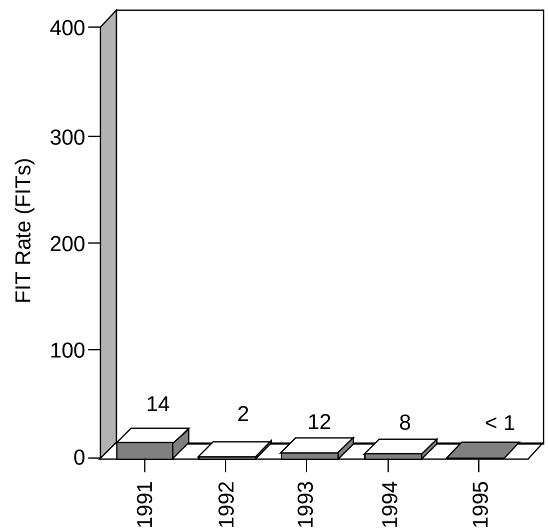


FIGURE 7: PIC16/17 MICROCONTROLLER RETENTION BAKE



NOTE: Representation of reliability data typically shows calendar year grouping along the x-axis, except for 1993 which includes only first, second and third quarters. This provides the equal time interval normally expected for graphical presentation. However, Chi-square statistics demand equivalent device-hours for fair interval comparison. Such data grouping assures that relatively small sample sizes do not indicate unrepresentative FIT rates.

PCT (AUTOCLAVE)

Originally, this test was designed to evaluate corrosion of bond pads due to penetrating moisture combining with contaminant residue on the metal surface. The corrosion failure rate for this test has become nearly zero and a new failure mode has surfaced. This is memory cell charge loss due to moisture penetration along the floating gate allowing a conduction path for removal of stored charge. This moisture path is between the seal of the metal and the passivation which can then be traced to the substrate near the edge of the floating gate. This failure type is the primary mode in the data provided.

Operating Hours		
Package	**24**	**168**
PDIP	0/1334	0/1334
PLCC	0/1014	7/1014
SOIC	0/2439	0/2439
TSOP	0/192	0/192

PCT Failure Modes:
1 unit of 32L PLCC (27C256) failed due to lifted ball bonds.
5 units of 32L PLCC (27C256) failed due to lifted ball bonds.
1 unit of 32L PLCC (27C256) failed due to a leaky oxide causing single bit charge loss.

TEMPERATURE CYCLING

This thermal tests evaluates air to air rapid temperature change evaluating built in material stresses. This is a worst case simulation of system power up/power down and is based on stringent military packaging requirements.

Operating Results	
Package	**100 Cycles**
PDIP	0/364
PLCC	0/188
SOIC	0/964
TSOP	0/30
SSOP	0/60
VSOP	2/20

TC Failure Modes:
2 units of 28L VSOP (28C64A) failed due to lifted ball bonds.

THERMAL SHOCK

Thermal shock is the most extreme case of temperature cycling by using liquid immersion for the technique to change the device environment. This accelerates any stress related failures with the rapidly changing gradient. After the temperature stressing a constant force centrifuge test is also preformed prior to final electrical testing to further uncover any defects that may have occurred under stress.

Operating Results	
Package	**100 Cycles**
PDIP	0/354
PLCC	0/132
SOIC	0/872
TSOP	0/30
SSOP	0/60
VSOP	2/66

TS Failure Modes:
2 units of 28L VSOP (28C64A) failed due to oxide defects.

HAST (130°/85% R.H.)

Highly Accelerated Stress Testing evaluates plastic encapsulated devices' ability to withstand extreme high temperature, high humidity environments while under electrical bias. This is done by a new method known as HAST. This stress is designed to create corrosion of the metal or internal device leakage if ionic contaminants are present but also may cause charge loss in memory cells.

Operating Results		
Package	**48 Hours**	**168 Hours**
PDIP	0/969	1/969
PLCC	0/477	0/477
SOIC	8/2572	0/2482
TSOP	0/150	0/149

HAST Failure Modes:
8 units of 18L SOIC (PIC16CR54) failed due to high static Idd.
1 unit of 8L PDIP (24LC65) failed due to single bit charge loss.

PRODUCT RELIABILITY DATA

CMOS PIC16/17						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hours	FITS 60% CL@55°C
PIC16C54	DLT	1/2281	1/1028	2	1,246,728	60
PIC16C54A	DLT	1/1520	3/760	4	893,760	75
PIC16C55	DLT	3/1474	0/710	3	844,032	119
PIC16C56	DLT	0/2286	0/1028	0	1,247,568	18
PIC16C57	DLT	0/1865	0/868	0	1,042,440	21
PIC16C58A	DLT	1/2670	0/720	1	1,053,360	25
PIC16C64	DLT	3/774	1/324	4	402,192	168
PIC16C71	DLT	0/1521	0/756	0	890,568	25
PIC16C74	DLT	0/405	2/162	2	204,120	196
PIC16C84	DLT	0/1523	1/723	1	863,184	56
PIC17C42	DLT	1/767	0/370	1	439,656	59
PIC17C44	DLT	0/342	0/162	0	193,536	61
PIC16C54	BAKE	1/2915	0/585	1	981,120	18
PIC16C54A	BAKE	0/1874	0/390	0	642,432	< 1
PIC16C55	BAKE	0/1869	0/382	0	634,872	12
PIC16C56	BAKE	3/2901	0/580	3	974,568	37
PIC16C57	BAKE	1/2312	1/464	2	778,176	34
PIC16C58A	BAKE	0/1887	0/385	0	640,416	< 1
PIC16C64	BAKE	0/950	0/190	0	319,200	< 1
PIC16C71	BAKE	0/1852	0/385	0	634,536	12
PIC16C74	BAKE	0/481	0/95	0	160,608	< 1
PIC16C84	BAKE	0/1392	0/295	0	481,656	< 1
PIC17C42	BAKE	0/928	0/190	0	315,504	< 1
PIC17C44	BAKE	0/438	0/99	0	156,744	< 1

Failure Modes - Dynamic Life:

1 unit of PIC16C58A failed static Idd.
3 units of PIC16C55 failed due to mishandling exacerbated by thermal stress.
1 unit of PIC16C54A failed dynamic Idd due to oxide defects.
2 units of PIC16C65/74 failed due to poor programming margin.
3 units of PIC16C64 failed for fuse charge gain.
1 unit of PIC16C64 had a column fail.
1 unit of PIC17C42 failed due to single bit charge loss.
1 unit of PIC16C84 failed continuity at high temperature.
1 unit of PIC16C54 failed due to high Idd standby.
1 unit of PIC16C54 failed leakage due to wire sweep.
3 units of PIC16C54A failed dynamic Idd.

Failure Modes - Retention Bake:

2 units of PIC16C56 failed single/double bits due to metal shorting the floating gates to ground.
2 units of PIC16C57 failed due to single bit charge loss.
1 units of PIC16C54 failed due to single bit charge loss.
1 units of PIC16C56 failed due to single bit charge loss.

EEPROM						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hours	FITS 60% CL@55°C
24C01A/02A	DLT	0/2297	0/880	0	1,125,096	29
24C04	DLT	0/1530	0/842	0	964,320	20
93C06/46	DLT	0/1147	0/459	0	578,256	23
93LC46	DLT	0/2681	0/1078	0	1,355,928	38
93LC56/66	DLT	0/3447	0/1609	0	1,930,656	16
93LCS56/66	DLT	0/383	0/160	0	198,744	11
24LC01B	DLT	1/1915	0/779	1	976,080	29
24LC02B	DLT	0/2297	3/925	3	1,162,896	50
24LC04B	DLT	0/1519	0/612	0	769,272	86
24LC08B	DLT	0/1915	0/767	0	966,000	29
24LC16B	DLT	0/1915	0/767	0	966,000	23
24LC65	DLT	0/1149	0/688	0	770,952	23
24C01A/02A	BAKE	0/2320	0/480	0	792,960	< 1
24C04	BAKE	0/1392	0/285	0	473,256	< 1
93C06/46	BAKE	0/0	0/0	0	0	NA
93LC46	BAKE	1/2316	0/474	1	787,248	< 1
93LC56/66	BAKE	0/3712	0/765	0	1,266,216	< 1
93LCS56/66	BAKE	0/0	0/0	0	0	NA
24LC01B	BAKE	0/2320	0/480	0	792,960	< 1
24LC02B	BAKE	0/2320	0/494	0	804,720	< 1
24LC04B	BAKE	0/1856	0/380	0	631,008	< 1
24LC08B	BAKE	0/2336	0/500	0	812,448	< 1
24LC16B	BAKE	0/2320	0/475	0	788,760	< 1
24LC65	BAKE	2/928	0/195	2	319,704	< 1

Failure Modes - Dynamic Life:

1 unit of 24LC01B failed leakage on the SDA pin.
3 units of 24LC02B failed due to high standby current.

Failure Modes - Retention Bake:

1 unit of 93LC46 failed to program.
2 units of 24LC65 failed for single bit charge loss.

EPROM						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hours	FITS 60% CL@55°C
27C256	DLT	4/5360	0/2291	4	2,824,920	44
27C512A	DLT	1/2310	5/929	6	1,168,440	81
27C256	BAKE	1/6496	0/1235	1	2,128,728	< 1
27C512A	BAKE	0/2771	0/570	0	944,328	< 1

Failure Modes - Dynamic Life:

2 units of 27C512A failed for single bit charge loss due to a hole in the oxide.
4 units of 27C512A failed for leadage due to a hole in the oxide.
4 units of 27C256 failed due to marginal Vih.

Failure Modes - Retention Bake:

1 unit of 27C256 failed due to an oxide defect in the 1st gate oxide.

Operation Legend: DLT - Dynamic Life Test (125°C) Bake -Retention Bake (150°C)

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