1996 Annual Reliability Report (compiled 7/97)

INTRODUCTION

"Quality Comes First"

By adhering to this guiding value, Microchip Technology Inc. has achieved competitive leadership in quality and reliability for its products. Demonstrated performance levels of less than 100 Failures in Time (FITS) for most products have been realized through the design-in of reliability and continued use of reliability monitors.

This report details Microchip's quality and reliability systems as well as presenting data on the results of these systems. It includes the following:

- Reliability Control System
- Failure Calculation Methodology
- Reliability Test Descriptions
- 1996 Product Reliability

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system is employed to ensure that released products are designed, processed, packaged, and tested to meet both design functionality and reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability. The system is diagrammed in Table 1.

TABLE 1: RELIABILITY CONTROL SYSTEM DIAGRAM

DESIGN AND DEVELOPMENT	QUALIFICATION	RELIABILITY CONTROL
Specify: • Design objectives/ specifications • Testability goals • Reliability requirements • Process/packaging requirements • Design guidelines **Design:** • Functional models • Logic design and verification • Circuit design and verification • Layout design and verification • Prototype verification • Performance characterization **Develop (as required):** • Wafer fabrication processes • Package/packaging technology	**Confirm Design Objectives Using Qualification Tests:** • Dynamic life, 125°C ambient • Temp-cycle, -65°/150°C • Thermal shock, -55°/125°C • ESD, ± 4000 volts HBM • ESD, ±400 volts MM • Latch-up (CMOS devices) • HAST 130°C/85% RH • Autoclave (pressure cooker) • Retention bake	**Assure Outgoing Quality Level:** • Design release document • Baseline wafer fabrication process • Baseline assembly process • Qualification release • Enter device to specification system • Wafer-level reliability controls • Assembly reliability controls • Early failure rate sampling • Reliability monitoring • Statistical process control feedback • Audit specifications • Analyze returned failures • Requalify devices as needed for major changes such as ESD resistance enhancement, cost reduction/die shrink, process improvement and new package types

FAILURE RATE CALCULATION

FIT (Failure in Time): Expresses the estimated field failure rate in number of failures per billion device hours. 100 FITS equals 0.01% fail per 1,000 device hours.

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius Equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip agree closely with those published in the literature. For complex CMOS devices in production at Microchip, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink or air flow by convection is used.

Environment	Attribute Tested
Operating Life	Process parameter drift/shift
	Metal electromigration
	Internal leakage path
	Data retention
	Bond/ball bond integrity
Temperature Cycle	Bond/ball integrity
	Die or surface integrity
	Bond pad integrity
HAST	Internal device leakage
	Corrosion resistance
PCT	Inter-pin leakage
	Data retention
	Corrosion resistance
High Temp. Bake	Data retention

RELIABILITY TEST DESCRIPTIONS

High Temperature (125°C) Dynamic Life Test

High temperature dynamic life testing accelerates random failure modes which could occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems. The voltage maintained during the tests is at or near the maximum data sheet voltage supply. Derating from high temperature, an ambient use condition failure rate can be calculated. The extrapolation of data for FIT rate purposes of this test does not include electrical acceleration.

Temperature Cycle

The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 15 minutes, 150°C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

PCT (Pressure Cooker or Autoclave)

Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Originally, this test was designed to evaluate corrosion of bond pads due to penetrating moisture combining with contaminant residue on the metal surface. The corrosion failure rate for this test has become nearly zero and a new failure mode has surfaced. This is memory cell charge loss due to moisture penetration along the floating gate allowing a conduction path for removal of stored charge. This moisture path is between the seal of the metal and the passivation which can then be traced to the substrate near the edge of the floating gate.

Thermal Shock

Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media. This is a sudden temperature change, as opposed to the gradual change in the Temperature Cycling test. Otherwise, it induces the same stresses as Temperature Cycling.

Data Retention Bake

A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of data states. In order to evaluate the level of this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell and 1000 hours at 150°C is equivalent to greater than 10 years in the field at 55°C.

Highly Accelerated Stress Test (HAST)

Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 Volts and ground on alternating pins.

Erase/Write Endurance of EEPROMs

Measurement of Cycling

Microchip defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. An endurance failure is determined when any one bit in the array is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices (Microchip currently uses a cumulative 2.5 percent) have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from every wafer lot of material manufactured for shipment. Samples are subjected to byte cycling of a checkerboard pattern at 85°C in rapid succession to the specified number of guaranteed cycles. These units then are baked at 150°C for 48 hours in both checkerboard and inverse checkerboard states and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a monthly basis and reviewed to measure both results of continuous improvement programs and conformance to the device standards.

Endurance Variables

a) **Temperature:** Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b) **Delay Between Cycles:** This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies, this does have a positive effect; however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c) **Write Timing:** The decrease in write time to the device correlates directly with the write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.

> **Note:** The rise time of the signal, which the customer does not have control over, is also a dominant effect.

d) **Vcc Voltage:** The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.
Lower voltages have the opposite effect on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at V_{CC} = 5.5 Volts.

e) **Pattern Effect:** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a non-volatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric.

> **Note:** To write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to its original state!

Conversely writing a one from a one then passes no charge through the cell and, therefore, does no damage to the cell but does stress the charge pump.
From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles of an all zero patterned device. In general, this appears to be approximately correct but does neglect the charge pump and other peripheral wear-out mechanisms.

f) **Cycling Mode:** Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field as well as the method of monitoring that has been chosen internally. This is to best estimate field lifetime expectations and actual failure rates. A second technique exists called block mode which exercises all the cells of the array simultaneously. The failure rates of byte cycled devices are approximately two times the failure rates of block cycled devices according to experimental test data. This effect has been traced back to the rise time of the programming

signal at the memory cell. The faster this voltage rise occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/ capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate.

g) **Array Size:** This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are, therefore, not directly related to array size.

Field Results

After significant experimentation, Microchip has developed a model of the endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called Total Endurance™. The Total Endurance Software Model allows the customer to bypass confusing information and conditions other than their application and directly predict the failure rate in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system.

RELIABILITY DATA SUMMARY

This section provides a reliability summary of Microchip's product. Included is reliability data and packaging information obtained during 1996.

SUMMARY OF RELIABILITY – 1996 ANNUAL REPORT DEVICE DATA

I. DYNAMIC LIFE/ RETENTION BAKE

Dynamic Life

Stress Temperature:	125°C	Activation Energy:	0.6	eV	57K, 77K
Derated Temperature:	55°C	Acceleration Rate:	42		
		Activation Energy:	0.7	eV	90K
		Acceleration Rate:	78		

Retention Bake

Stress Temperature:	150°C	Activation Energy:	0.6	eV	57K EPROM
Derated Temperature:	55°C	Acceleration Rate:	117		
		Activation Energy:	1.2	eV	57K EE, 77K,
		Acceleration Rate:	13718		& 90K

Microcontrollers					Fit Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Term Life**	**Total Life**
ALL PICs	Dynamic Life	7/10758	2/5063	9	6,060,264	83	13	31
	Retention Bake	4/14993	1/2980	5	5,022,024	<1	<1	<1
ALL 90K PICs	Dynamic Life	1/4328	1/2002	2	2,408,784	36	15	17
	Retention Bake	3/6490	0/1304	3	2,185,680	<1	<1	<1
ALL 57K PICs	Dynamic Life	6/6430	1/3061	7	3,651,480	163	19	55
	Retention Bake	1/8503	1/1676	2	2,836,344	<1	1	<1
PIC16C84	Dynamic Life	0/831	0/377	0	456,288	157	69	48
	Retention Bake	0/1763	0/300	0	548,184	<1	<1	<1
PIC16C74	Dynamic Life	0/842	0/324	0	413,616	83	43	29
	Retention Bake	0/707	0/198	0	285,096	1	<1	<1
PIC16C71	Dynamic Life	2/1537	0/760	2	896,616	288	34	83
	Retention Bake	0/1387	1/300	1	485,016	34	69	36
PIC16C64	Dynamic Life	0/374	0/162	0	198,912	188	87	59
	Retention Bake	0/995	0/199	0	334,320	<1	<1	<1
PIC16C58A	Dynamic Life	0/1207	0/569	0	680,736	58	25	17
	Retention Bake	1/1531	0/300	1	509,208	1	<1	<1
PIC16C57	Dynamic Life	1/640	1/393	2	437,640	451	147	170
	Retention Bake	0/1047	0/216	0	357,336	44	43	22

Microcontrollers					Fit Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Term Life**	**Total Life**
PIC16C56	Dynamic Life	1/1257	0/568	1	688,296	230	46	70
	Retention Bake	0/1710	0/300	0	539,280	27	31	15
PIC16C55	Dynamic Life	0/770	0/393	0	459,480	170	67	48
	Retention Bake	1/1056	0/260	1	395,808	97	36	44
PIC16C54	Dynamic Life	2/1395	0/570	2	713,160	318	46	104
	Retention Bake	0/1540	0/300	0	510,720	30	31	15
PIC16C54A	Dynamic Life	1/1395	0/570	1	713,160	111	25	37
	Retention Bake	1/1822	0/300	1	558,096	<1	<1	<1
PIC17C44	Dynamic Life	0/510	1/377	1	402,360	138	82	65
	Retention Bake	1/1435	0/307	1	498,960	1	<1	<1
Failure Modes:	Dynamic Life	1 unit of PIC16C57 failed due to wire sweep						
		1 unit of PIC16C57 failed due to leakage						
		2 units of PIC16C71 failed due to high I_{DD} dynamic						
		1 unit of PIC16C56 failed due to single bit charge gain						
		1 unit of PIC16C54 failed due to high I_{DD} dynamic						
		1 unit of PIC16C54 failed functionality						
		1 unit of PIC16C54A failed due to high I_{DD} dynamic						
		1 unit of PIC17C44 failed due to single bit charge loss						
	Retention Bake	1 unit of PIC16C58A failed to execute test program (functionality)						
		1 unit of PIC16C55 failed due to a poly short						
		1 unit of PIC16C54A failed due to mechanical damage						
		1 unit of PIC17C44 failed due to low fuse programming margin						
		1 unit of PIC16C71 failed functionality						

Serial EEPROMS					Fit Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Term Life**	**Total Life**
ALL SERIAL	Dynamic Life	31/16019	0/6549	31	8,192,352	295	4	97
EEPROMs	Retention Bake	15/19311	6/4100	21	6,688,248	<1	<1	<1
57K SERIAL	Dynamic Life	0/3531	0/1440	0	1,802,808	37	18	12
EEPROMs	Retention Bake	0/4290	0/900	0	1,476,720	<1	<1	<1
77K SERIAL	Dynamic Life	31/12488	0/5109	31	6,389,544	378	5	124
EEPROMs	Retention Bake	15/15021	6/3200	21	5,211,528	<1	<1	<1
24C01A/02A	Dynamic Life	0/1960	0/800	0	1,001,280	67	33	22
	Retention Bake	0/2375	0/500	0	819,000	<1	<1	<1
24C04	Dynamic Life	0/1571	0/640	0	801,528	83	41	27
	Retention Bake	0/1915	0/400	0	657,720	<1	<1	<1
93LC46B	Dynamic Life	2/1930	0/800	2	996,240	230	33	75
	Retention Bake	0/2332	0/500	0	811,776	<1	<1	<1
93LC56B/66B	Dynamic Life	0/1966	0/800	0	1,002,288	67	33	22
	Retention Bake	0/1856	0/400	0	647,808	<1	<1	<1
93LCS56/66	Dynamic Life	0/801	0/320	0	403,368	163	82	55
	Retention Bake	2/1376	0/300	2	483,168	1	<1	<1
24LC01B	Dynamic Life	0/1169	0/480	0	599,592	112	55	37
	Retention Bake	0/1392	0/300	0	485,856	<1	<1	<1
24LC02B	Dynamic Life	0/1553	0/629	0	789,264	84	42	28
	Retention Bake	0/1881	0/400	0	652,008	<1	<1	<1
24LC04B	Dynamic Life	0/1553	0/640	0	798,504	84	41	28
	Retention Bake	0/1904	0/400	0	655,872	<1	<1	<1
24LC08B	Dynamic Life	3/1955	0/800	3	1,000,440	305	33	100
	Retention Bake	0/2384	0/500	0	820,512	<1	<1	<1
24LC16B	Dynamic Life	0/785	0/320	0	400,680	167	82	55
	Retention Bake	0/968	0/200	0	330,624	<1	<1	<1
24LC65	Dynamic Life	26/776	0/320	26	399,168	5146	82	1681
	Retention Bake	13/928	6/200	19	323,904	7	3	5
Failure Modes:	Dynamic Life	1 unit of 24LC08B failed due to high I_{DDS}						
		1 unit of 24LC08B failed due to a timing problem						
		1 unit of 24LC08B failed due to mechanical stress						
		2 units of 93LC46B failed functionality						
		26 units of 24LC65 failed due to single bit charge loss*						
	Retention Bake	2 units of 93LCS56/66 failed to program						
		19 units of 24LC65 failed due to single bit charge loss*						

* Root cause failure analysis determined 24LC65 failures were due to an error embedded in a wafer sort test program. Corrective actions were implemented which have eliminated this problem. Without the 26 DLT fails and 19 Retention Bake fails, the numbers would be:

		Infant Mortality	**Long**	**Total Life**
ALL SERIAL EEPROMS	Dynamic Life	55	4	18
	Retention Bake	<1	<1	<1
77K SERIAL EEPROMs	Dynamic Life	70	5	23
	Retention Bake	<1	<1	<1
24LC65	Dynamic Life	113	82	47
	Retention Bake	<1	3	1

Parallel EPROMs					Fit Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Term Life**	**Total Life**
ALL PARALLEL	Dynamic Life	1/1979	0/800	1	1,004,472	146	33	48
EEPROMs	Retention Bake	0/2368	0/500	0	817,824	<1	<1	<1
28C64A	Dynamic Life	1/1979	0/800	1	1,004,472	146	33	48
	Retention Bake	0/2368	0/500	0	817,824	<1	<1	<1
Failure Modes:	Dynamic Life	1 unit of 28C64A failed programming						
	Retention Bake	N/A						

EPROMs					Fit Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Term Life**	**Total Life**
ALL EPROMs	Dynamic Life	15/5843	1/2400	16	2,997,624	305	18	106
	Retention Bake	17/6962	0/1500	17	2,429,61”	1	<1	1
ALL 90K	Dynamic Life	13/2316	0/960	13	1,195,488	486	15	158
EPROMs	Retention Bake	13/2772	0/600	13	969,696	2	<1	1
ALL 77K	Dynamic Life	2/3527	1/1440	3	1,802,136	126	40	56
EPROMs	Retention Bake	4/4190	0/900	4	1,459,920	1	<1	<1
27C256	Dynamic Life	2/3527	1/1440	3	1,802,136	126	40	56
	Retention Bake	4/4190	0/900	4	1,459,920	1	<1	<1
27C512A	Dynamic Life	13/2316	0/960	13	1,195,488	486	15	158
	Retention Bake	13/2772	0/600	13	“969,696”	2	<1	1
Failure Modes:	Dynamic Life	3 units of 27C256 failed due to single bit charge loss						
		1 unit of 27C512A failed due to single bit charge gain						
		1 unit of 27C512A failed due row fails						
		11 units of 27C512A failed due to single bit charge loss						
	Retention Bake	1 unit of 27C256 failed due to leakage						
		1 unit of 27C256 failed due to a resistive short						
		2 units of 27C256 failed due to single bit charge loss						
		13 units of 27C512A failed due to single bit charge loss						

II. PRESSURE COOKER, HAST, TEMPERATURE CYCLE, AND THERMAL SHOCK PACKAGE DATA SUMMARY

Pressure Cooker

Stress Temperature: 121.5°C
Derated Temperature: 55°C

HAST

Stress Temperature: 130°C
Derated Temperature: 55°C

Operation	Package	24 Hrs.	168 Hrs.	Fails	Device Hrs.	% Fails per 1000 Hrs.
Pressure Cooker	ALL PACKAGES	0/21643	17/21634	17	3,634,728	0.49
Pressure Cooker	MQFP	0/1279	1/1278	1	214,728	0.78
Pressure Cooker	PDIP	0/3774	0/3774	0	634,032	0.11
Pressure Cooker	PLCC	0/3500	5/3500	5	588,000	0.96
Pressure Cooker	SOIC	0/12521	11/12516	11	2,102,808	0.56
Pressure Cooker	TSOP	0/569	0/566	0	95,160	0.73
Failure Modes:	1 unit of 44L MQFP (PIC16C74) failed due to corrosion					
	1 unit of 32L PLCC (27C512A) failed due to bond pad corrosion/cratering					
	1 unit of 44L PLCC (PIC16C74A) failed due to a faulty contact					
	3 units of 32L PLCC (27C256) had single bit fails due to assembly					
	2 units of 8L SOIC (24LC02B) failed due to moisture in the package					
	6 units of 28L SOIC (PIC16C57) failed due to moisture in the package					
	2 units of 28L SOIC (28C64A) failed due to corrosion					
	1 unit of 8L SOIC (24LC02B) failed due to high I_{DD} standby					

Operation	Package	48 Hrs.	168 Hrs.	Fails	Device Hrs.	% Fails per 1000 Hrs.
HAST	ALL PACKAGES	2/13506	21/13354	23	2,250,768	1.05
HAST	MQFP	0/574	0/567	0	95,424	0.73
HAST	PDIP	0/2676	11/2668	11	448,608	2.60
HAST	PLCC	0/2275	0/2245	0	378,600	0.18
HAST	SOIC	0/7646	1/7549	1	1,272,888	0.13
HAST	TSOP	2/335	9/325	11	55,080	21.20
Failure Modes:	11 units of 18L PDIP (PIC16CR54) failed due to moisture in the package					
	1 unit of 18L SOIC (PIC16CR54) failed to read correctly					
	9 units of 28L TSOP (28C16A) failed due to corrosion					
	1 unit of 28L TSOP (28C16A) failed high I_{DD} standby					
	1 unit of 28L TSOP (28C16A) failed write timer fuse					

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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602-786-7200 Fax: 602-786-7277
Technical Support: 602 786-7627
Web: http://www.microchip.com

Atlanta

Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508-480-9990 Fax: 508-480-8575

Chicago

Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972-991-7177 Fax: 972-991-8588

Dayton

Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Los Angeles

Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714-263-1888 Fax: 714-263-1338

New York

Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 516-273-5305 Fax: 516-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong

Microchip Asia Pacific
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

India

Microchip Technology Inc.
No. 6, Legacy, Convent Road
Bangalore 560 025, India
Tel: 91-80-229-0061 Fax: 91-80-229-0062

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai

Microchip Technology
RM 406 Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hong Qiao District
Shanghai, PRC 200335
Tel: 86-21-6275-5700
Fax: 86 21-6275-5060

Singapore

Microchip Technology Taiwan
Singapore Branch
200 Middle Road
#10-03 Prime Centre
Singapore 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C

Microchip Technology Taiwan
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886-2-717-7175 Fax: 886-2-545-0139

EUROPE

United Kingdom

Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Bourne End, Buckinghamshire SL8 5AJ
Berkshire, England RG41 5TU
Tel: 44-1628-851077 Fax: 44-1628-850259

France

Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Müchen, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-39-6899939 Fax: 39-39-6899883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa 222 Japan
Tel: 81-4-5471- 6166 Fax: 81-4-5471-6122

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