1995 Reliability Report (Published 9/96)

INTRODUCTION

By adhering to this guiding value, Microchip Technology Inc. has achieved competitive leadership in quality and reliability for its products. Demonstrated performance levels of less than 100 Failures in Time (FITS) for most products have been realized through the design-in of reliability and continued use of reliability monitors.

This report details Microchip's quality and reliability systems as well as presenting data on the results of these systems. It includes the following:

- Reliability Control System
- Failure Calculation Methodology
- Reliability Test Descriptions
- 1995 Product Reliability

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system is employed to ensure that released products are designed, processed, packaged and tested to meet both design functionality and performance, and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability. The system is diagrammed in Table 1.

TABLE 1: RELIABILITY CONTROL SYSTEM DIAGRAM

DESIGN AND DEVELOPMENT → QUALIFICATION → RELIABILITY CONTROL

Specify:
- Design objectives/ specifications
- Testability goals
- Reliability requirements
- Process/packaging requirements
- Design guidelines

Design:
- Functional models
- Logic design and verification
- Circuit design and verification
- Layout design and verification
- Prototype verification
- Performance characterization

Develop (as required):
- Wafer fabrication processes
- Package/packaging technology

Confirm design objectives using qualification tests:
- Operating life, 125°C ambient
- Temp-cycle, -65°/150°C
- Thermal shock, -65°/150°C
- ESD, ±4000 volts HBM
- ESD, ±400 volts MM
- Latch-up (CMOS devices)
- HAST 130°C/85%
- Autoclave (pressure cooker)
- Retention bake

Assure Outgoing Quality Level:
- Design release document
- Baseline wafer fabrication process
- Baseline assembly process
- Qualification release
- Enter device to specification system
- Wafer-level reliability controls
- Assembly reliability controls
- Early failure rate sampling
- Reliability monitoring
- Statistical process control feedback
- Audit specifications
- Analyze returned failures
- Requalify devices as needed for major changes such as ESD resistance enhancement, cost reduction/die shrink, process improvement and new package types

FAILURE RATE CALCULATION

FIT (Failure in Time): Expresses the estimated field failure rate in number of failures per billion device hours. 100 FITS equals 0.01% fail per 1,000 device hours.

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius Equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip agree closely with those published in the literature. For complex CMOS devices in production at Microchip, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink or air flow by convection is used.

Environment	Attribute Tested
Operating Life	Process parameter drift/shift
	Metal electromigration
	Internal leakage path
	Data retention
	Bond/ball bond integrity
Temperature Cycle	Bond/ball integrity
	Die or surface integrity
	Bond pad integrity
HAST	Internal device leakage
	Corrosion resistance
PCT	Inter-pin leakage
	Data retention
	Corrosion resistance
High Temp. Bake	Data retention

RELIABILITY TEST DESCRIPTIONS

High Temperature (125°C) Dynamic Life Test

High temperature dynamic life testing accelerates random failure modes which could occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems. The voltage maintained during the tests is at or near the maximum data sheet voltage supply. Derating from high temperature, an ambient use condition failure rate can be calculated. The extrapolation of data for FIT rate purposes of this test does not include electrical acceleration.

Temperature Cycle

The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 15 minutes, 150°C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

PCT (Pressure Cooker or Autoclave)

Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Originally, this test was designed to evaluate corrosion of bond pads due to penetrating moisture combining with contaminant residue on the metal surface. The corrosion failure rate for this test has become nearly zero and a new failure mode has surfaced. This is memory cell charge loss due to moisture penetration along the floating gate allowing a conduction path for removal of stored charge. This moisture path is between the seal of the metal and the passivation which can then be traced to the substrate near the edge of the floating gate.

Thermal Shock

Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media. This is a sudden temperature change, as opposed to the gradual change in the Temperature Cycling test. Otherwise, it induces the same stresses as Temperature Cycling.

Data Retention Bake

A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of data states. In order to evaluate the level of this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell and 1000 hours at 150°C is equivalent to greater than 10 years in the field at 55°C.

Highly Accelerated Stress Test (HAST)

Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 Volts and ground on alternating pins.

Erase/Write Endurance of EEPROMs

Measurement of Cycling

Microchip defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. An endurance failure is determined when any one bit in the array is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices (Microchip currently uses a cumulative 2.5 percent) have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from every wafer lot of material manufactured for shipment. Samples are subjected to byte cycling of a checkerboard pattern at 85°C in rapid succession to the specified number of guaranteed cycles. These units then are baked at 150°C for 48 hours in both checkerboard and inverse checkerboard states and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a monthly basis and reviewed to measure both results of continuous improvement programs and conformance to the device standards.

Endurance Variables

a) **Temperature:** Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b) **Delay Between Cycles:** This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies, this does have a positive effect; however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c) **Write Timing:** The decrease in write time to the device correlates directly with the write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.

> **Note:** The rise time of the signal, which the customer does not have control over, is also a dominant effect.

d) **Vcc Voltage:** The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.
Lower voltages have the opposite effect on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at V_{CC} = 5.5 Volts.

e) **Pattern Effect:** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a non-volatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric.

> **Note:** To write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to its original state!

Conversely writing a one from a one then passes no charge through the cell and, therefore, does no damage to the cell but does stress the charge pump.
From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles of an all zero patterned device. In general, this appears to be approximately correct but does neglect the charge pump and other peripheral wear-out mechanisms.

f) **Cycling Mode:** Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field as well as the method of monitoring that has been chosen internally. This is to best estimate field lifetime expectations and actual failure rates. A second technique exists called block mode which exercises all the cells of the array simultaneously. The failure rates of byte cycled devices are approximately two times the failure rates of block cycled devices according to experimental test data. This effect has been traced back to the rise time of the programming signal at the memory cell. The faster this voltage rise

occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate.

g) **Array Size:** This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are, therefore, not directly related to array size.

Field Results

After significant experimentation, Microchip has developed a model of the endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called Total Endurance™. The Total Endurance Software Model allows the customer to bypass confusing information and conditions other than their application and directly predict the failure rate in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system.

RELIABILITY DATA SUMMARY

This section provides a reliability summary of Microchip's product. Included is reliability data and packaging information obtained during 1995.

SUMMARY OF RELIABILITY DATA - 1995 ANNUAL REPORT DEVICE DATA

I. DYNAMIC LIFE/RETENTION BAKE

Dynamic Life

Stress Temperature:	125°C	Activation Energy:	0.6	eV	
Derated Temperature:	55°C	Acceleration Rate:	42		

Retention Bake

Stress Temperature:	150°C	Activation Energy:	0.6	eV	(EPROM)
Derated Temperature:	55°C	Acceleration Rate:	117		(EPROM)
		Activation Energy:	1.2	eV	(EEPROM)
		Acceleration Rate:	13718		(EEPROM)

Micrcontrollers **FIT Rates, 60% Confidence Level**

Device	Operation	168 Hrs.	1008 Hrs.	Fails	Device Hrs.	Infant Mortality	Long Term Life	Total Life
PIC16/17's	Dynamic Life	12/17428	8/7611	20	9,321,144	85	28	43
	Retention Bake	5/19799	1/4040	6	6,719,832	<1	<1	<1
PIC16C84	Dynamic Life	0/1523	1/723	1	863,184	86	80	56
	Retention Bake	0/1392	0/295	0	481,656	<1	<1	<1
PIC16C74	Dynamic Life	0/405	2/162	2	204,120	174	294	196
	Retention Bake	0/481	0/95	0	160,608	1	1	<1
PIC16C71	Dynamic Life	0/1521	0/756	0	890,568	86	35	25
	Retention Bake	0/1852	0/385	0	634,536	25	24	12
PIC16C64	Dynamic Life	3/744	1/324	4	402,192	414	96	168
	Retention Bake	0/950	0/190	0	319,200	<1	<1	<1
PIC16C58A	Dynamic Life	1/2670	0/720	1	1,053,360	58	20	25
	Retention Bake	0/1887	0/385	0	640,416	<1	<1	<1
PIC16C57	Dynamic Life	0/1865	0/868	0	1,042,440	70	30	21
	Retention Bake	1/2312	1/464	2	778,176	44	44	34
PIC16C56	Dynamic Life	0/2286	0/1028	0	1,247,568	57	25	18
	Retention Bake	3/2901	0/580	3	974,568	73	16	37
PIC16C55	Dynamic Life	5/1474	0/710	5	844,032	609	37	179
	Retention Bake	0/1869	0/382	0	634,872	25	24	12
PIC16C54	Dynamic Life	1/2281	1/1028	2	1,246,728	127	56	60
	Retention Bake	1/2915	0/585	1	981,120	35	16	18
PIC16C54A	Dynamic Life	1/1520	3/760	4	893,760	102	84	75

Device	Operation	168 Hrs.	1008 Hrs.	Fails	Device Hrs.	Infant Mortality	Long Term Life	Total Life
	Retention Bake	0/1874	0/390	0	642,432	<1	<1	<1
PIC17C42	Dynamic Life	1/767	0/370	1	439,656	202	38	59
	Retention Bake	0/982	0/190	0	315,504	<1	<1	<1
PIC17C44	Dynamic Life	0/342	0/162	0	193,536	205	87	61
	Retention Bake	0/438	0/99	0	156,744	1	1	<1
Failure Modes:	Dynamic Life	1 unit of PIC16C58A failed static I_{DD} 5 units of PIC16C55 failed due to mishandling exacerbated by thermal stress 1 unit of PIC16C54A failed dynamic I_{DD} due to oxide defects 2 units of PIC16C65/74 failed due to poor programming margin 3 units of PIC16C64 failed for fuse charge gain 1 unit of PIC16C64 had a column fail 1 unit of PIC17C42 failed due to single bit charge loss 1 unit of PIC16C84 failed continuity at high temperature 1 unit of PIC16C54 failed due to high I_{DD} standby 1 unit of PIC16C54 failed leakage due to wire sweep 3 units of PIC16C54A failed dynamic I_{DD}						
	Retention Bake	2 units of PIC16C56 failed single/double bits due to metal shorting the floating gates to ground 2 units of PIC16C57 failed due to single bit charge loss 1 unit of PIC16C54 failed due to single bit charge loss 1 unit of PIC16C56 failed due to single bit charge loss						

Serial EEPROMs					FIT Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL SERIAL	Dynamic Life	1/22195	3/9566	4	11,764,200	13	12	11
EEPROMS	Retention Bake	3/21820	0/4528	3	7,469,280	<1	<1	<1
24C01A/02A	Dynamic Life	0/2297	0/880	0	1,125,096	57	30	20
	Retention Bake	0/2320	0/480	0	792,960	<1	<1	<1
24C04	Dynamic Life	0/1530	0/842	0	964,320	86	31	23
	Retention Bake	0/1392	0/285	0	473,256	<1	<1	<1
93C06/46	Dynamic Life	0/1147	0/459	0	578,256	114	57	38
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
93LC46	Dynamic Life	0/2681	0/1078	0	1,355,928	49	24	16
	Retention Bake	1/2316	0/474	1	787,248	<1	<1	<1
93LC56/66	Dynamic Life	0/3447	0/1609	0	1,930,656	38	16	11
	Retention Bake	0/3712	0/765	0	1,266,216	<1	<1	<1
93LCS56/66	Dynamic Life	0/383	0/160	0	198,744	86	43	29
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
24LC01B	Dynamic Life	1/1915	0/799	1	976,080	151	34	50
	Retention Bake	0/2320	0/480	0	792,960	<1	<1	<1
24LC02B	Dynamic Life	0/2297	3/925	3	1,162,896	57	129	86
	Retention Bake	0/2320	0/494	0	804,720	<1	<1	<1
24LC04B	Dynamic Life	0/1519	0/612	0	769,272	86	43	29
	Retention Bake	0/1856	0/380	0	631,008	<1	<1	<1
24LC08B	Dynamic Life	0/1915	0/767	0	966,000	68	34	23
	Retention Bake	0/2336	0/500	0	812,448	<1	<1	<1
24LC16B	Dynamic Life	0/1915	0/767	0	966,000	68	34	23
	Retention Bake	0/2320	0/475	0	788,760	<1	<1	<1
24LC65	Dynamic Life	0/1149	0/688	0	770,952	114	38	29
	Retention Bake	2/928	0/195	2	319,704	1	<1	1
Failure Modes:	Dynamic Life	1 unit of 24LC01B failed leakage on the SDA pin 3 units of 24LC02B failed due to high standby current						
	Retention Bake	1 unit of 93LC46 failed to program 2 units of 24LC65 failed for single bit charge loss						

Parallel EEPROMs					FIT Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL PARALLEL	Dynamic Life	0/766	0/313	0	391,608	171	84	56
EEPROMS	Retention Bake	0/384	0/95	0	144,312	1	1	<1
28C64A	Dynamic Life	0/766	0/313	0	391,608	171	84	56
	Retention Bake	0/384	0/95	0	144,312	1	1	<1
Failure Modes:	Dynamic Life	N/A						
	Retention Bake	N/A						

EPROMs					FIT Rates, 60% Confidence Level			
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL EPROMS	Dynamic Life	5/7670	5/3220	10	3,993,360	93	45	55
	Retention Bake	1/9267	0/1805	1	3,073,056	<1	<1	<1
27C256	Dynamic Life	4/5360	0/2291	4	2,824,920	139	11	44
	Retention Bake	1/6496	0/1235	1	2,128,728	<1	<1	<1
27C512A	Dynamic Life	1/2310	5/929	6	1,168,440	67	104	81
	Retention Bake	0/2771	0/570	0	944,328	<1	<1	<1
Failure Modes:	Dynamic Life	2 units of 27C512A failed for single bit charge loss due to a hole in the oxide 4 units of 27C512A failed for leakage due to a hole in an oxide 4 units of 27C256 failed due to marginal V_{IH}						
	Retention Bake	1 unit of 27C256 failed due to an oxide defect in the 1st gate oxide						

II. PRESSURE COOKER and HAST PACKAGE DATA SUMMARY

Pressure Cooker

Stress Temperature:	121.5°C	Activation Energy:	0.6 eV
Derated Temperature:	55°C	Acceleration Rate:	36

HAST

Stress Temperature:	130°C	Activation Energy:	0.6 eV
Derated Temperature:	55°C	Acceleration Rate:	52

Operation	Package	168 Hrs.	1008 Hrs.	Fails	Device Hrs.	% Fails per 1000 Hrs.
Operation	**Package**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**% Fails per 1000 Hrs.**
Pressure Cooker	ALL PACKAGES	0/4979	7/4979	7	836,472	0.92
Pressure Cooker	PDIP	0/1334	0/1334	0	224,112	0.31
Pressure Cooker	PLCC	0/1014	7/1014	7	170,352	4.5
Pressure Cooker	SOIC	0/2439	0/2439	0	409,752	0.17
Pressure Cooker	TSOP	0/192	0/192	0	32,256	2.15
Failure Modes:	1 unit of 32L PLCC (27C256) failed due to lifted ball bonds 5 units of 32L PLCC (27C256) failed due to lifted ball bonds 1 unit of 32L PLCC (27C256) failed due to a leaky oxide causing single bit charge loss					

Operation	Package	168 Hrs.	1008 Hrs.	Fails	Device Hrs.	% Fails per 1000 Hrs.
HAST	ALL PACKAGES	8/4168	1/4077	9	689,304	1.4
HAST	PDIP	0/969	1/969	1	162,792	1.03
HAST	PLCC	0/477	0/477	0	80,136	0.86
HAST	SOIC	8/2572	0/2482	8	421,296	2.06
HAST	TSOP	0/150	0/149	0	25,080	2.76
Failure Modes:	8 units of 18L SOIC (57219) failed for high static I_{DD} 1 unit of 8L PDIP (24LC56) failed due to single bit charge loss					

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