Product Quality

A CORPORATE COMMITMENT

Microchip Technology Inc. has evolved a culture where a commitment to quality is an integral part. By empowering every employee to be responsible for the quality of their work, the entire corporation is involved in the quality process. This interaction creates an environment for continuous improvement throughout the organization. The benefits of the system are then not only enhanced product quality and reliability but also product services.

THE CHALLENGE OF COMPLEXITY

Integrating an Ideal

Microchip's quality programs and business plan are vertically integrated and touch all levels of the company. From the top down, the President and CEO actively lead programs to ensure continuous improvement is a perpetual process. Improvement and cross functional teams work to enhance performance at every department level. Incorporating the improvement objectives into the business plan creates a unity of purpose and mandates that the two merge as one measurement.

Determination to be the Best

A fundamental concept at Microchip is the commitment to continuous improvement. All areas are constantly looking for ways to improve every aspect of the company. This has allowed products and processes to become world class in quality and reliability. These programs are the foundation for success.

PROCESS TECHNOLOGY

All the products manufactured at Microchip make use of a common N-Well CMOS baseline process to which modules are added in order to create the specific functions required by the product (EEPROM, Microcontroller, Logic and EPROM).

The baseline process, which has been in Manufacturing for the last 8 years, uses minimum dimensions of 1.5µm, 360Å gate oxide thickness, N+ doped polysilicon gates and arsenic implanted source-drain diffusions for the N-channel devices.

A more advanced process uses minimum dimensions of 1µm, 250Å gate oxide thickness, polycide gate and LDD junction for the N-channel devices. A double level metal module can be added to both processes.

All of these devices utilize a proprietary passivation suitable for a wide variety of package types. Microchip's processes have been developed with reliability and manufacturability as their primary goals.

EEPROM

Microchip's CMOS floating gate EEPROM technology produces a non-volatile memory cell by storing or removing charge from the floating gate. Charge is transferred bidirectionally to the floating gate by Fowler-Nordheim tunneling through a sub-10 nm oxide over the drain of the transistor. This technology produces a memory cell with a typical endurance of $> 10^7$ cycles and greater than 40 years of data retention. (See EEPROM application note for details).

EPROM

This technology uses a non-volatile memory cell which stores charge on a self aligned floating gate. Electrons are provided to the floating gate via hot electron injection from the drain depletion region. Each byte can typically be programmed in 100 microseconds, and can retain that data for more than 10 years with unlimited reads. Block erasing is accomplished with a high intensity UV source through the package window. Windowed parts can be erased and reprogrammed more than 100 times.

Microcontroller and Logic

Logic products are built on a variety of Microchip's processes and their derivatives. These products have process modules for production of controllers that feature ROM, Analog, EPROM, and EEPROM. By utilizing the standard processing modules, the designs meld these technologies and their flexibility while maintaining the high quality and reliability standards expected.

QUALITY

Design for Quality and Reliability

Product reliability is designed into all Microchip processes and products. Design margins are established to guarantee every product can be produced economically, error-free and within the tolerances of the manufacturing process. Product Introduction Teams representing manufacturing, engineering, quality and product divisions ensure that exacting standards are met for each specific product.

Documentation and Procurement Specifications

Microchip's documentation control program assures the correct and current document always is available at the point of use. Active documents are revision coded and serialized. Procurement specifications bear the same requirements. These document control procedures, which are common in the industry for military and high reliability products, are employed by Microchip, system wide.

In Line Controls and Process Assessment

Product integrity is assured by sampling and inspection plans performed in-line. This enables Microchip to control and improve product quality levels as product moves through the manufacturing operation. Microchip's acceptance sampling plans in assembly emphasize the attempt to eliminate defective product as it is discovered. Acceptance and sampling plans are based on proprietary low fraction defective (<1000ppm) quality statistics.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at selected process steps. In-process controls are performed by operators in the wafer fabrication and assembly operations. Operators take immediate corrective action if a process step is out of its control limit. Through these in-line controls the true capability of a process is generated. (See Appendix A:In Line Controls)

Control of Customer Quality is attained through a statistical program based on minimum defect capability levels. These levels are defined as the error levels associated with the circuit design and science limitations of the chemistry and physics of processing.

Material controls prevent defective piece parts from getting into the line. Microchip's assembly material control sample plan is typical of the emphasis placed on safeguards. (See Appendix B:Material Controls Package).

Testing for Margin

Microchip conducts a product's initial test under stringent requirements. All quality assurance tests are run to tighter limits than customer specifications. As part of an outgoing quality assurance program, products are tested at least two machine tolerances tighter than those limits specified by the customer on every parameter. Margin testing accounts for normal tolerances of any particular test system and provides the assurance that Microchip's products meet a customer's specifications.

Variation from Expectation

Microchip works to make variation from target as small as possible. The better process is the one that holds the narrowest dispersion. Processes are targeted to maintain Cpk's of >1.5 and currently have typical values of >2.0. Higher process capability values are continually strived for indicating that better process control is being obtained.

Outgoing Quality

Quality Control samples all outgoing product from final testing. These samples measure in-line defect levels after screens have been applied. Root cause analysis follows, initiating technical change to effect continuous improvement.

Programmability Yield

Using programmable devices adds a complexity to the Quality Level interpretation. It is not unlikely that some programmable devices will not program. The programmability yield is dependent on (but not limited to): programmers, technology, array size, and handling.

Any device that does not program properly will not be used in the end system. Therefore, programmability yields should not be used to calculate AQLs.

For convenience, Microchip offers programming services for certain devices. This service is an advantage to the customer since it not only eliminates programmability rejects, but also reduces the handling of the parts. See the individual data sheets for details on our Quick-Turnaround-Production (QTP) service.

RELIABILITY

Process Qualification

No priority is more important than the one where processes under which Microchip products are built operate without fail. All products are stressed beyond normal use limits when undergoing high temperature operating life and retention bake tests. This is done to ensure that the devices meet the strictest reliability guidelines and will maintain industry low failure rates.

Package Qualification

Package qualification measures a component's ability to withstand extreme thermal and mechanical stresses. All products are stressed to high level industrial specifications to ensure reliability.

Ongoing Sampling of Key Reliability Variables

Microchip conducts accelerated mechanical tests, operating life tests and memory retention tests to explore the many ways failures might occur. Data obtained from continuous testing is used to identify potential reliability problems and for defining action courses to improve product. Microchip's reliability knowledge is shared with customers. This data is available for use in customer's own quality and reliability improvement programs and is published in regular quarterly and yearly reports.

RELIABILITY CONCEPTS

Definition

Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The reliability (or probability of survival) range runs from 0 (no chance of survival) to 1 (no chance of failure). Current microelectronic circuits are manufactured and controlled to such tight specifications that reliability figures for the total operation time approaching 1 (i.e., 0.9999) are common. As a result, the complement of reliability, or the failure probability, is more often quoted in current literature.

The failure rate is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per unit circuit-hour would generally be very small. To avoid reporting such small numbers, failure rates have been defined for greater circuit-hours. One thousand circuit-hours is defined as one circuit operating for one thousand hours, or 1,000 circuits operating for 1 hour, etc. The numbers of circuit-hours is the number of circuits multiplied by the number of operation hours for each circuit.

Two methods to define failure rate are commonly used:

- Percent failures per thousand circuit-hours
- Absolute failures per billion circuit-hours, or FITs.

Note that a failure rate of 0.0001%/1000 hours and 1 FIT are equivalent numbers.

Bathtub Curve: Failure Rate Over Time

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. (See Figure 1).

The early failure rate (infant mortality) period starts from initial operation (time T0) and decreases as time goes on.

Time T1 signifies the end of the infant mortality period. The next phase of the curve occurs between time T1 and T2. This long period of time is distinguished by a nearly constant and very low failure rate. After T2 is passed, the failure rate starts to increase slowly. This last phase of failure rate vs. time is known as the wear-out period.

Temperature Dependency

In order to establish failure rates in a reasonable time, it is necessary to accelerate the incidence of the failure modes. Higher environmental stress levels than those encountered under normal conditions are needed. The accelerating parameter most employed is junction temperature, although voltage and humidity, for example, are also used. Higher temperatures are capable of accelerating many common failure modes dramatically.

Arrhenius Equation

A number of mathematical models were developed to quantify the relationship between accelerated failure rates and increased junction temperatures. The one model most commonly used employs the Arrhenius Equation. It is as follows:

$$AF = e^{x}, \text{ where } x = \frac{E_A}{K}\left[\frac{1}{T_N} - \frac{1}{T_A}\right]$$

AF = Acceleration Factor (non-dimensional)

e = 2.718281828... (non-dimensional constant)

E_A = Activation energy level (electron volts)

k = Boltzmann's constant = 8.6172 x 10-5 (electron-volts/degree Kelvin)

T_N = Normal junction temperature (degrees Kelvin)

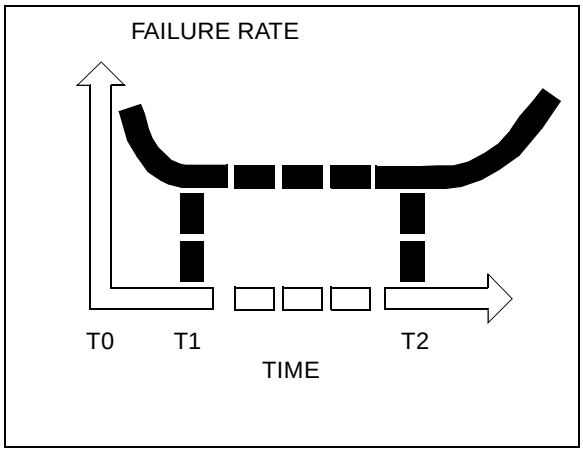
T_A = Accelerated junction temperature (degrees Kelvin)

Thus, the time to achieve a certain probability of failure at time T1 under temperature T_N can be compressed to T1 divided by AF at the accelerated temperature, T_A.

Note that for true acceleration, the acceleration factor AF is independent of the probability of the fail point specified.

AF, the dependent variable of the Arrhenius Equation is a function of several variables. T_N and T_A are specified for the situation under consideration. E_A is a function of the particular mode of failure, and is determined by experimental evaluation.

FIGURE 1: BATHTUB CURVE



Activation Energy Level

Activation energy levels in semiconductors generally are in the 0.3 - 1.1 electron-volt range. Each failure mode has its own activation energy. Some typical examples are:

FAILURE MECHANISM	E_A (eV)
Oxide/Dielectric Breakdown	0.3
Electromigration	0.5 to 0.7
Surface Related Contamination	1.0
Intermetallics	1.0
Floating Gate Charge Loss	0.6 to 1.2
Hot Electron Trapping	-.1
Charge Trapping	0.12

A compromise value of 0.6 electron-volts is often used when there is no specific information relating to the failure modes being accelerated.

RELIABILITY TESTS

Operating Life Test

The Operating Life Test is run under dynamic bias conditions where inputs are clocked. The test is conducted at high temperature to accelerate the failure mechanisms. The normal temperature for the test is +125°C for 1,000 hours. Readouts occur at 168 and 1,000 hours. Early hour failures are usually associated with manufacturing defects or otherwise marginal material.

Retention Bake

The Retention Bake Test is performed to accelerate data loss on floating gate devices. The test consists of unbiased baking at elevated temperature. Usually the test lasts for 1,000 hours at +150°C. The failure mechanism that is accelerated is charge leakage from a stored element.

Endurance Cycling

Endurance Cycling establishes the number of times a device can be programmed and erased. Normally the test is conducted at rated temperature conditions and is followed by retention bake. The standard cycling at Microchip is done at 85°C using a page cycle mode and is followed by a bake of both a checkerboard and an inverse checkerboard of 48 hours at 150°C.

Temperature Cycle

The Temperature Cycle test simulates stresses which occur to systems during power up/power down sequences. The test is intended to reveal any deficiencies resulting from thermal expansion mismatch of the die/package structure. Normally the test is conducted by cycling between -65°C and +150°C in an air ambient. Duration for the test is typically 500 cycles for both plastic and ceramic packages. Endpoint criteria are both electrical and visual/mechanical.

Thermal Shock

The Thermal Shock test is similar to the Temperature Cycle test except that the ambient during cycling is liquid-to-liquid. This stimulates rapid thermal environmental changes. The mechanisms accelerated are identical to those in the Temperature Cycle test except that the Thermal Shock test is a more accelerated test with temperatures normally +125°C to -55°C. The number of cycles are 500 for qualification testing.

Autoclave

The autoclave test determines the survivability of devices in molded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121°C and 15 pounds per square inch (one atmosphere) gauge pressure. The 168 or more hours of testing allows moisture to penetrate into the die. Chemical corrosion of the die metallization may occur if ionic contaminants are present and the die surface protection is deficient or damaged. Charge leaks from floating devices usually happen before a corrosion mechanism develops.

Temperature Humidity Test

The Temperature Humidity test determines the survivability of devices in molded plastic packages functioning in a hot, humid environment. By convention, test conditions are 85°C with 85% relative humidity. The parts are biased to lend themselves to electrochemical corrosion. The duration of the test is usually 1,000 hours or more. The test checks the adequacy of the die surface protection and the plastic's lack of ionic impurities. The applied bias is 5 volts on alternating pins or set up for minimum power to reduce internal heating and consequent moisture evaporation on the device. Similar to the Autoclave test, charge loss on floating gate devices is a principle failure mechanism.

HAST

The Highly Accelerated Stress Test is similar to the Temperature Humidity Test but with more stringent temperature exposure. Devices are subjected to 130°C with 85% relative humidity and an alternating bias of 5 volts and ground on device pins. The duration of the test is 168 hours. This tests for ionic contamination and corrosion, but floating gate devices may also fail for charge loss, due to the high temperature.

QUALIFICATION CATEGORIES

In general, qualification is required for new design, major changes in old design, process or material when either wafer fabrication or package assembly operations are affected. Cross functional teams which include reliability develop new products for introduction. In other areas, Microchip utilizes the concept of a Change Control Board which meets regularly to establish which criteria is to be used for all specific proposed changes. This board is made up of representative leaders of various groups and departments throughout Microchip to insure all concerns are heard early during the process.

QUALIFICATION PROGRAMS

Qualifications guarantee changes to or new processes and technologies are properly evaluated for reliability performance.

Reliability Monitoring

Microchip's reliability monitoring program is a comprehensive effort to measure the reliability of all process families with strict regularity. The program strives to improve performance through failure analysis and corrective action. Numerous screening procedures are used and estimates of product life and expected failure rates are provided.

Typical tests and frequencies include:

- Die Monitor on selected product for -
  - Dynamic Life
  - Retention Bake
  - Endurance
- Periodic (weekly, monthly and quarterly) package monitors to evaluate:
  - Mechanical stresses
  - Alignment
  - Temperature and moisture stresses
  - Corrosion resistance
  - Marking permanency

APPENDIX A: IN LINE CONTROLS

TABLE 1: CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% sample LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	4X/Lot/Machine LTPD 15	X	—	N/A
Wire Bond	Machine Shut Down	1% AQL each 1/2 shift	X	—	MIL-STD-883C Method 2010
Post Wire Bond	Reject defectives 100% rescreen per LTPD	LTPD 15	X	—	MIL-STD-883C Method 2010
Mold Press	Machine Shut Down	One sample /4 hrs	X	—	N/A
Die Plating	Reject defectives 100% rescreen per LTPD	Every 4 hrs LTPD 10	X	—	N/A
Trim and Form	Reject defectives 100% rescreen per LTPD	Once/ 2 hrs LTPD 10	X	—	N/A
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

TABLE 2: CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	Non-destruct each 2 hrs destruct each shift	X	—	MIL-STD-883C Method 2010
Wire Bond	Machine Shut Down	4X/shift/machine	X	—	MIL-STD-883C Method 2010
Preseal Visual	Reject defectives 100% rescreen per LTPD	100% LTPD 15	— X	X —	MIL-STD-883C Method 2010
Package Seal	Machine Shut Down	LTPD 15	X	—	N/A
Environmental Stress Centrifuge Temp Cycle	Machine Shut Down	LTPD 5 84(0) 84(0)	X	—	MIL-STD-883C Method 2001 Method 1010
Fine Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Gross Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Lead Trim	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2009
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

APPENDIX B: MATERIAL CONTROLS PACKAGE

TABLE 3: MATERIALS CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Lead Frame	Reject defectives 100% rescreen per LTPD	Visual, LTPD 2 Functional, LTPD 10 and material spec	X	—	N/A
Die Attach Epoxy	Reject	Functional, LTPD 15 and material spec	X	—	N/A
Gold Wire	Reject	Per material spec	X	—	N/A
Molding Compound	Reject	Spiral flow, 3X/lot Functional, 1X/lot and material spec	X	—	N/A

TABLE 4: MATERIALS CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Base/Lead Frame	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Package	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Preform	Reject	Visual, LTPD 10 Functional, LTPD 15	X	—	MIL-M-38510
Bond Wire	Reject	Per material spec 2 spools/lot	X	—	MIL-M-38510
Lid	Reject	Visual, LTPD 7 Functional, LTPD 10 and material spec	X	—	MIL-M-38510

WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 786-7277
Technical Support: 602 786-7627

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770 640-0034 Fax: 770 640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508 480-9990 Fax: 508 480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 708 285-0071 Fax: 708 285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 214 991-7177 Fax: 214 991-8588

Dayton
Microchip Technology Inc.
35 Rockridge Road
Englewood, OH 45322
Tel: 513 832-2543 Fax: 513 832-2841

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 455
Irvine, CA 92715
Tel: 714 263-1888 Fax: 714 263-1338

New York
Microchip Technology Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

AMERICAS (continued)

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

ASIA/PACIFIC

Hong Kong
Microchip Technology
Unit No. 3002-3004, Tower 1
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T. Hong Kong
Tel: 852 2 401 1200 Fax: 852 2 401 3431

Korea
Microchip Technology
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku,
Seoul, Korea
Tel: 82 2 554 7200 Fax: 82 2 558 5934

Singapore
Microchip Technology
200 Middle Road
#10-03 Prime Centre
Singapore 0718
Tel: 65 334 8870 Fax: 65 334 8850

Taiwan
Microchip Technology
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2 717 7175 Fax: 886 2 545 0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire
SL8 5AJ
Tel: 44 0 1628 851077 Fax: 44 0 1628 850259

France
Arizona Microchip Technology SARL
2 Rue du Buisson aux Fraises
91300 Massy - France
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Muenchen, Germany
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Pegaso Ingresso No. 2
Via Paracelso 23, 20041
Agrate Brianza (MI) Italy
Tel: 39 039 689 9939 Fax: 39 039 689 9883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shin Yokohama
Kohoku-Ku, Yokohama
Kanagawa 222 Japan
Tel: 81 45 471 6166 Fax: 81 45 471 6122

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