EVALUATION KIT AVAILABLE

MAXIM

Low-Power, 60Msps, Dual, 6-Bit ADC

MAX1002

_____General Description

The MAX1002 is a dual, 6-bit analog-to-digital converter (ADC) that combines high-speed, low-power operation with a user-selectable input range, an internal reference, and a clock oscillator. The dual, parallel ADCs are designed to convert in-phase (I) and quadrature (Q) analog signals into two 6-bit offset-binary-coded digital outputs at sampling rates up to 60Msps while achieving typical integral nonlinearity (INL) and differential nonlinearity (DNL) of ±1/4LSB. The ability to interface directly with baseband I and Q signals makes the MAX1002 ideal for use in direct-broadcast satellite, VSAT, and QAM16 demodulation applications.

The MAX1002 input amplifiers feature true differential inputs, a 55MHz -0.5dB analog bandwidth, and user-programmable input full-scale ranges of 125mVp-p, 250mVp-p, or 500mVp-p. With an AC-coupled input signal, matching performance between input channels is typically 0.1dB gain, 1/4LSB offset, and 0.5° phase. Dynamic performance is 5.85 effective number of bits (ENOB) with a 20MHz analog input signal, or 5.78 ENOB with a 50MHz input signal.

The MAX1002 operates with a single +5V power supply and provides TTL-compatible digital outputs. The device is available in the commercial temperature range (0°C to +70°C) and comes in a 36-pin SSOP package.

_____Applications

Direct Broadcast Satellite (DBS) Receivers

VSAT Receivers

Wide Local Area Networks (WLAN)

Cable Television Set-Top Boxes

_____Features

♦ **±1/4LSB INL and DNL, Typical**

♦ **1/4LSB (typ) Channel-to-Channel Offset Matching**

♦ **0.1dB Gain and 0.5° Phase Matching, Typical**

♦ **Internal Bandgap Voltage Reference**

♦ **Two Matched 6-Bit, 60Msps ADCs**

♦ **Excellent Dynamic Performance:**
   5.85 ENOB with 20MHz Analog Input
   5.7 ENOB with 50MHz Analog Input

♦ **Internal Oscillator with Overdrive Capability**

♦ **55MHz (-0.5dB) Bandwidth Input Amplifiers with True Differential Inputs**

♦ **User-Selectable Input Full-Scale Range (125mVp-p, 250mVp-p, or 500mVp-p)**

♦ **Single-Ended or Differential Input Drive**

♦ **+5V Single Supply**

♦ **TTL Outputs**

♦ **90Msps Upgrade with +3.3V CMOS-Compatible Output Available (MAX1003)**

_____Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1002CAX	0°C to +70°C	36 SSOP

Pin Configuration appears at end of data sheet.

_____Functional Diagram

MAXIM _____ **Maxim Integrated Products   1**
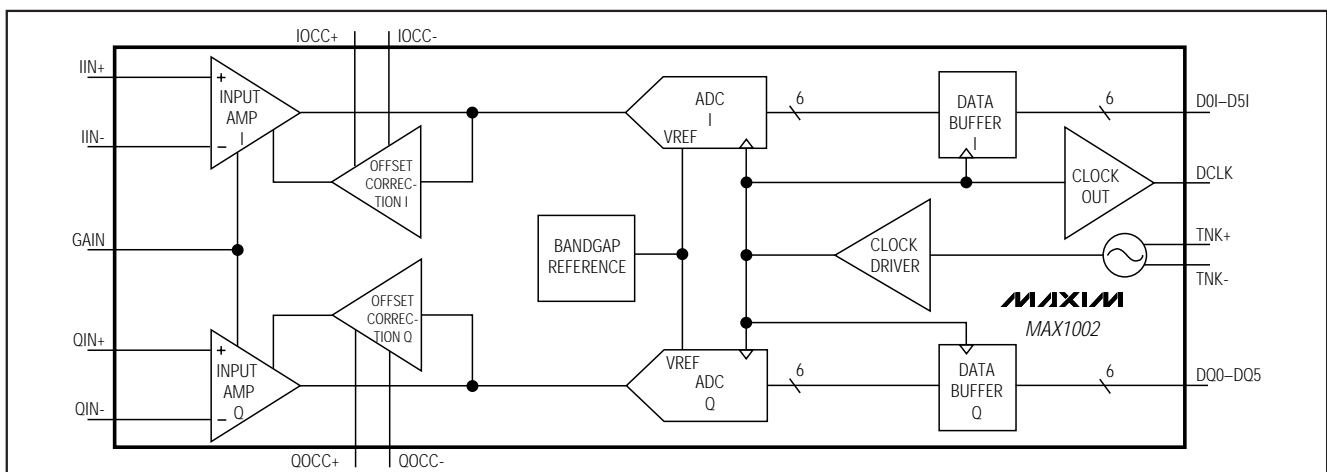
Low-Power, 60Msps, Dual, 6-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V$_{CC}$ to GND ....-0.3V to +6.5V
V$_{CCO}$ to OGND...-0.3V, +6.5V
GND to OGND ....-0.3V, +0.3V
Digital and Clock Output Pins to OGND ....-0.3V, V$_{CCO}$ (<10sec)
All Other Pins to GND..-0.3V, V$_{CC}$

Continuous Power Dissipation (T$_A$ = +70°C)
   SSOP (derate 45mW/°C above +70°C) 941mW
Operating Temperature Range..............................0°C to +70°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, <10sec)...........................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V$_{CC}$, V$_{CCO}$ = +5V ±5%; T$_A$ = T$_{MIN}$ to T$_{MAX}$; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution	RES		6			Bits
Integral Nonlinearity	INL		-0.5	±0.25	0.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature	-0.5	±0.25	0.5	LSB
Full-Scale Input Range	V$_{FSH}$	GAIN = V$_{CC}$ (high gain)	118.75	125	131.25	mVp-p
	V$_{FSM}$	GAIN = open (mid gain)	237.5	250	262.5	
	V$_{FSL}$	GAIN = GND (low gain)	475	500	525	
INVERTING AND NONINVERTING ANALOG INPUTS						
Input Open-Circuit Voltage	V$_{AOC}$		2.25	2.35	2.45	V
Input Resistance	R$_{IN}$		13	20	29	kΩ
Input Capacitance	C$_{IN}$	Guaranteed by design		3	5	pF
Common-Mode Voltage Range	V$_{CM}$	Other analog input driven with external source (Note 2)	1.75		2.75	V
OSCILLATOR INPUTS						
Oscillator Input Resistance	R$_{OSC}$	Other oscillator input tied to V$_{CC}$ + 0.3V	4.8	8	12.1	kΩ
DIGITAL OUTPUTS (DI0–DI5, DQ0–DQ5)						
Digital Outputs Logic-High Voltage	V$_{OH}$	I$_{SOURCE}$ = 50µA	2.4			V
Digital Outputs Logic-Low Voltage	V$_{OL}$	I$_{SINK}$ = 400µA			0.5	V
POWER SUPPLY						
Supply Current	I$_{CC}$			63	104	mA
Power-Supply Rejection Ratio	PSRR	V$_{CC}$ = 4.75V to 5.25V (Note 3)		-75	-40	dB
Digital Outputs Supply Current	I$_{CCO}$	20MHz, FS I & Q analog inputs, C$_{LOAD}$ = 15pF (Note 4)			24	mA
Power Dissipation	PD			380		mW

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AC ELECTRICAL CHARACTERISTICS

(V_{CC}, V_{CCO} = +5V ±5%; T_A = +25°C; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (GAIN = open; external 60MHz clock (Figure 7); V_{INI}, V_{INIQ} = 20MHz sine; amplitude -1dB below FS; unless otherwise noted.)						
Maximum Sample Rate	f_{MAX}			60		Msps
Analog Input -0.5dB Bandwidth	BW	Gain = GND, open, V_{CC}		55		MHz
Effective Number of Bits	$ENOB_M$	GAIN = open (mid gain)	5.6	5.85		Bits
		GAIN = open (mid gain), V_{IN} = 50MHz, -1dB below FS		5.7		
	$ENOB_H$	Gain = V_{CC} (high gain)		5.8		
	$ENOB_L$	Gain = V_{CC} (low gain)		5.85		
Signal-to-Noise and Distortion Ratio	SINAD	Gain = open (mid gain)	35.4	37		dB
Input Offset (Note 5)	OFF	I channel	-0.5		0.5	LSB
		Q channel	-0.5		0.5	
Crosstalk Between ADCs	XTLK			-55		dB
Offset Mismatch Between ADCs	OMM2	(Note 5)	-0.5	±0.25	0.5	LSB
Amplitude Match Between ADCs	AM		-0.2	±0.1	0.2	dB
Phase Match Between ADCs	PM		-2	±0.5	2	degrees
TIMING CHARACTERISTICS (data outputs: R_L = 1MΩ, C_L = 15pF, Figure 8)						
DCLK to Data-Propagation Delay	t_{PD}	(Note 6)		7.1		ns
Data Valid Skew	t_{SKEW}	(Note 6)		3.6		ns
Input to DCLK Delay	t_{DCLK}	TNK+ to DCLK (Note 6)		5.3		ns
Aperture Delay	t_{AP}			5.5		ns
Pipeline Delay	PD			1		clock cycle

Note 1: Best straight-line linearity method.
Note 2: A typical application will AC couple the analog input to the DC bias level present at the analog inputs (typically 2.35V). However, it is also possible to DC couple the analog input (using differential or single-ended drive) within this common-mode input range (Figures 4, 5).
Note 3: PSSR is defined as the change in the mid-gain, full-scale range as a function of the variation in V_{CC} supply voltage (expressed in decibels).
Note 4: The current in the V_{CCO} supply is a strong function of the capacitive loading on the digital outputs. To minimize supply transients and achieve the best dynamic performance, reduce the capacitive loading effects by keeping line lengths on the digital outputs to a minimum.
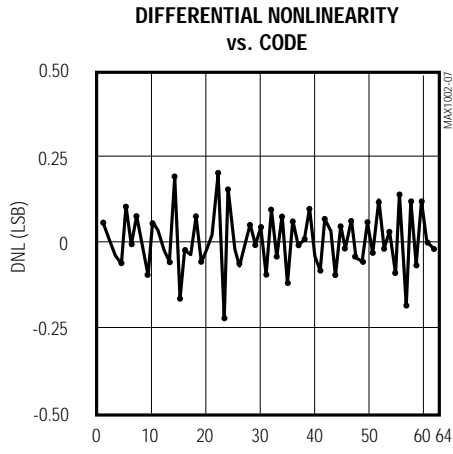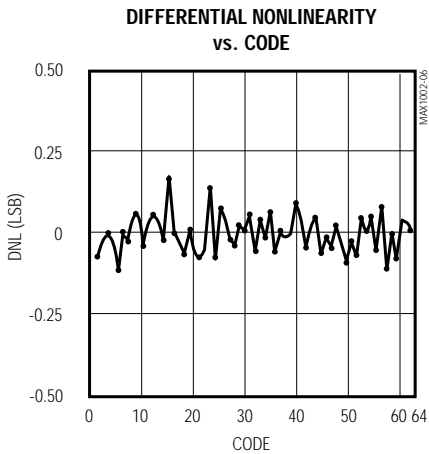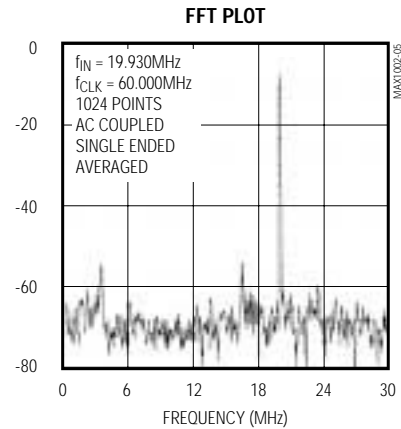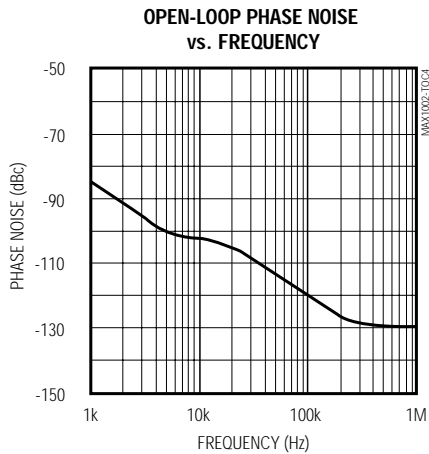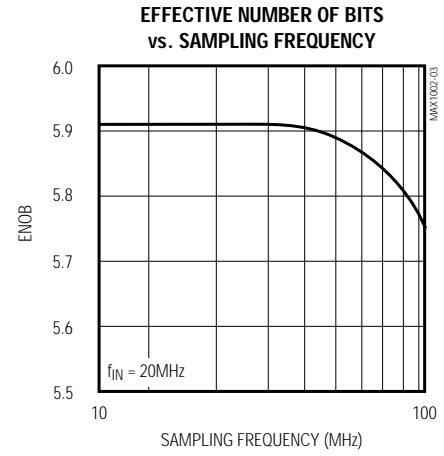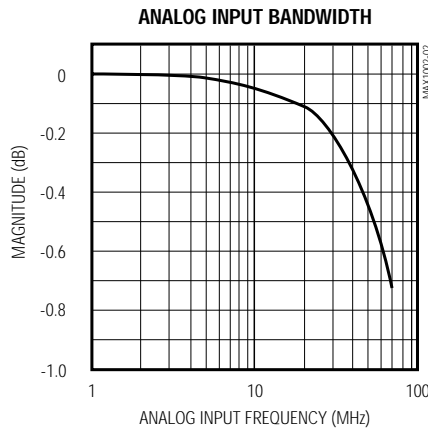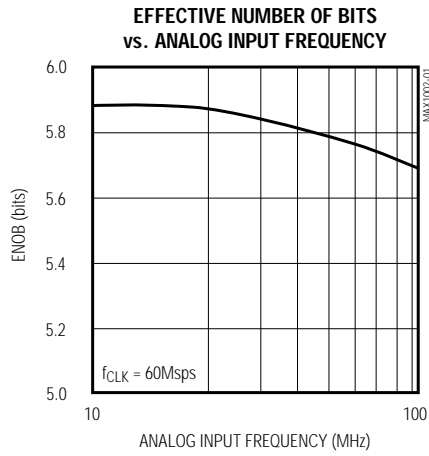**Note 5:** Offset-correction compensation enabled, 0.22µF at Q and I compensation inputs (Figures 2, 3).
Note 6: t_{PD} and t_{SKEW} are measured from the 1.4V level of the output clock, to the 1.4V level of either the rising or falling edge of a data bit. t_{DCLK} is measured from the 50% level of the clock overdrive signal on TNK+ to the 1.4V level of D_{CLK}. The capacitive load on the outputs is 15pF.

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(V_CC, V_CCO = +5V ±5%; MAX1002/MAX1003 evaluation kit; T_A = +25°C; unless otherwise noted.)

EFFECTIVE NUMBER OF BITS vs. ANALOG INPUT FREQUENCY

ANALOG INPUT BANDWIDTH

EFFECTIVE NUMBER OF BITS vs. SAMPLING FREQUENCY

OPEN-LOOP PHASE NOISE vs. FREQUENCY

FFT PLOT

DIFFERENTIAL NONLINEARITY vs. CODE

DIFFERENTIAL NONLINEARITY vs. CODE

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_____Pin Description

PIN	NAME	FUNCTION
1	GAIN	Gain-Select Input. Sets input full-scale range: 125/250/500mVp-p (Table 1).
2	IOCC+	Positive I-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
3	IOCC-	Negative I-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
4	IIN+	I-Channel Noninverting Analog Input
5	IIN-	I-Channel Inverting Analog Input
6	V_{CC}	+5V ±5% Supply. Bypass with 0.01µF capacitor to GND (Pin 7).
7, 11, 12, 18, 19	GND	Analog Ground
8	V_{CC}	+5V ±5% Supply. Bypass with 0.01µF capacitor to GND (Pin 11).
9	TNK+	Positive Oscillator/Clock Input
10	TNK-	Negative Oscillator/Clock Input
13	V_{CC}	+5V ±5% Supply. Bypass with 0.01µF capacitor to GND (Pin 12).
14	QIN-	Q-Channel Inverting Analog Input
15	QIN+	Q-Channel Noninverting Analog Input
16	QOCC-	Negative Q-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
17	QOCC+	Positive Q-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
20–25	DQ5–DQ0	Q-Channel Digital Outputs 0–5. DQ5 is the most significant bit (MSB).
26, 28	V_{CCO}	+5V ±5% Digital Supply. Bypass each with 47pF to OGND (Pin 27).
27	OGND	Digital Output Ground
29	DCLK	Digital Clock Output. Frames the output data.
30–35	DI0–DI5	I-Channel Digital Outputs 0–5. DI5 is the most significant bit (MSB).
36	V_{CC}	+5V ±5% Supply. Bypass with 0.01µF to GND (Pin 19).

_____Detailed Description

Converter Operation

The MAX1002 contains two 6-bit analog-to-digital converters (ADCs), a buffered voltage reference, and oscillator circuitry. The ADCs use a flash-conversion technique to convert an analog input signal into a 6-bit parallel digital output code. The MAX1002's unique design includes 63 fully differential comparators and a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. The control logic interfaces easily to most digital signal processors (DSPs) and microprocessors (µPs) with +5V CMOS-compatible logic interfaces. Figure 1 shows the MAX1002 in a typical application.

Programmable Input Amplifiers

The MAX1002 has in-phase (I) and quadrature (Q) programmable-gain input amplifiers with a 55MHz -0.5dB bandwidth and true differential inputs. To maximize performance in high-speed systems, each amplifier has less than 5pF of input capacitance. The input amplifier gain is programmed via the GAIN pin to provide three possible input full-scale ranges (FSR) (Table 1).

Table 1. Input Amplifier Programming

GAIN	INPUT FULL-SCALE RANGE (mVp-p)
GND	500
Open	250
V_{CC}	125

/VI/IXI/VI

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Figures 2 and 3 show single-ended and differential AC-coupled input circuits. Each of the amplifier inputs is internally biased to a 2.35V reference through a 20kΩ resistor, eliminating external DC bias circuits. A series 0.1µF capacitor is required at each amplifier input for AC-coupled signals.

When operating with AC-coupled inputs, the input amplifiers' DC offset voltage is nulled to within ±1/2LSB by an on-chip offset-correction amplifier. An external compensation capacitor is required to set the dominant pole of the offset-correction amplifier's frequency response (Figures 2 and 3). The compensation capacitor determines the low-frequency corner of the analog input response according to the following formula:

$$f_C = 1 / (0.1 \times C)$$

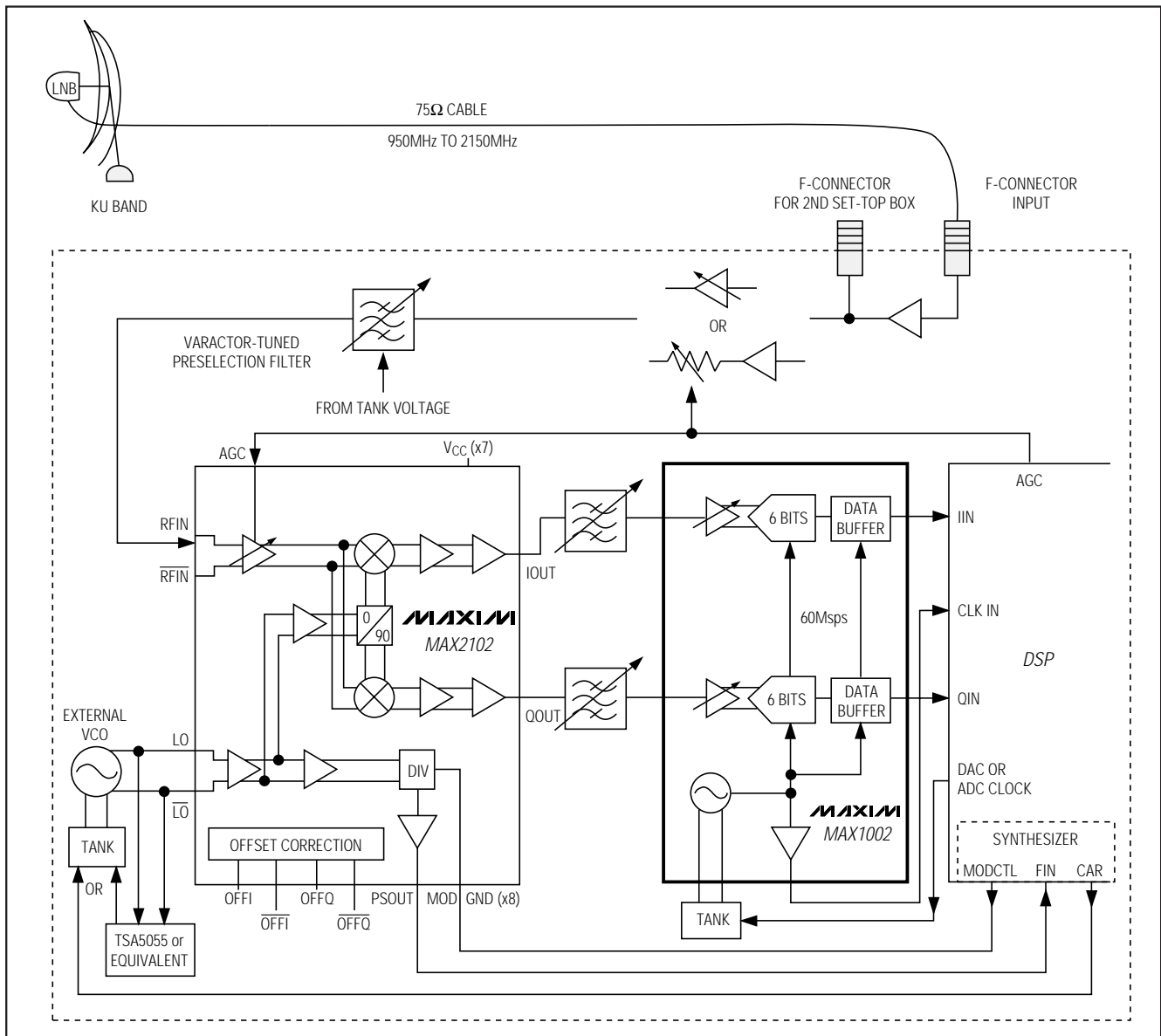where C is the value of the compensation capacitor in µF, and fc is the corner frequency in Hz.

Figure 1. Commercial Satellite Receiver System

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Figures 4 and 5 show single-ended and differential DC-coupled input circuits for applications where a DC component of the input signal is present. The amplifiers' input common-mode voltage range extends from 1.75V to 2.75V. To prevent attenuation of the input signal's DC component when operating in this mode, disable the offset-correction amplifier by grounding the _OCC+ and _OCC- pins for the I and Q blocks (Figures 4 and 5).

ADCs

The I and Q ADC blocks receive the analog signals from the respective I and Q input amplifiers. The ADCs use flash conversion with 63 fully differential comparators to digitize the analog input signal into a 6-bit output in offset binary format.
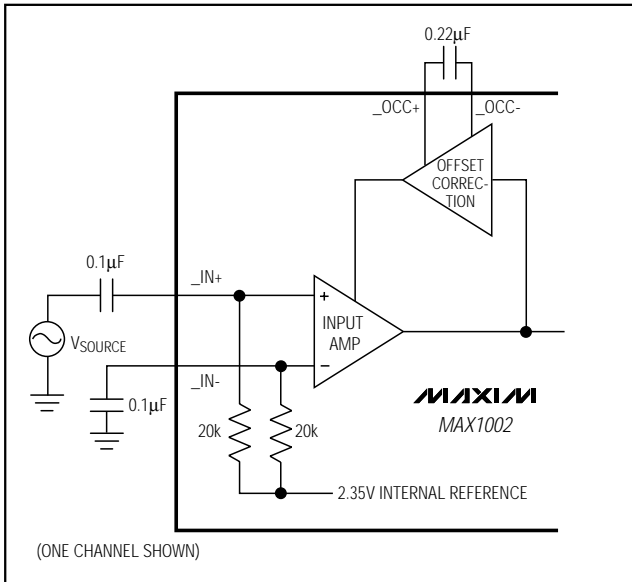

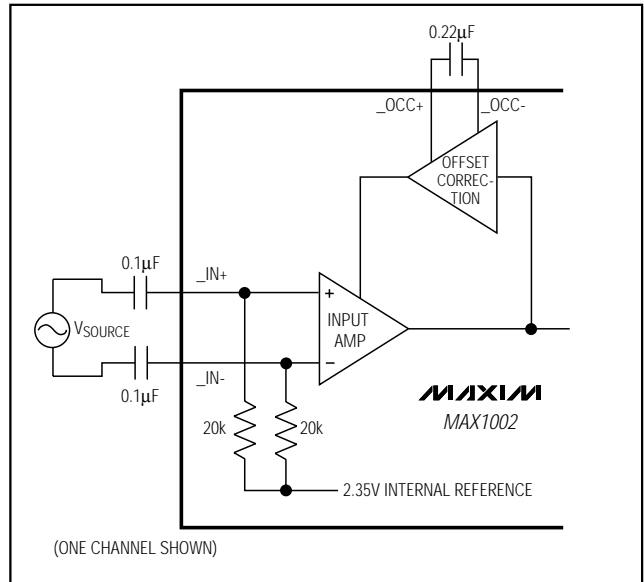Figure 2. Single-Ended AC-Coupled Input

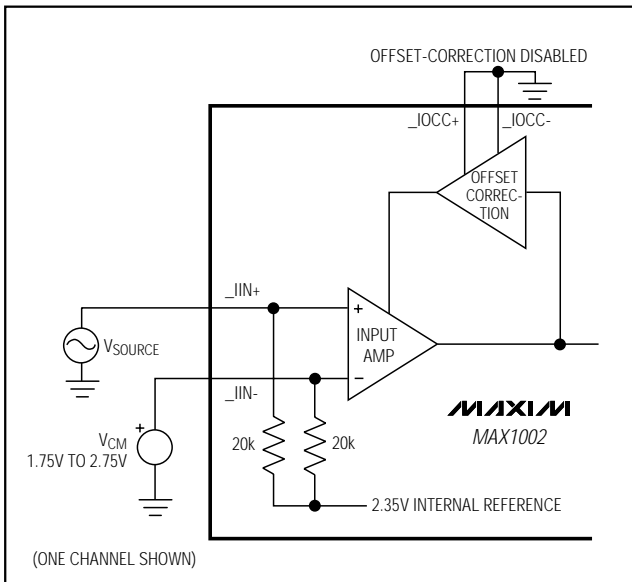Figure 3. Differential AC-Coupled Input

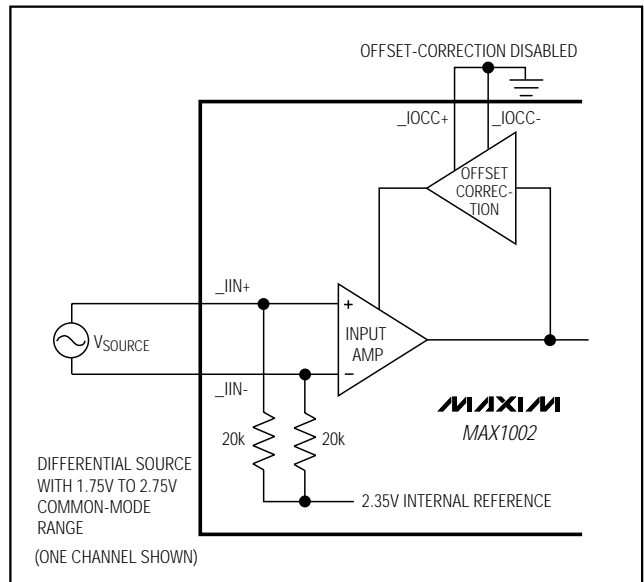Figure 4. Single-Ended DC-Coupled Input

Figure 5. Differential DC-Coupled Input

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The MAX1002 features a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. Dynamic encoding errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for typical converters can be incorrect, including false full- or zero-scale outputs. The MAX1002's unique design reduces the magnitude of this type of error to 1LSB.

Internal Voltage Reference

An internal buffered bandgap reference is included on the MAX1002 to drive the ADC's reference ladders. The on-chip reference and buffer eliminate any external (high-impedance) connections to the reference ladder, minimizing the potential for noise coupling from external circuitry while ensuring that the voltage reference, input amplifier, and reference ladder track well with variations in temperature and power supplies.

Oscillator Circuit

The MAX1002 includes a differential oscillator, which is controlled by an external parallel resonant (tank) network (Figure 6). As an alternative, the oscillator may be overdriven with an external clock source (Figure 7).

Internal-Clock Operation (Tank)

If the tank circuit is used, the resonant inductor should have a sufficiently high Q and a self-resonant frequency (SRF) of at least twice the intended oscillator frequency. Coilcraft's 1008HS-221, with a 700MHz SRF and a Q of 45, works well for this application. Generate different clock-frequency ranges by adjusting varactor and tank elements.

An internal-clock-driver buffer is included to provide sharp clock edges to the internal flash comparators. The buffer ensures that the comparators are simultaneously clocked, maximizing the ADC's effective number of bits of performance.

External-Clock Operation

To accommodate designs that use an external clock, the MAX1002's internal oscillator can be overdriven by an external clock source (Figure 7). The external clock source should be a sinusoid to minimize clock-phase noise and jitter, which can degrade the ADC's effective bits performance. AC couple the clock source (recommended voltage level is approximately 1Vp-p) to the oscillator inputs (Figure 7).
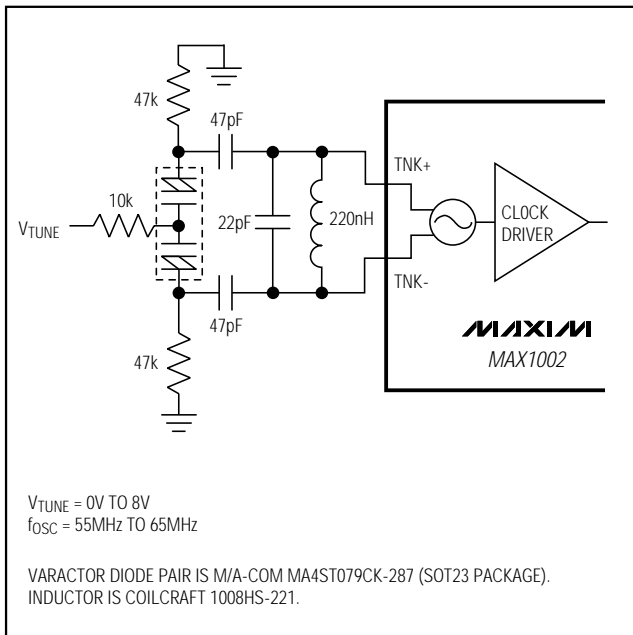

V_{TUNE} = 0V TO 8V
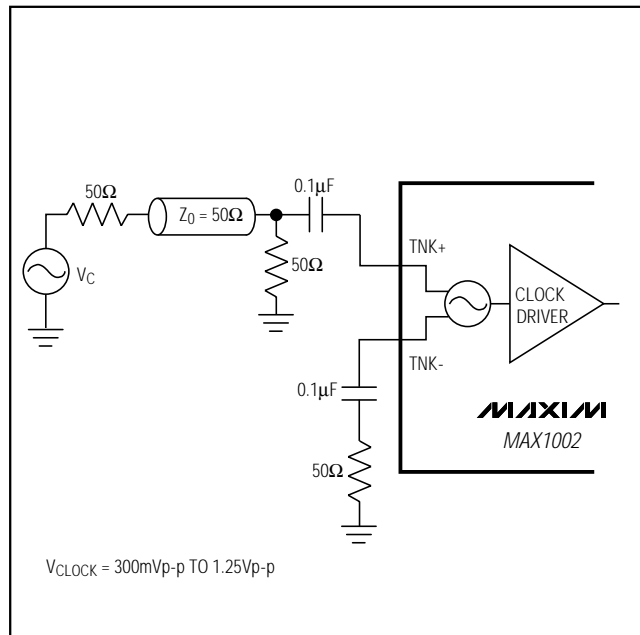f_{OSC} = 55MHz TO 65MHz

VARACTOR DIODE PAIR IS M/A-COM MA4ST079CK-287 (SOT23 PACKAGE).
INDUCTOR IS COILCRAFT 1008HS-221.

Figure 6. Tank-Resonator Oscillator

V_{CLOCK} = 300mVp-p TO 1.25Vp-p

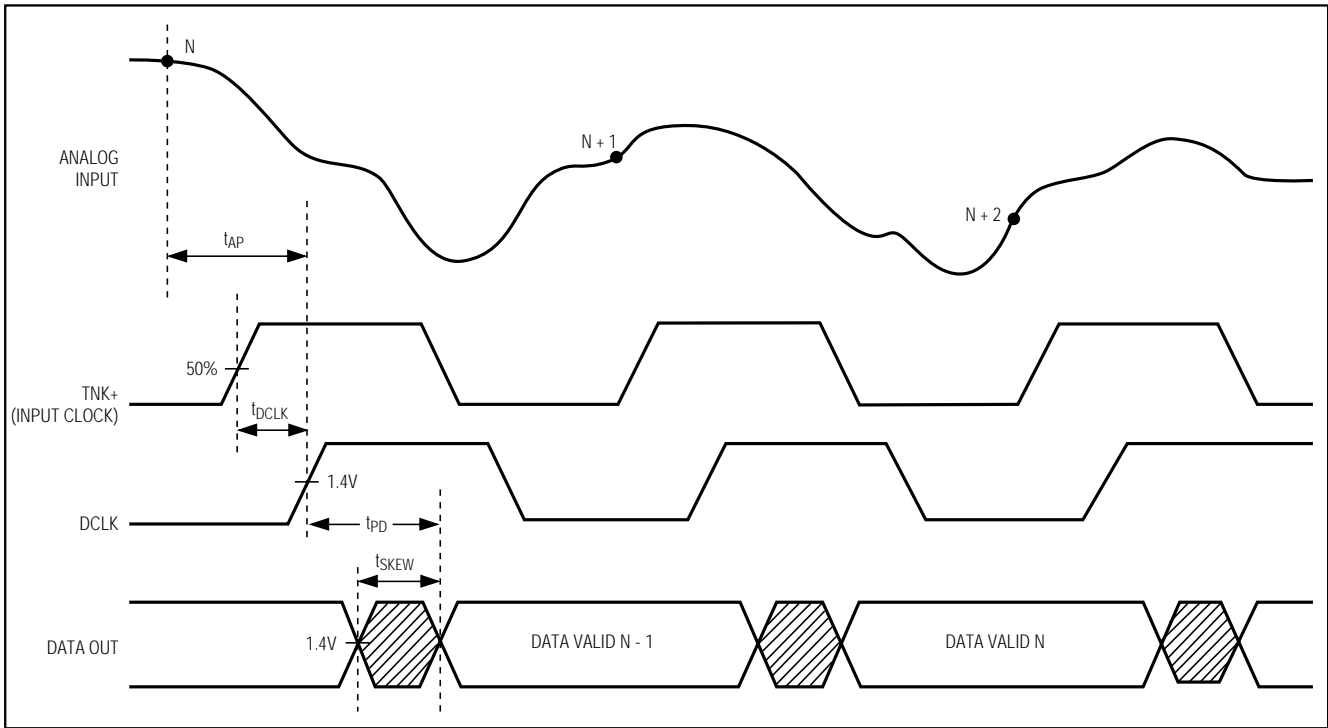Figure 7. External-Clock-Drive Circuit

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Figure 8. MAX1002 Timing Diagram

Output Data Format

The conversion results are output on a dual 6-bit-wide data bus. Data is latched into the ADC output latch following a pipeline delay of one clock cycle (Figure 8). Output data is clocked out of the respective ADC's data-output pins (D_0 through D_5) on the rising edge of the clock output (DCLK), with a DCLK-to-data propagation delay (t_{PD}) of 7.1ns. The MAX1002 outputs are TTL compatible.

Transfer Function

Figure 9 shows the MAX1002's nominal transfer function. Output coding is offset binary with 1LSB = FSR / 63.
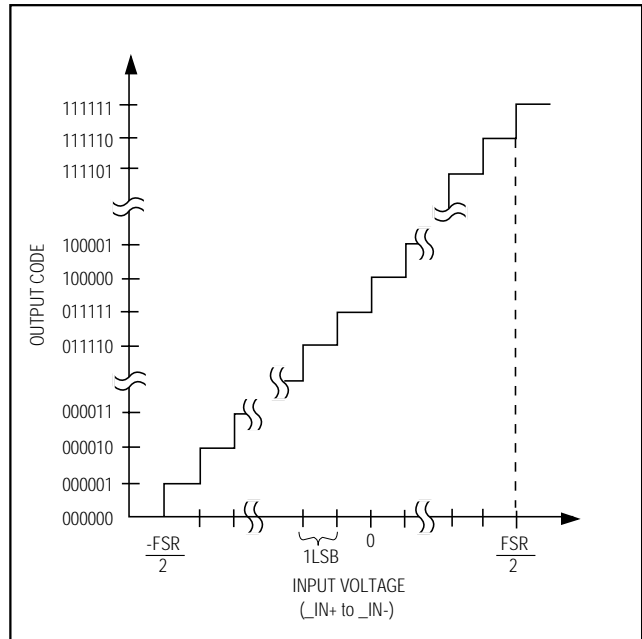

Figure 9. Ideal Transfer Function

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_____Applications Information

Layout, Grounding, and Bypassing

The MAX1002 is designed with separate analog and digital power-supply and ground connections to isolate high-current digital noise spikes from the more sensitive analog circuitry. The high-current digital output ground (OGND) and analog ground (GND) should be at the same DC level, connected at only one location on the board. This provides best noise immunity and improved conversion accuracy. Use of separate ground planes is strongly recommended.

The entire board requires good DC bypassing for both analog and digital supplies. Place the bypass capacitors close to where the power is routed onto the board, i.e., close to the connector. 10µF electrolytic capacitors with low ESR-ratings are recommended. For best effective bits performance, minimize capacitive loading at the digital outputs. Keep the digital output traces as short as possible.

The MAX1002 can operate with one +5V supply. For optimum performance, separate +5V ±5% supplies and bypassing are recommended. Bypass each of the V_{CC} supply pins to its respective GND with high-quality ceramic capacitors located as close to the package as possible (Table 2). Consult the evaluation kit for a suggested layout and bypassing scheme.

Table 2. Bypassing

SUPPLY FUNCTION	V_{CC} / V_{CCO}	BYPASS TO GND/OGND	CAPACITOR VALUE
Analog Inputs	6	7	0.01µF
Oscillator/Clock	8	11	0.01µF
Converter	13	12	0.01µF
Digital Q Output	26	27	47pF
Digital I Output	28	27	47pF
Buffer	36	19	0.01µF

_____Dynamic Performance

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum A/D noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 6-bit ADC can do no better than 38dB.

The FFT Plot (see _Typical Operating Characteristics_) shows the result of sampling a pure 20MHz sinusoid at a 60MHz clock rate. This FFT plot of the output shows the output level in various spectral bands. The plot has been averaged to reduce the quantization noise floor and reveal the low-amplitude spurs. This emphasizes the excellent spurious-free dynamic range of the MAX1002.

The effective resolution (or ENOB) the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SINAD - 1.76) / 6.02 (see _Typical Operating Characteristics_).
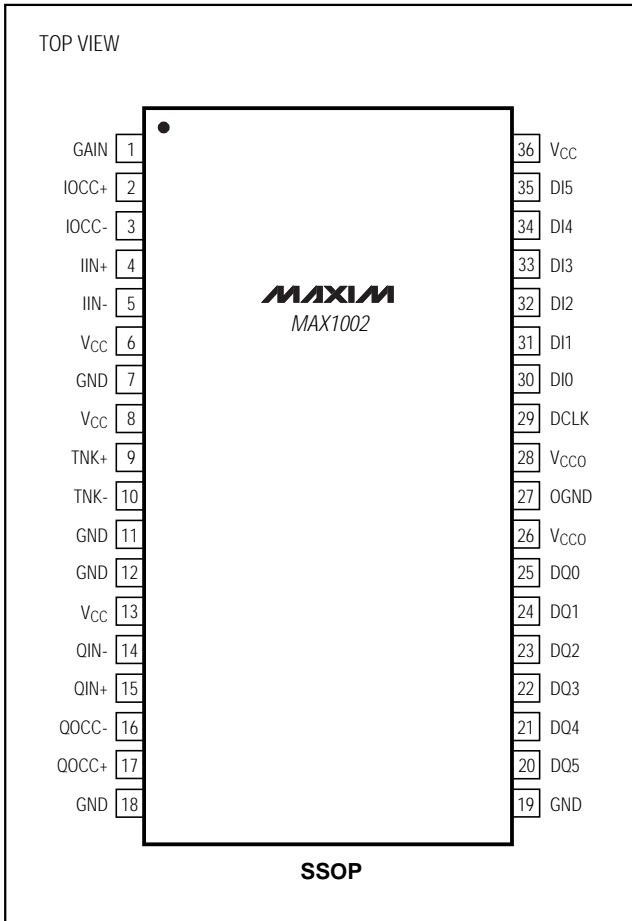
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_____Pin Configuration

TOP VIEW

Pin	Name		Pin	Name
1	GAIN		36	V_{CC}
2	IOCC+		35	DI5
3	IOCC-		34	DI4
4	IIN+		33	DI3
5	IIN-		32	DI2
6	V_{CC}		31	DI1
7	GND		30	DI0
8	V_{CC}		29	DCLK
9	TNK+		28	V_{CCO}
10	TNK-		27	OGND
11	GND		26	V_{CCO}
12	GND		25	DQ0
13	V_{CC}		24	DQ1
14	QIN-		23	DQ2
15	QIN+		22	DQ3
16	QOCC-		21	DQ4
17	QOCC+		20	DQ5
18	GND		19	GND

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SSOP

_____Chip Information

TRANSISTOR COUNT: 6097

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_____**Package Information**

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
e	0.0315		0.80	
E	0.292	0.298	7.42	7.57
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.604	0.610	15.34	15.49	36
D	0.702	0.708	17.83	17.98	44

SSOP2.EPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT
   TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN
   .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

/\/\/XI/\/
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 36/44L, .300X8mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0040	A	1/1