Introduction to GAL® Device Architectures

Overview

In 1985, Lattice Semiconductor introduced a new type of programmable logic device (PLD) that transformed the PLD market: the Generic Array Logic (GAL) device. The $E^2CMOS^{®}$ technology of the GAL devices gave them significant advantages over their bipolar PAL counterparts; not only could GAL devices be programmed quickly and efficiently, but they could also be erased and reprogrammed. Today, Lattice is the leading supplier, worldwide, of low-density PLDs. Industry leading performance, low power E^2CMOS technology, 100% testability and 100% programming yields make the GAL family the preferred choice among system designers.

The GAL family includes fourteen distinct product architectures, with a variety of performance levels specified across commercial, industrial, and military (MIL-STD-883) operating ranges, to meet the demands of any system logic design.

These GAL products can be segmented into three broad categories:

Base Products - Aimed at providing superior design alternatives to bipolar PLDs, these five architectures replace over 98% of all bipolar PAL devices. The GAL16V8 and GAL20V8 replace forty-two different PAL devices. The GAL22V10, GAL20RA10, and GAL20XV10 round out the base products. These GAL devices meet and, in most cases, beat bipolar PAL performance specifications while consuming significantly lower power and offering higher quality and reliability via Lattice's electrically reprogrammable E^2CMOS technology. High-speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

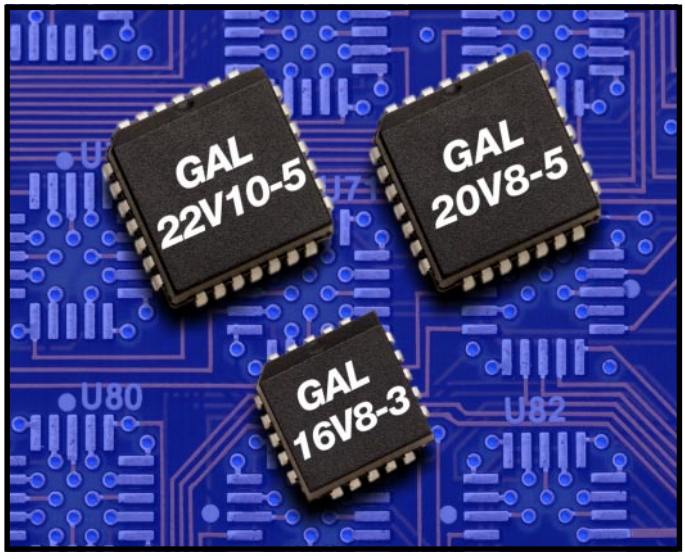
Extension Products – These products build upon the Base GAL product features to provide enhanced functionality including innovative architectures (GAL18V10, GAL26CV12, GAL6001/6002), 64mA high output drive (GAL16VP8 & GAL20VP8), "Zero power" operation (GAL16V8Z/ZD & GAL20V8Z/ZD) and In-System Programmability™ (ispGAL22V10).

Low Voltage GAL Products – As more system designers move to 3.3V, Lattice provides high-performance 3.3V versions of the popular GAL devices. The standard (GAL16LV8, GAL20LV8 and GAL26CLV12), zero-power (GAL16LV8ZD, GAL20LV8ZD and GAL22LV10Z/ZD) and in-system programmable (ispGAL22LV10) device architectures are all available.

A Product for any System Design Need

Lattice GAL products have the performance, architectural features, low power, and high quality to meet the needs of the most demanding system designs.

Lattice Offers the Broadest Line of High-Performance PLDs.



Introduction to GAL Device Architectures

The GAL16V8 and GAL20V8

The GAL16V8 (20-pin) and GAL20V8 (24-pin) provide the highest speed performance available in the PLD market at 3.5 ns and 5.0 ns respectively. CMOS circuitry allows the GAL16V8 and GAL20V8 low power devices to consume just 75mA typical Icc, which represents a 50% savings in power when compared to bipolar counterparts. Quarter power versions save even more at 45mA Icc.

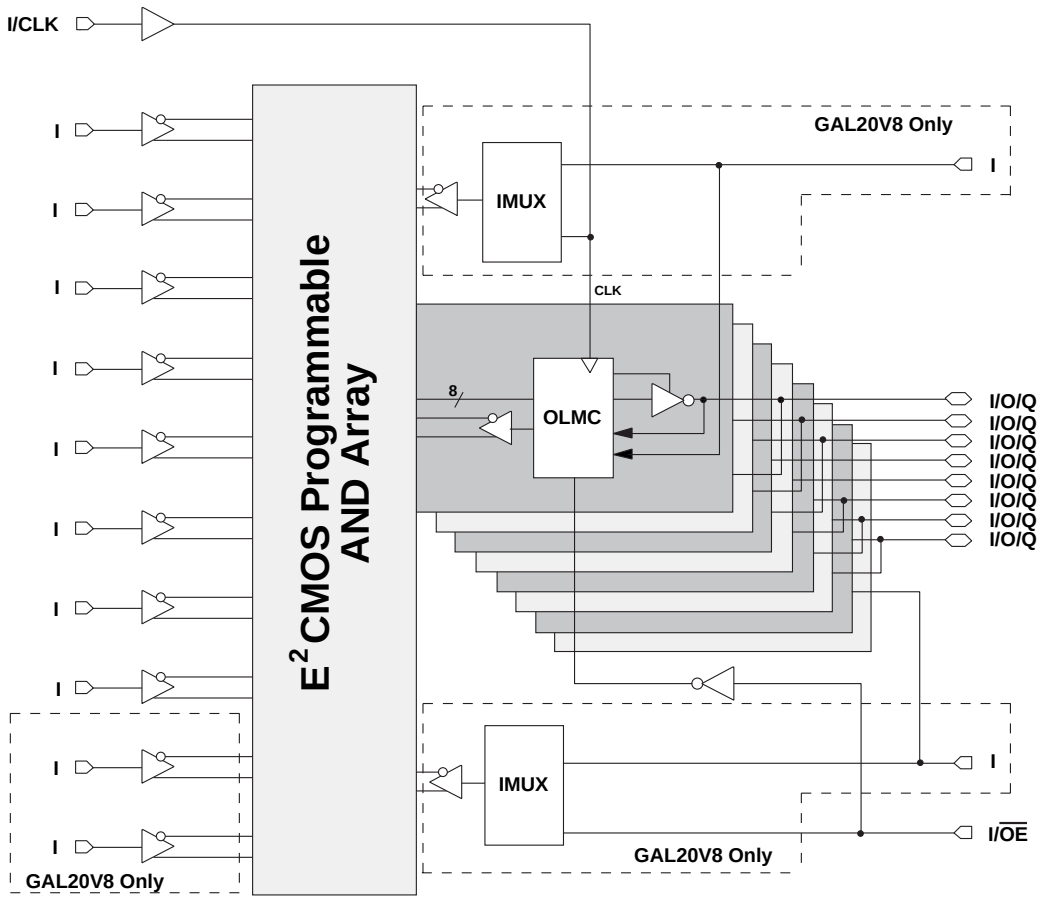
The GAL16V8 is a 20-pin device which contains eight dedicated input pins and eight I/O pins. The GAL20V8 is a 24-pin version of the 16V8 device with 12 dedicated input pins and eight I/O pins. Their generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 and GAL20V8 are the standard PAL architectures. Providing eight OLMCs with eight product terms each, GAL16V8 and GAL20V8 devices are capable of emulating virtually all PAL architectures with full function/fuse map/parametric compatibility.

Output Logic Macrocell

There are three OLMC configuration modes possible in GAL16V8 and GAL20V8 devices: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes; all OLMCs are either simple, complex, or registered (in registered mode, the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs, or a product term can be used to provide individual output

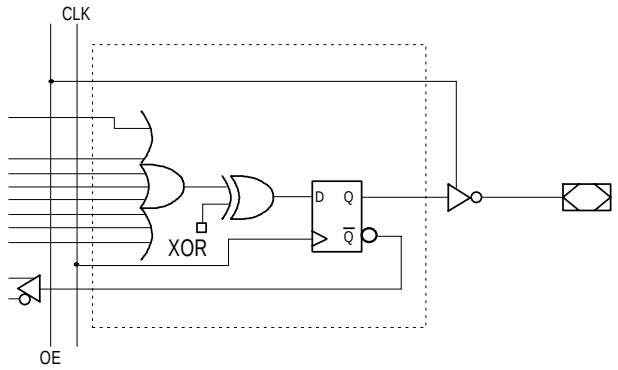
GAL16V8 and GAL20V8 Block Diagram



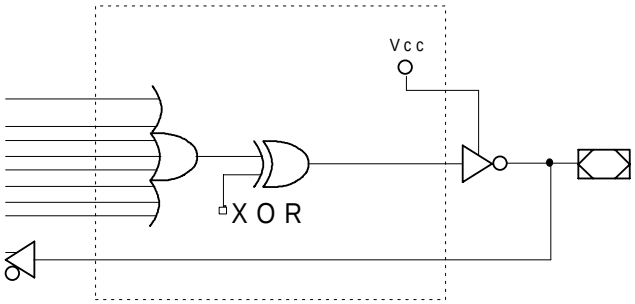
enable control for combinational outputs in the registered mode or combinational outputs in the complex mode.

There is no output enable control in the simple mode. The OLMC provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with standard PAL devices.

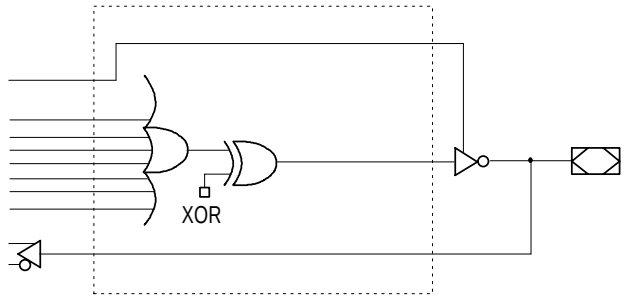
Registered Configuration for Registered Mode



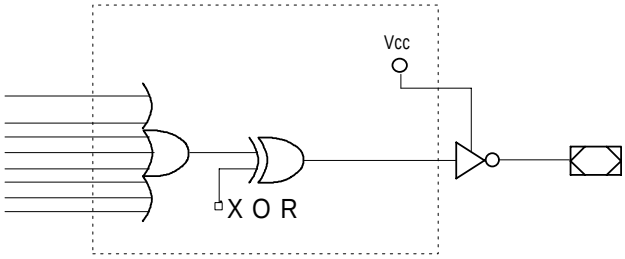
Combinatorial Output with Feedback Configuration for Simple Mode



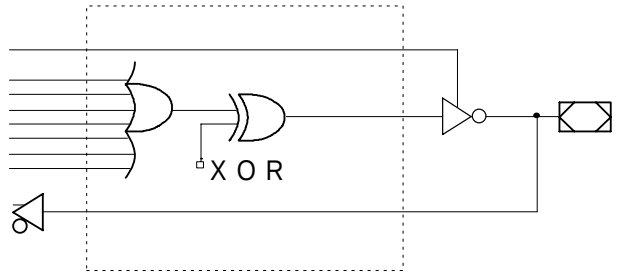
Combinatorial Configuration for Registered Mode



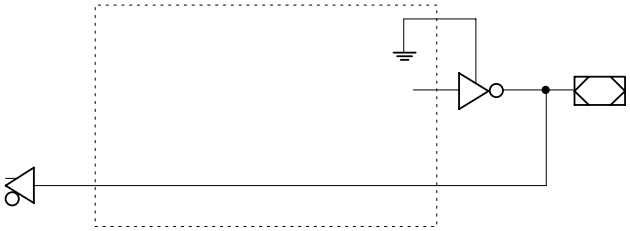
Combinatorial Output Configuration for Simple Mode



Combinatorial Output Configuration for Complex Mode



Dedicated Input Configuration for Simple Mode



The GAL22V10, GAL18V10 and GAL26CV12

Three devices are offered in the high-speed, E^{2}CMOS GAL22V10 family: the GAL22V10 (24-pin), GAL18V10 (20-pin), and GAL26CV12 (28-pin). Each of these devices uses the industry standard 22V10 universal architecture, which provides maximum design flexibility by allowing the OLMC to be configured by the user. The GAL22V10 family low power devices consume just 90mA typical Icc, with quarter power versions consuming only 45mA Icc. The devices differ in the number of I/Os, pins, and product terms offered.

The 24-pin GAL22V10 contains twelve dedicated input pins and ten macrocells and I/O pins. The device has a variable number of product terms per OLMC, ranging from eight to sixteen per output.

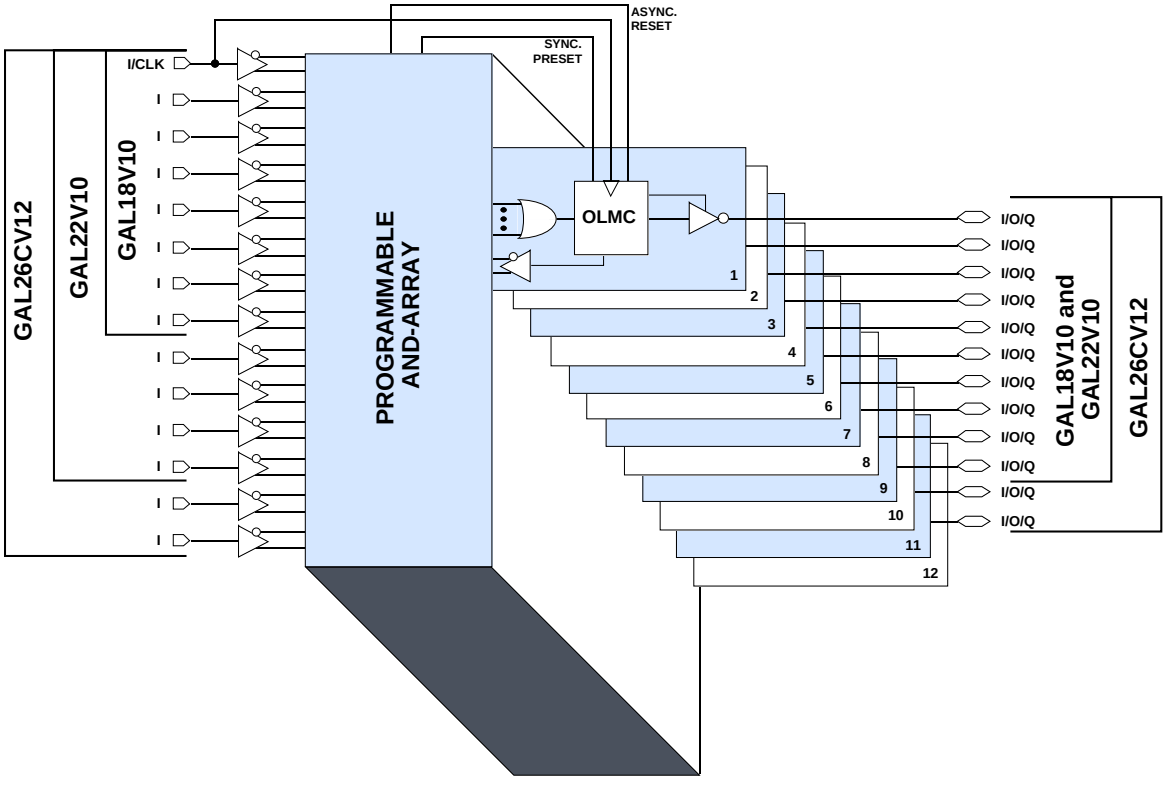
The GAL18V10 is a 20-pin version of the popular 22V10 device. It provides a smaller footprint and lower cost alternative to the 22V10 device. The GAL18V10 contains eight dedicated input pins and ten macrocells and I/O pins.

The GAL26CV12 is a 28-pin version of the 22V10 device. It features more inputs and outputs in order to provide greater functionality and increased I/O. The GAL26CV12 contains fourteen dedicated input pins and twelve macrocells and I/O pins.

Output Logic Macrocell

The GAL22V10, 18V10, and 26CV12 each have a variable number of product terms per OLMC. Of the ten OLMCs available in the GAL22V10, two have access to eight product terms, two have ten product terms, two have 12 product terms, two have 14 product terms, and two have 16 product terms. Of the ten OLMCs available in the GAL18V10, eight have access to eight product terms, and two have ten product terms. Of the 12 OLMCs available in the GAL26CV12, eight have access to eight product terms, two have ten product terms, and two have 12 product terms.

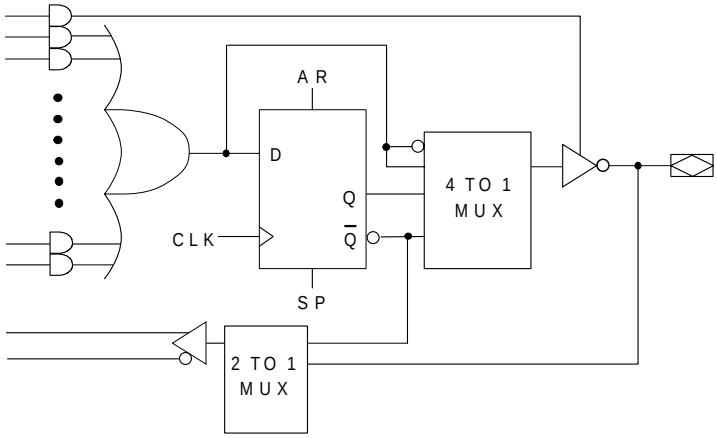
GAL22V10, GAL18V10 and GAL26CV12 Block Diagram



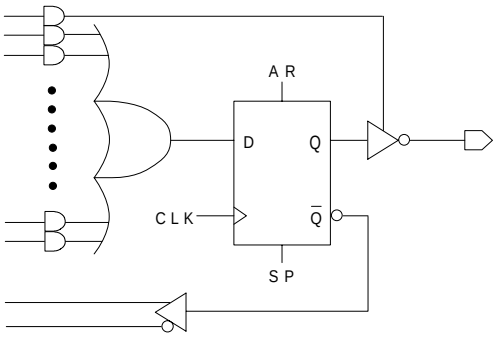
The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinational or registered mode. This allows the user to reduce the overall number of product terms required in a design and/or to invert the output signal.

GAL22V10 family devices have a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs.

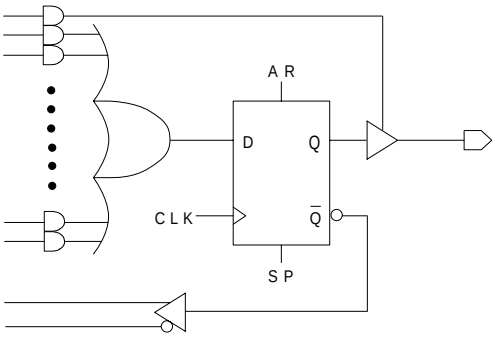
GAL22V10, GAL18V10 and GAL26CV12 Output Logic Macrocell



Output Logic Macrocell Configuration (Registered Mode)

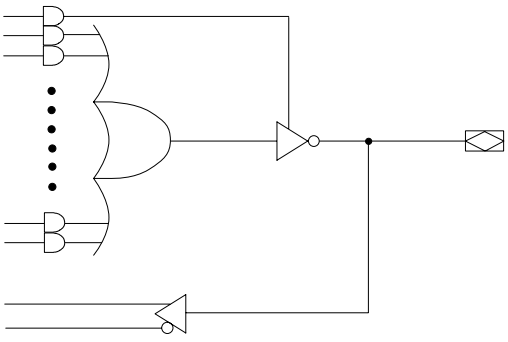


Active Low

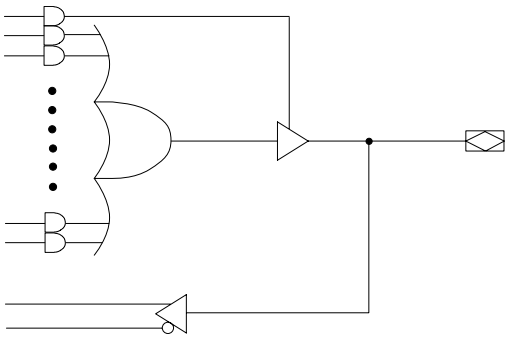


Active High

Output Logic Macrocell Configuration (Combinatorial Mode)



Active Low



Active High

The GAL20RA10

The GAL20RA10 (24-pin) supports high performance, asynchronous logic. It is a direct parametric compatible CMOS replacement for the PAL20RA10 device. However, Lattice's E^2CMOS circuitry achieves power levels as low as 75mA typical Icc, which represents a substantial savings in power when compared to bipolar counterparts like the PAL20RA10.

The GAL20RA10 contains ten dedicated input pins and ten I/O pins. As with other GAL devices, it has user-configurable OLMCs.

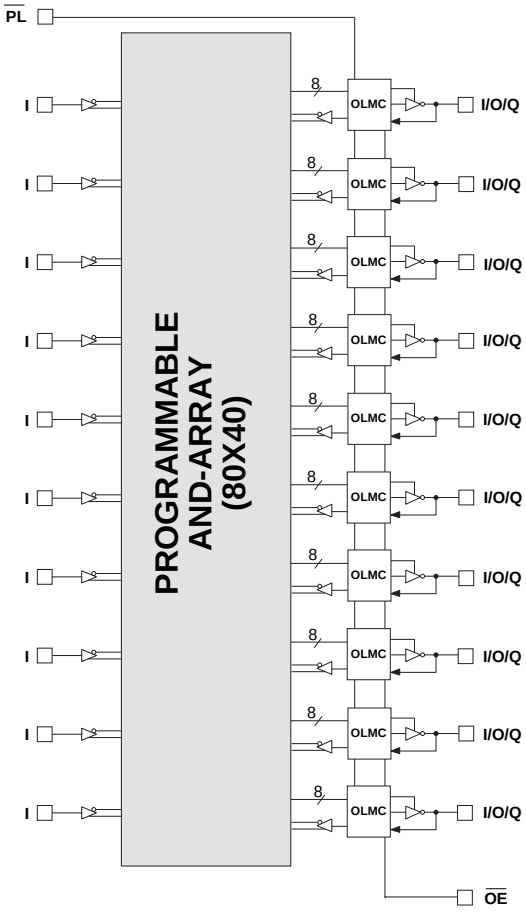
Output Logic Macrocell

The GAL20RA10 OLMC consists of ten D flip-flops with individual asynchronous programmable reset, preset, and clock product terms. The four product terms and an Exclusive-OR gate provide a programmable polarity D-input to each flip-flop. An output enable term, combined with a dedicated output enable pin, provide tri-state control of each output. Each OLMC has a flip-flop bypass, allowing any combination of registered or combinational outputs.

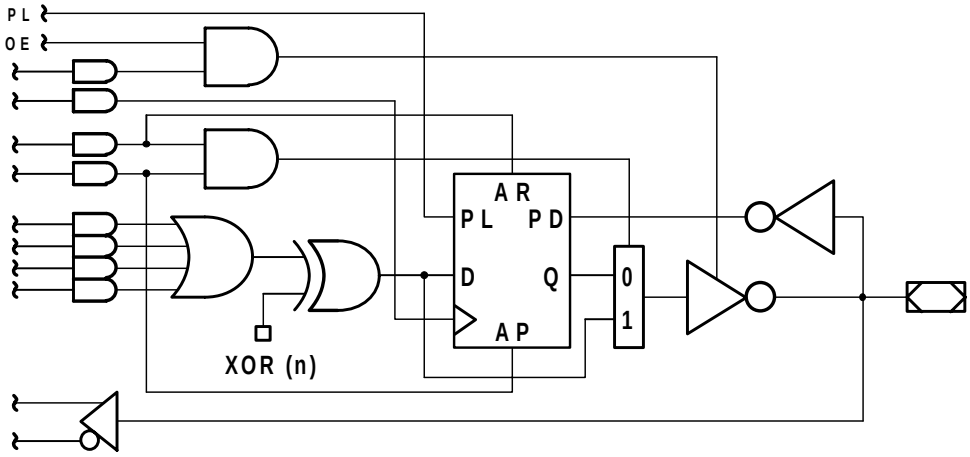
An independent clock control product term is provided for each GAL20RA10 macrocell. Data is clocked into the flip-flop on the active edge of the clock product term. The use of individual clock control product terms allows up to ten separate clocks. These clocks can be derived from any pin or combination of pins and/or feedback from other flip-flops. Multiple clock sources allow a number of asynchronous register functions to be combined into a single GAL20RA10. This allows the designer to combine discrete logic functions into a single device.

The polarity of the D-input to each macrocell flip-flop is individually programmable to be active high or low. This is accomplished with a programmable Exclusive-OR gate on the D-input of each flip-flop. While any one of the four logic function product terms are active, the D-input to the flip-flop will be low if the Exclusive-OR bit is set to zero, and high if the Exclusive-OR bit is set to one. It should be noted that the programmable polarity only affects the data latched into the flip-flop on the active edge of the clock product term. The reset, preset, and preload will alter the state of the flip-flop independent of the state of the programmable polarity bit. The ability to program the active polarity of the D-inputs can be used to reduce the total number of product terms used, by allowing the DeMorganization of the logic functions. This logic reduction is accomplished by the logic compiler, and does not require the designer to define the polarity.

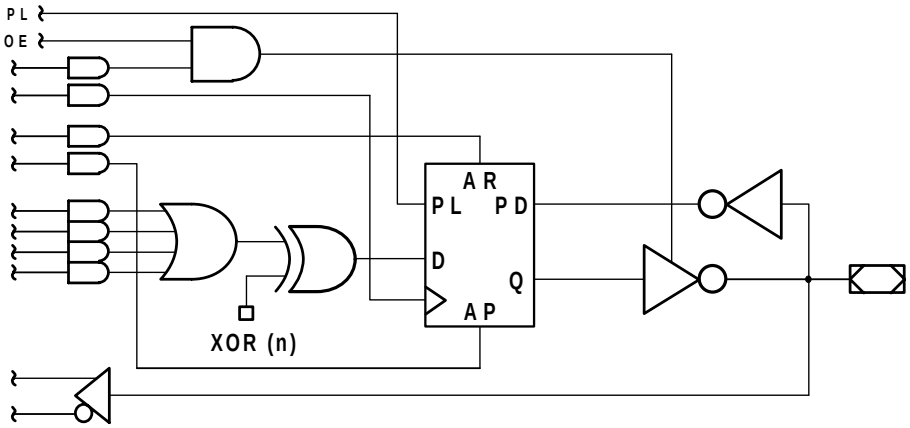
GAL20RA10 Block Diagram



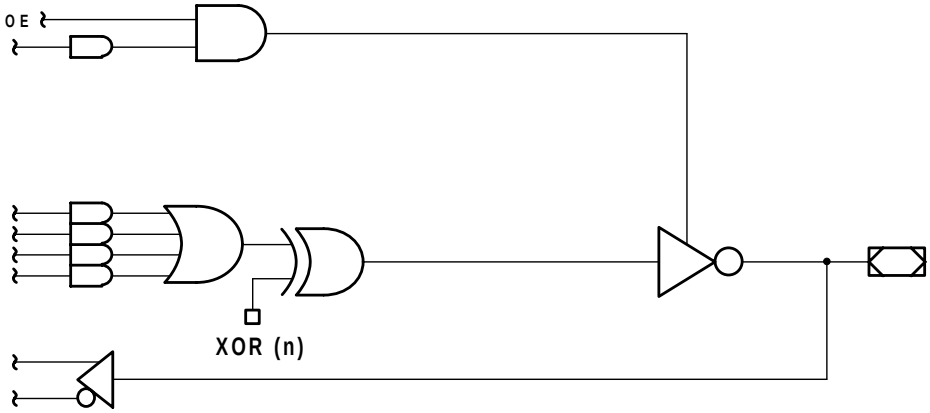
GAL20RA10 Output Logic Macrocell Diagram



Output Logic Macrocell Configuration (Registered with Polarity)



Output Logic Macrocell Configuration (Combinatorial with Polarity)



The GAL20XV10

The GAL20XV10 (24-pin) provides the highest speed, low-density Exclusive-OR PLD available in the market, making it perfect for the fast counters, decoders, or comparators common in video, multimedia, and graphics applications. At 75mA typical Icc, the E^2CMOS GAL20XV10 reduces power by over 50% from bipolar XOR architectures.

The GAL20XV10 is a 24-pin device which contains ten dedicated input pins and ten I/O pins. Its generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20XV10 are the standard PAL architectures. Providing ten OLMCs with four product terms each, the GAL20XV10 is capable of emulating the PAL12L10, PAL20L10, PAL20X10, PAL20X8, and PAL20X4 devices.

Output Logic Macrocell

Each OLMC has an Exclusive-OR gate capability with programmable polarity. This minimizes product term usage.

The GAL20XV10 has two global OLMC architecture configurations that allow it to emulate PAL architectures. Input mode emulates combinatorial PAL devices, whereas Feedback mode emulates registered PAL devices.

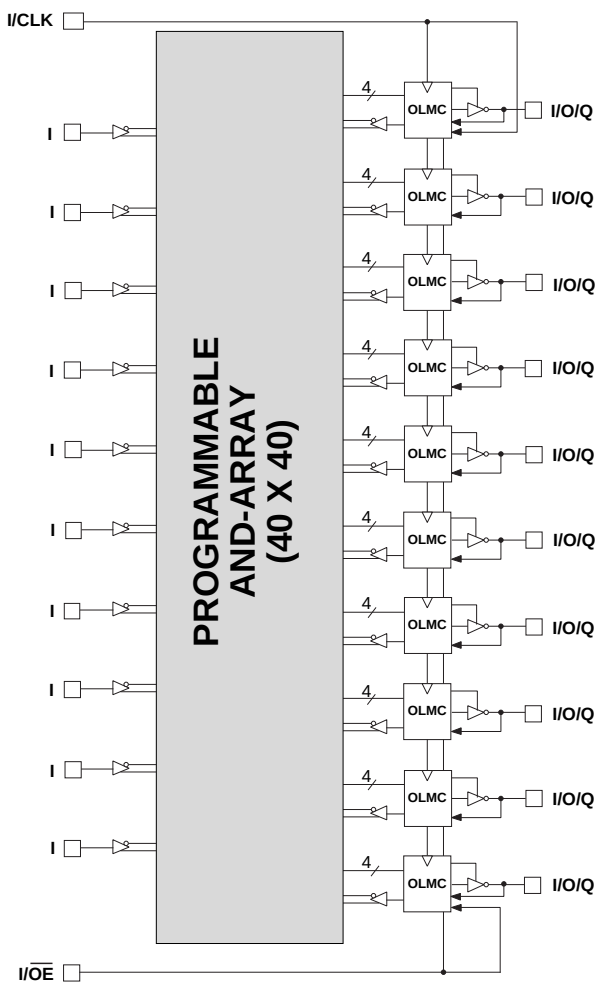
Each OLMC has four possible logic function configurations: XOR Registered, Registered, XOR Combinatorial, and Combinatorial. Four product terms are fed into each macrocell.

When the macrocell is set to the Exclusive-OR Registered configuration, the four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed into a D-type register that is clocked by the low-to-high transition of the I/CLK pin.

When the macrocell is set to Registered configuration, three of the four product terms are used as sum-of-product terms for the D input of the register. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. The XOR bit controls the polarity of the output.

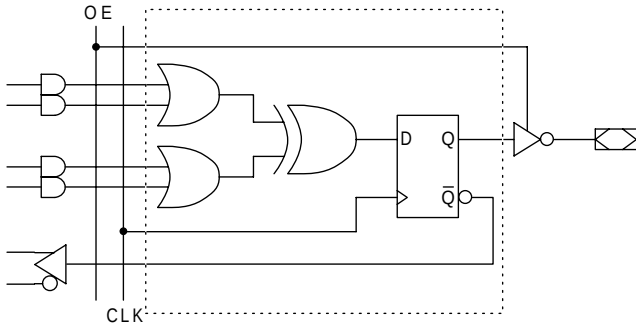
When the macrocell is set to the Exclusive-OR combinatorial configuration, the four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed to an output buffer.

GAL20XV10 Block Diagram

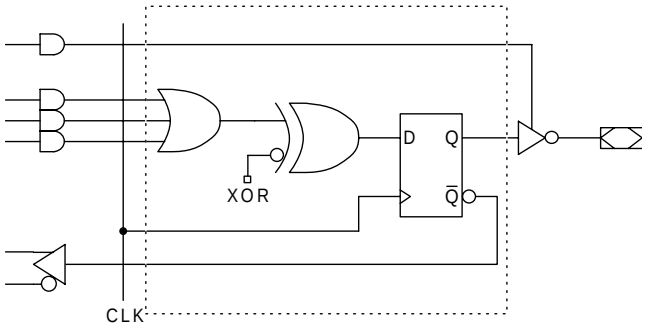


GAL20XV10 OLMC Configurations

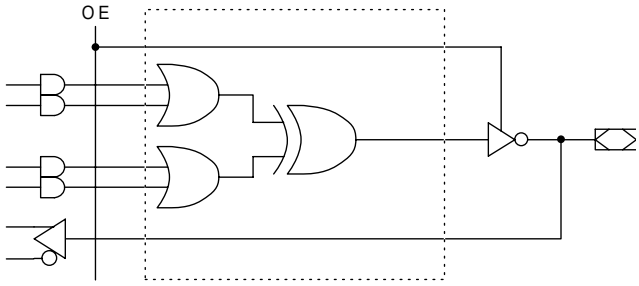
XOR Registered Configuration



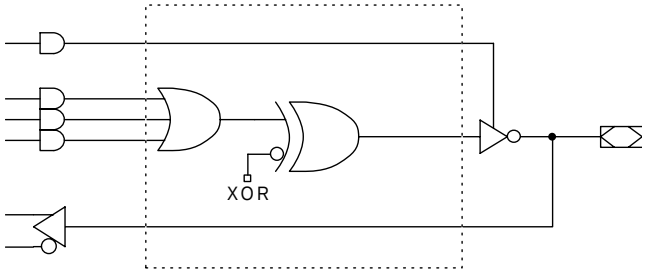
Registered Configuration



XOR Combinatorial Configuration



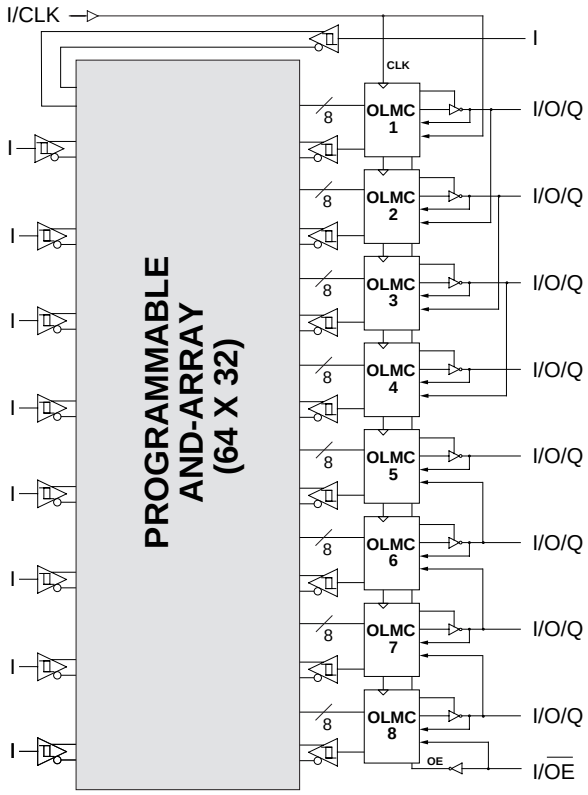
Combinatorial Configuration



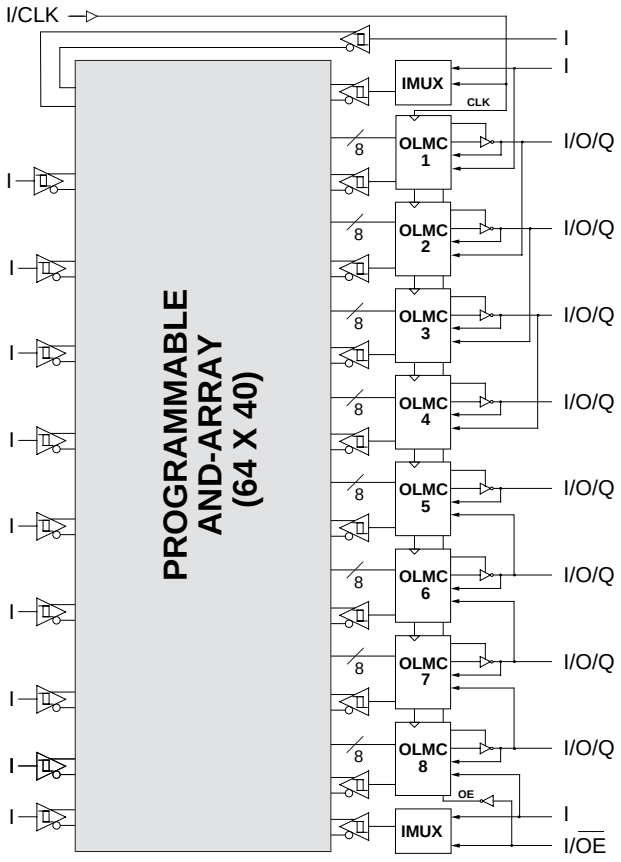
The GAL16VP8 and GAL20VP8

The GAL16VP8 (20-pin) and 20VP8 (24-pin), with 64 mA drive capability, are ideal for bus and memory control applications. System bus and memory interfaces require control logic before driving the bus or memory interface signals. The GAL16VP8 and 20VP8 combine the familiar GAL16V8 and 20V8 architectures (refer to the GAL16V8 and GAL20V8 section in this article) with bus drivers at their outputs. Programmable open-drain or totem pole outputs and 64mA output drive eliminate the need for additional devices to provide bus-driving capability. Also, Schmitt trigger inputs are provided to screen out noise.

GAL16VP8 Block Diagram



GAL20VP8 Block Diagram



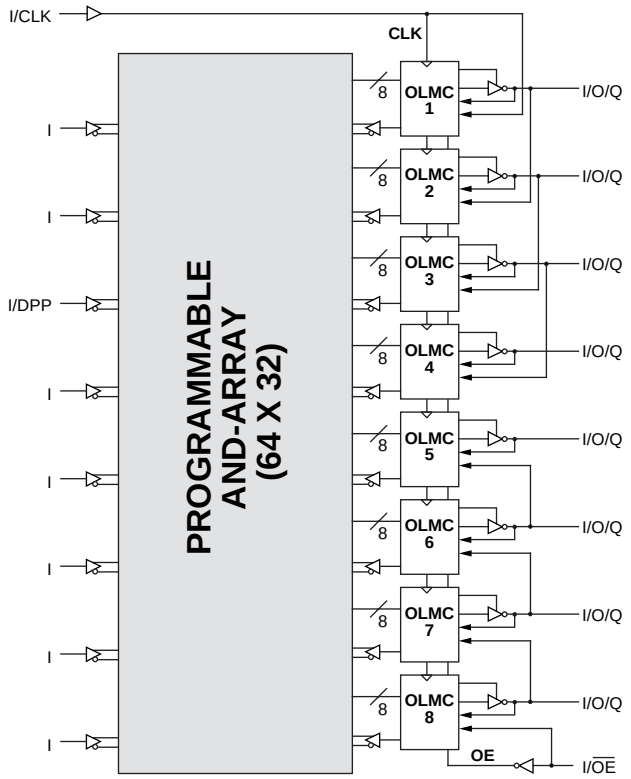
The GAL16V8Z/ZD and GAL20V8Z/ZD

The GAL16V8Z/ZD (20-pin) and GAL20V8Z/ZD (24-pin), at 100uA standby current, provide the highest speed and lowest power combination PLDs available in the market. These devices are ideal for battery powered systems.

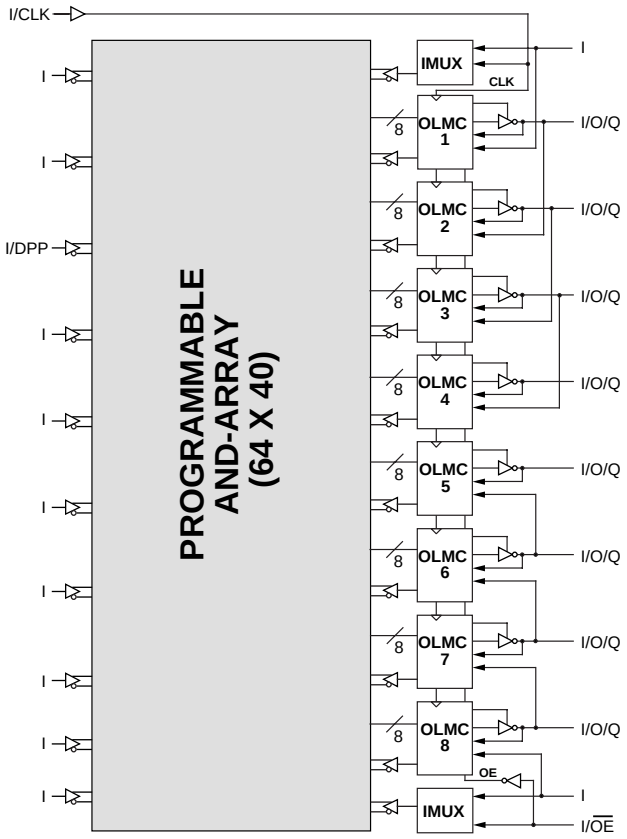
The GAL16V8Z and 20V8Z use Input Transition Detection (ITD) to put the device in standby mode and are capable of emulating the full functionality of the standard GAL16V8 and 20V8 respectively (refer to the GAL16V8 and GAL20V8 section in this article). The GAL16V8ZD and 20V8ZD utilize a dedicated power-down pin (DPP) to put the device in standby mode.

The GAL16V8ZD has 15 inputs available to the AND array, whereas the GAL20V8ZD has 19 inputs available to the AND array.

GAL16V8Z/ZD Block Diagram



GAL20V8Z/ZD Block Diagram



The GAL6001 and GAL6002

Offering an FPLA architecture and superior flexibility in state machine design, the GAL6001 (24-pin) and GAL6002 (24-pin) provide a high degree of functional integration and flexibility in a 24-pin device.

The GAL6001 and GAL6002 have ten programmable Output Logic Macrocells (OLMCs) and eight programmable Buried Logic Macrocells (BLMCs). In addition, there are ten Input Logic Macrocells (ILMCs) and ten I/O Logic Macrocells (IOLMCs). Two clock inputs are provided for independent control of the input and output macrocells.

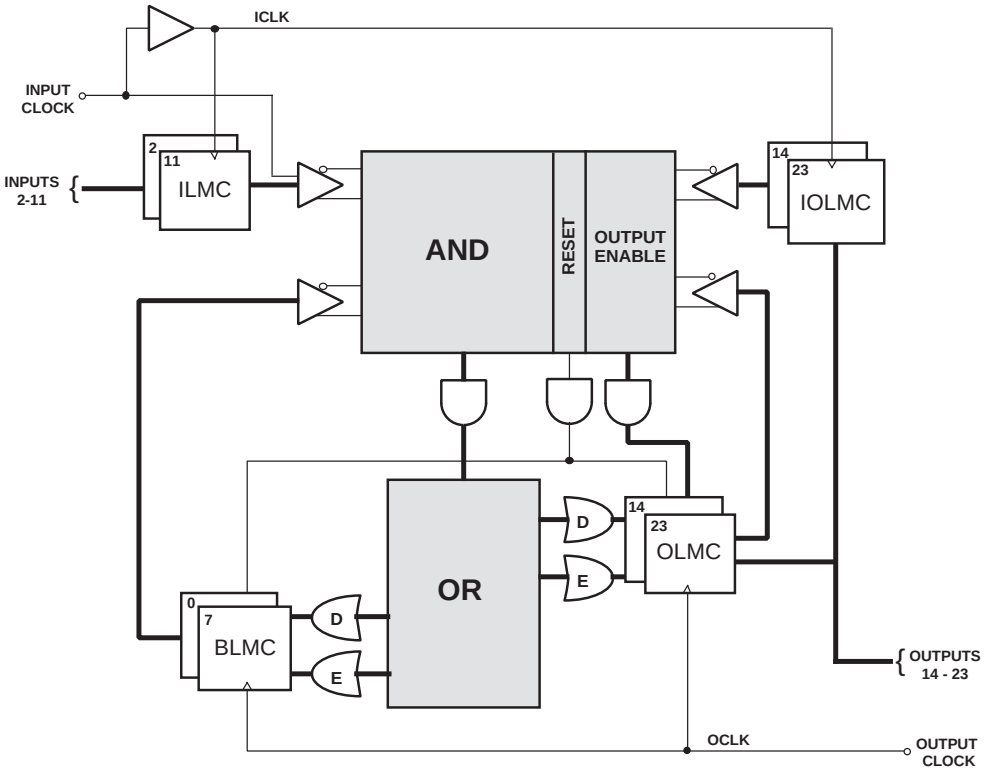
The GAL6001 and 6002 contain two E^2 reprogrammable arrays, an AND array and an OR array. The AND array is organized as 78 inputs by 75 product term outputs. Ten ILMCs, ten IOLMCs, eight BLMC feedbacks, ten OLMC feedbacks, and ICLK comprise the 39 inputs into this array. The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array.

Input Logic Macrocell (ILMC) and I/O Logic Macrocell (IOLMC)

The GAL6001 and 6002 feature two configurable input sections. The ILMC section corresponds to the dedicated input pins, and the IOLMC section corresponds to the I/O pins. On the GAL6001, each input section is configurable as a block for asynchronous, latched, or registered inputs. On the GAL6002, however, each input section is individually configurable as asynchronous, latched, or registered inputs. ICLK is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide system designers with unparalleled design flexibility. With the GAL6001 and 6002, external input registers and latches are not necessary.

For the GAL6001, both the ILMC and the IOLMC are block configurable; however, the ILMC can be configured independently of the IOLMC. For the GAL6002, both the ILMC and the IOLMC are individually configurable, and the ILMC can be configured independently of the IOLMC.

GAL6001 and GAL6002 Block Diagram



Output Logic Macrocell (OLMC) and Buried Logic Macrocell (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMCs), and are useful for building state machines. The second group of macrocells consists of ten cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMCs).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. They may be set to one of three configurations: combinatorial, D-type register with sum term (asynchronous) clock, or D/E-type register. Output macrocells always have I/O capability, with directional control provided by the ten output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the “D” XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all “E” sum terms is selected through the “E” XOR.

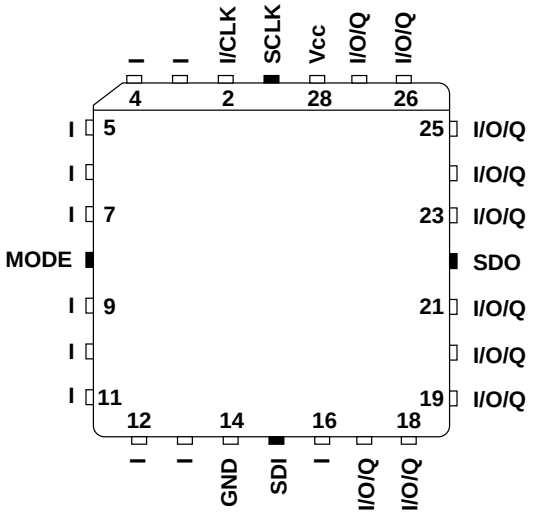
Registers in both the OLMCs and BLMCs feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an output pin, a logic one will occur because of the inverting output buffer.

The ispGAL22V10

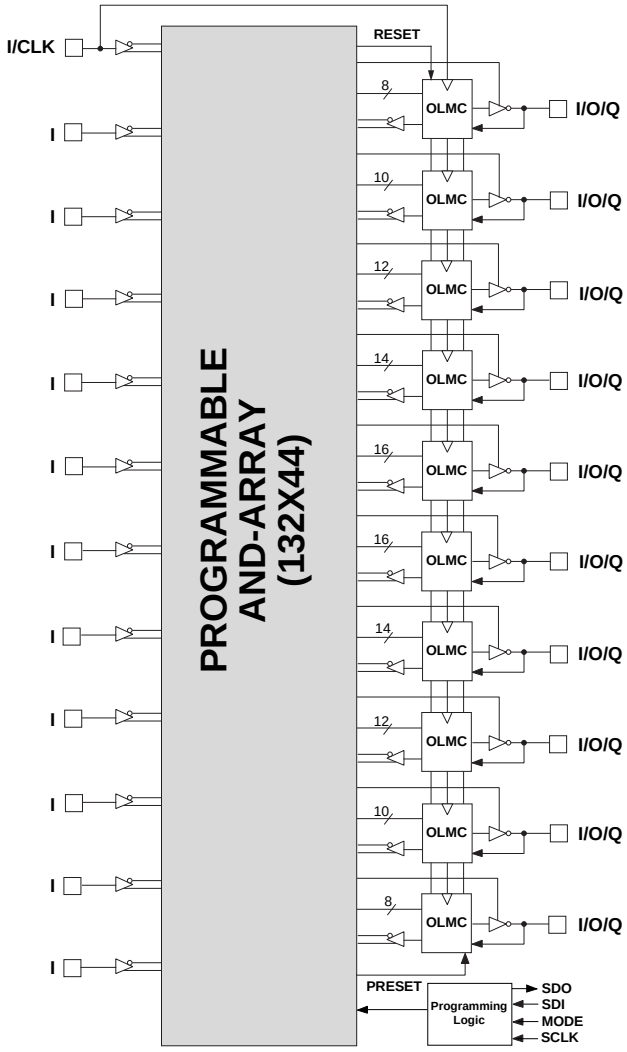
The ispGAL22V10 (28-pin) provides the industry's first in-system programmable 22V10 device. It is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices (refer to the GAL22V10, GAL18V10, and GAL26CV12 section in this article). The standard 28-pin PLCC package provides the same functional pinout at the standard 22V10 PLCC package with the four No-Connect pins being used for ISP interface signals. For space constrained designs, Lattice offers the 28-pin SSOP package.

The in-system programming capability of the ispGAL22V10 allows designers to define and develop systems with capabilities previously unattainable. ISP provides the ability to program and reprogram logic devices while attached to the printed circuit board (PCB). No other logic technology is better for reducing time to market, while assuring the highest system quality and lowest overall cost. With ISP technology, hardware as flexible and easy to modify as software becomes a reality: hardware functions can be programmed and modified in real time to expand product features, shorten system design and debug time, enhance product manufacturability and simplify field upgrades.

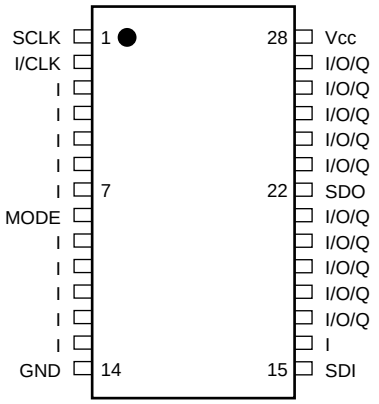
ispGAL22V10 28-Pin PLCC Pinout Diagram



ispGAL22V10 Block Diagram



ispGAL22V10 28-Pin SSOP Pinout Diagram



Low Voltage GAL Products

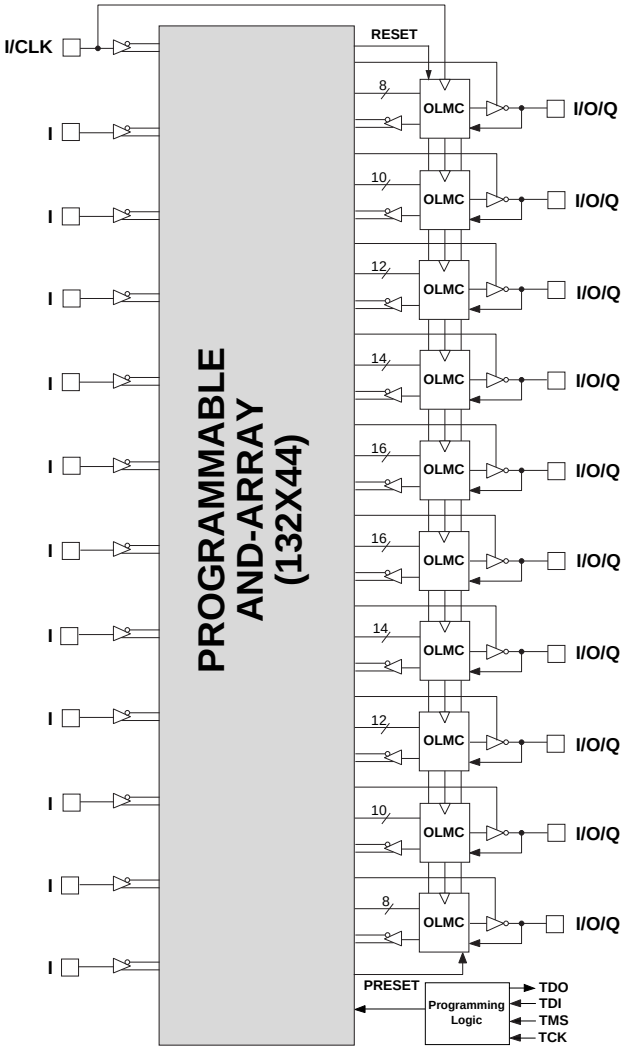
The low voltage GAL products are 3.3V versions of the GAL architectures. The low voltage GAL products from Lattice include the most popular standard GAL architectures as well as the extension architectures. The standard architecture devices include the GAL16LV8, GAL20LV8 and GAL26CLV12. Zero-power devices available include the GAL16LV8ZD, GAL20LV8ZD and GAL22LV10Z/ZD. The ispGAL22LV10 brings in-system programmability to 3.3V GAL systems.

The GAL16LV8, GAL20LV8 and GAL26CLV12 are 3.3V versions of the GAL16V8, GAL20V8 and GAL26CV12 architectures. The device fuse maps are the same between the 3.3V and 5V devices. Refer to the previous architecture discussions for the 5V standard devices.

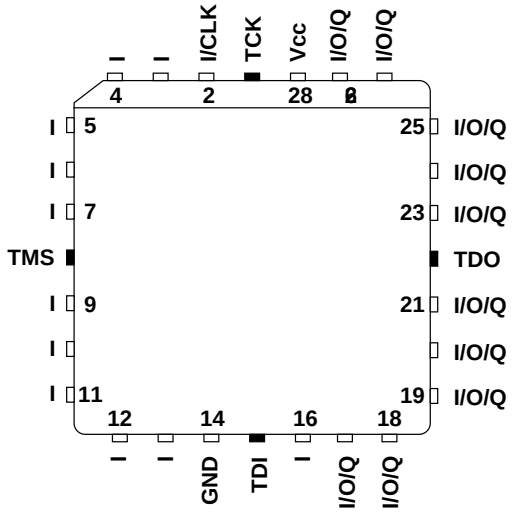
The GAL16LV8ZD, GAL20LV8ZD and GAL22LV10Z/ZD devices are 3.3V versions of the GAL16V8ZD, GAL20V8ZD and GAL22V10Z/ZD architectures. Again, the device fuse maps are the same. Refer to the previous architecture discussions for the 5V zero-power devices.

The ispGAL22LV10 is a 3.3V version of the 22V10 architecture, allowing in-system programming with 3.3V TTL signals. Refer to the GAL22V10, GAL18V10 and GAL26CV12 section of this document for an architecture description. The ispGAL22LV10 differs from the ispGAL22V10 in that it uses the boundary scan (IEEE 1149.1) state machine for programming instead of the proprietary Lattice ISP state machine. The ispGAL22LV10 is available in the 28-pin PLCC package with four no connect pins used for the boundary scan test access port (TAP) pins. In-system programmability allows the use of the smaller 28-pin SSOP package.

ispGAL22LV10 Block Diagram



ispGAL22LV10 28-Pin PLCC Pinout Diagram



ispGAL22LV10 28-Pin SSOP Pinout Diagram