38-to-38 Bit Crosspoint Switch Using the ispLSI® 8840

Introduction

Applications such as network switching, bus interfacing, distributed systems and reconfigurable computing frequently use Crossbar or Crosspoint switches. Crosspoint switches of varying sizes ranging from 8-bit to 128-bit are available in the market. This application note demonstrates the features of the Lattice ispLSI 8840 by implementing a 38-to-38 bit crosspoint switch. This same design extends beyond the capabilities of most other CPLDs in the market.

Overview

In an N-to-N bit crosspoint switch, the N sources can be connected to any of the N destinations available. Figure 1 shows an N-to-N bit crosspoint switch. The figure shows that Source 1 is now connected to the destination Destn 3. The dot denotes the connection made.

Figure 2 shows the 38-to-38 bit crosspoint switch implementation. The design consists of thirty-eight 38-to-1 multiplexers. Two 6-bit address lines (Sel[5:0] and Address[5:0]) are used to select the source and destination. The destination address lines (Address[5:0]) go to a decode logic which generates 38 enable signals (Enb[0] .. Enb[37]). The select lines to each of the multiplexers are latched by the respective enable signals (Enb[0] .. Enb[37]). Latching the select lines to the multiplexers ensures that the source line continues to be connected to the same destination, even if the destination address changes. This way, a single source can reach multiple destinations. Alternatively, other sources can be connected to any of the available destinations without disturbing the existing connections. The input to each of the select latches comes from the source address lines (Sel[5:0]). The data from the output of the multiplexers are registered to pipeline the system. The registers in the I/O cells are used for this purpose to reduce the Clock-to-Output delay.

ispLSI 8840 Design Implementation

The 38-to-1multiplexer functions in the design have 38 data inputs and six select inputs. This makes it a very wide input function (44 inputs). Most other CPLDs do not offer wide input logic blocks and such multiplexer functions would take up multiple levels of logic. Because the ispLSI 8840 has 44-input Generic Logic Blocks (GLBs), this design will fit into an ispLSI 8840 and only use 305 macrocells.

Figure 1. N-to-N Bit Crosspoint Switch

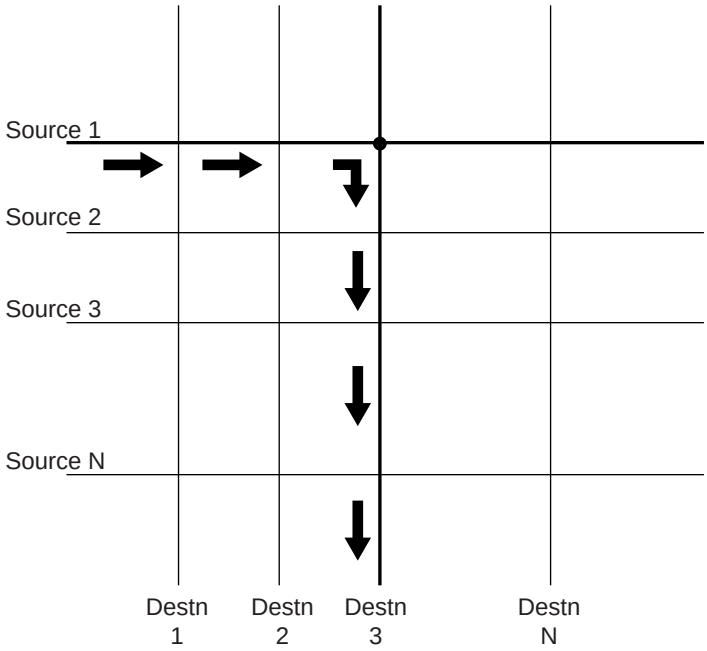

Figure 2. 38-to-38 Bit Crosspoint Switch Implementation

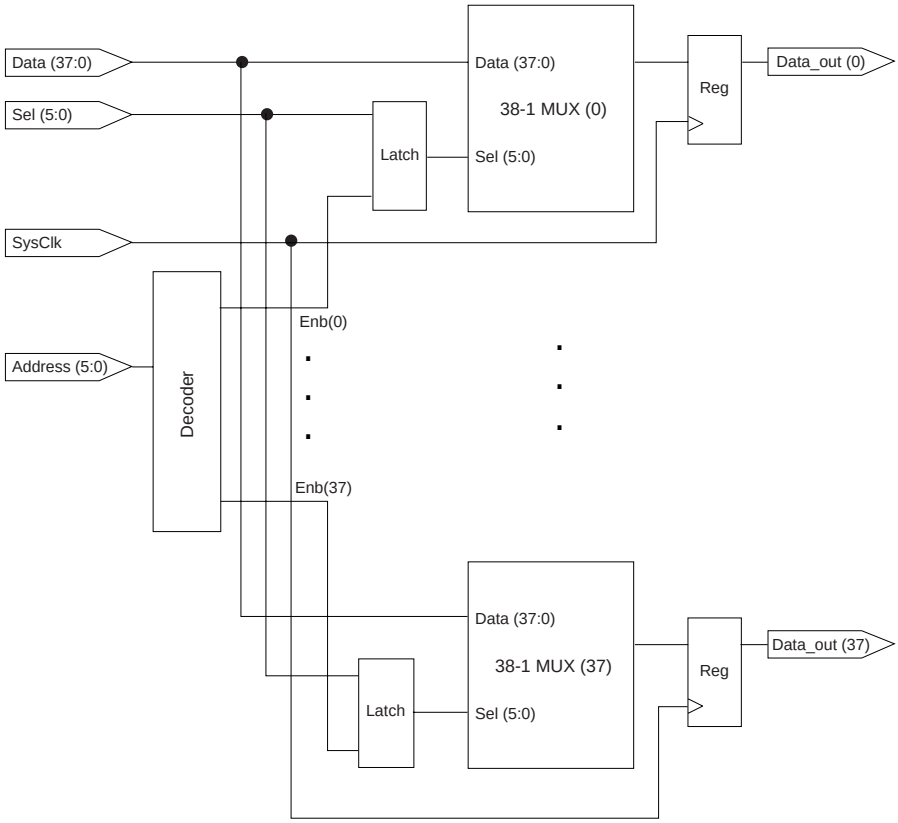

Table 1. Results

Parameter	Lattice ispLSI8840-110LB432	Altera EPF10K30BC356-4
Macrocells (Logic Elements) Used	305 out of 840	1339 out of 1728
Macrocell Utilization	36.3%	77%
Setup Time	31.4 ns	39.5 ns
Clock-to-Output Delay	6.0 ns	15.9 ns

Competitive Analysis

The same design was implemented in an Altera FLEX 10K (EPF10K30) device. Each look-up table within the Flex 10K Logic Element has a maximum of 4 data inputs. This forces the use of carry chains and cascade chains and consequently increases the delay. In the ispLSI 8840, each GLB has a product term sharing array (PTSA). The PTSA allows each macrocell to have a maximum of 28 product terms. With this feature, a function with a product term count of 28 can fit in one level of logic, thereby reducing the delay. Table 1 shows the results obtained from fitting the design in a Lattice ispLSI 8840 and an Altera FLEX 10K30 device.

Conclusion

The Lattice SuperBIG™ ispLSI 8840 CPLD with its superior and innovative architecture is targeted for applications requiring wide input functions, I/O capture registers and an internal tristate bus. The 38-to-38 crosspoint switch implementation results clearly demonstrate the superior performance of the Lattice ispLSI 8840 CPLD over the Altera FLEX 10K FPGA device.