

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6583 is a bit map LCD driver to display graphics or characters.

It contains 3,696 bits display data RAM, microprocessor interface circuits, instruction decoder, 96-segment and 33-common(1 out of 33-driver is prepared for Icon display)drivers.

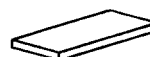
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel mode.

The NJU6583 automatically performs 7 or 15 dots horizontal smooth scroll, therefore the horizontal character scroll is easily controlled by the MPU.

33 x 96 dot graphics or 6-character 2-line by 16 x 16 dot character with icon are displayed by NJU6583 itself.

The wide operating voltage like as 2.4V to 5.5V and low operating current are useful to apply small sized battery operated items.

■ PACKAGE OUTLINE

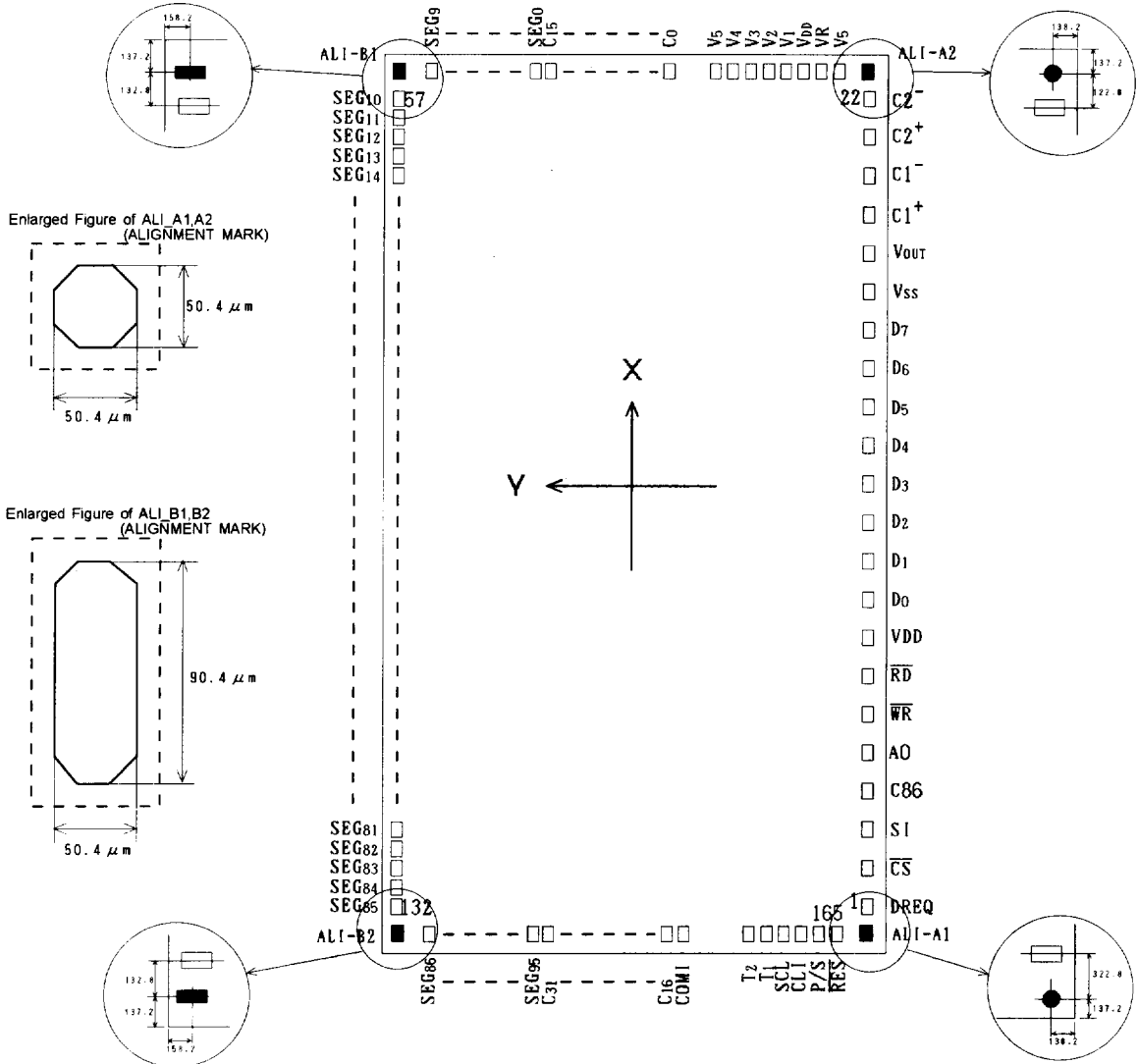


NJU6583C

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 3,696 bits
- LCD Drivers - 32-common + 1 Icon common x 96-segment
- Direct Interface with both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/32 or 1/33 Duty
- Useful Instruction Set
 - Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver Order Assignment, Power Saving, and Scroll ON/OFF.
- Power Supply Circuits for LCD Incorporated
 - Step up Circuits, Regulator, Voltage Follower x 4
- Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage — 2.4V ~ 5.5V
- LCD Driving Voltage — 6.0V ~ 13.5V
- Package Outline — Chip / Bumped Chip / TCP
- C-MOS Technology

PAD LOCATION




■ PAD COORDINATES

Chip Size 6.54mm x 4.11mm(Chip Center X=0um,Y=0um)

PAD No.	Terminal	X=(μ m)	Y=(μ m)
1	DERQ	-2810	-1890
2	CS	-2580	-1890
3	SI	-2430	-1890
4	C86	-2290	-1890
5	A0	-2140	-1890
6	WR	-1990	-1890
7	RD	-1850	-1890
8	V _{DD}	-1720	-1890
9	D ₀	-1400	-1890
10	D ₁	-900	-1890
11	D ₂	-400	-1890
12	D ₃	100	-1890
13	D ₄	600	-1890
14	D ₅	1100	-1890
15	D ₆	1600	-1890
16	D ₇	2100	-1890
17	V _{SS}	2450	-1890
18	V _{OUT}	2560	-1890
19	C1 ⁺	2670	-1890
20	C1 ⁻	2790	-1890
21	C2 ⁺	2900	-1890
22	C2 ⁻	3010	-1890
23	V ₆	3110	-1700
24	VR	3110	-1590
25	V _{DD}	3110	-1480
26	V ₁	3110	-1370
27	V ₂	3110	-1250
28	V ₃	3110	-1140
29	V ₄	3110	-1030
30	V ₅	3110	-920
31	C ₀	3110	-720
32	C ₁	3110	-640
33	C ₂	3110	-560
34	C ₃	3110	-480
35	C ₄	3110	-400
36	C ₅	3110	-320
37	C ₆	3110	-240
38	C ₇	3110	-160
39	C ₈	3110	-80
40	C ₉	3110	0
41	C ₁₀	3110	80
42	C ₁₁	3110	160
43	C ₁₂	3110	240
44	C ₁₃	3110	320
45	C ₁₄	3110	400
46	C ₁₅	3110	480
47	SEG ₀	3110	560
48	SEG ₁	3110	640
49	SEG ₂	3110	720
50	SEG ₃	3110	800

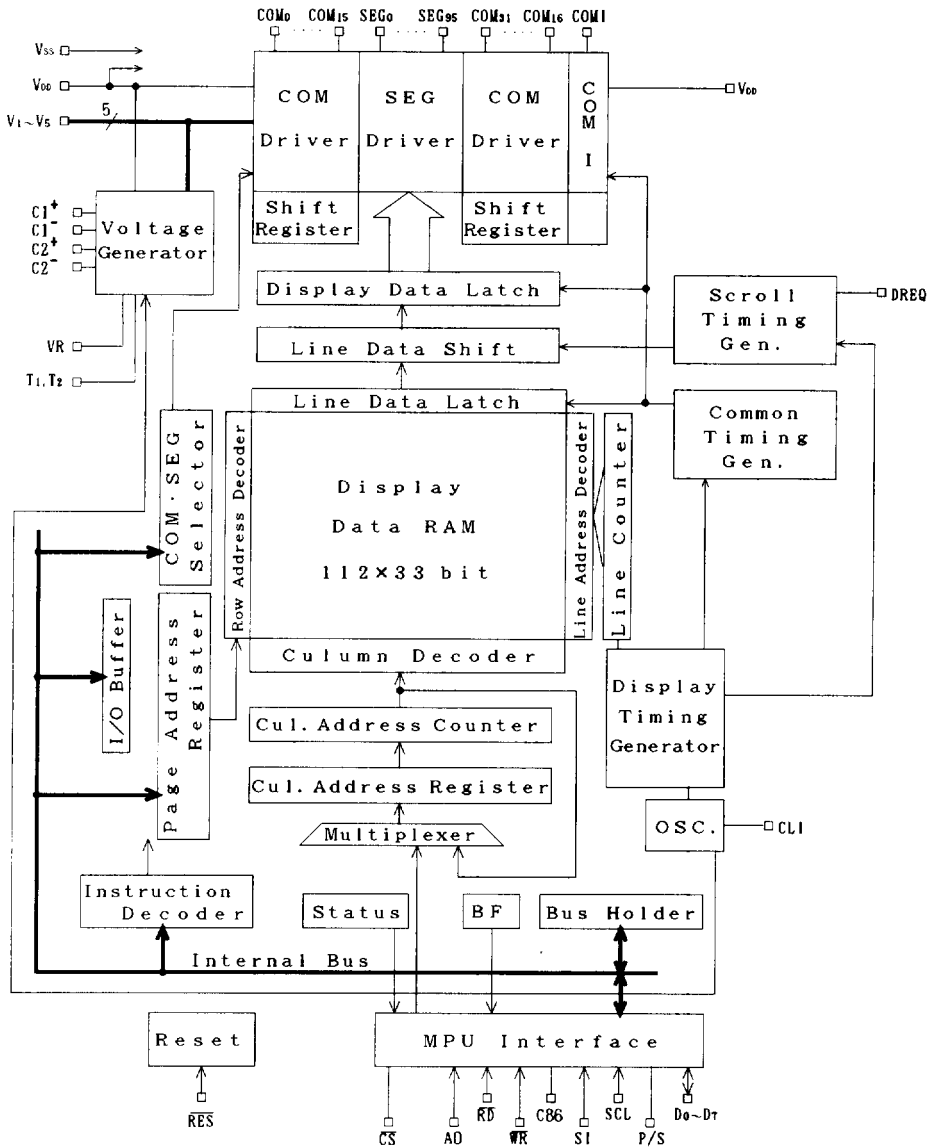
PAD No.	Terminal	X=(μ m)	Y=(μ m)
51	SEG ₄	3110	880
52	SEG ₅	3110	960
53	SEG ₆	3110	1040
54	SEG ₇	3110	1120
55	SEG ₈	3110	1200
56	SEG ₉	3110	1280
57	SEG ₁₀	3000	1890
58	SEG ₁₁	2920	1890
59	SEG ₁₂	2840	1890
60	SEG ₁₃	2760	1890
61	SEG ₁₄	2680	1890
62	SEG ₁₅	2600	1890
63	SEG ₁₆	2520	1890
64	SEG ₁₇	2440	1890
65	SEG ₁₈	2360	1890
66	SEG ₁₉	2280	1890
67	SEG ₂₀	2200	1890
68	SEG ₂₁	2120	1890
69	SEG ₂₂	2040	1890
70	SEG ₂₃	1960	1890
71	SEG ₂₄	1880	1890
72	SEG ₂₅	1800	1890
73	SEG ₂₆	1720	1890
74	SEG ₂₇	1640	1890
75	SEG ₂₈	1560	1890
76	SEG ₂₉	1480	1890
77	SEG ₃₀	1400	1890
78	SEG ₃₁	1320	1890
79	SEG ₃₂	1240	1890
80	SEG ₃₃	1160	1890
81	SEG ₃₄	1080	1890
82	SEG ₃₅	1000	1890
83	SEG ₃₆	920	1890
84	SEG ₃₇	840	1890
85	SEG ₃₈	760	1890
86	SEG ₃₉	680	1890
87	SEG ₄₀	600	1890
88	SEG ₄₁	520	1890
89	SEG ₄₂	440	1890
90	SEG ₄₃	360	1890
91	SEG ₄₄	280	1890
92	SEG ₄₅	200	1890
93	SEG ₄₆	120	1890
94	SEG ₄₇	40	1890
95	SEG ₄₈	-40	1890
96	SEG ₄₉	-120	1890
97	SEG ₅₀	-200	1890
98	SEG ₅₁	-280	1890
99	SEG ₅₂	-360	1890
100	SEG ₅₃	-440	1890

PAD No.	Terminal	X=(μ m)	Y=(μ m)
101	SEG ₅₄	-520	1890
102	SEG ₅₅	-600	1890
103	SEG ₅₆	-680	1890
104	SEG ₅₇	-760	1890
105	SEG ₅₈	-840	1890
106	SEG ₅₉	-920	1890
107	SEG ₆₀	-1000	1890
108	SEG ₆₁	-1080	1890
109	SEG ₆₂	-1160	1890
110	SEG ₆₃	-1240	1890
111	SEG ₆₄	-1320	1890
112	SEG ₆₅	-1400	1890
113	SEG ₆₆	-1480	1890
114	SEG ₆₇	-1560	1890
115	SEG ₆₈	-1640	1890
116	SEG ₆₉	-1720	1890
117	SEG ₇₀	-1800	1890
118	SEG ₇₁	-1880	1890
119	SEG ₇₂	-1960	1890
120	SEG ₇₃	-2040	1890
121	SEG ₇₄	-2120	1890
122	SEG ₇₅	-2200	1890
123	SEG ₇₆	-2280	1890
124	SEG ₇₇	-2360	1890
125	SEG ₇₈	-2440	1890
126	SEG ₇₉	-2520	1890
127	SEG ₈₀	-2600	1890
128	SEG ₈₁	-2680	1890
129	SEG ₈₂	-2760	1890
130	SEG ₈₃	-2840	1890
131	SEG ₈₄	-2920	1890
132	SEG ₈₅	-3000	1890
133	SEG ₈₆	-3110	1280
134	SEG ₈₇	-3110	1200
135	SEG ₈₈	-3110	1120
136	SEG ₈₉	-3110	1040
137	SEG ₉₀	-3110	960
138	SEG ₉₁	-3110	880
139	SEG ₉₂	-3110	800
140	SEG ₉₃	-3110	720
141	SEG ₉₄	-3110	640
142	SEG ₉₅	-3110	560
143	C ₃₁	-3110	480
144	C ₃₀	-3110	400
145	C ₂₉	-3110	320
146	C ₂₈	-3110	240
147	C ₂₇	-3110	160
148	C ₂₆	-3110	80
149	C ₂₅	-3110	0
150	C ₂₄	-3110	-80

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PAD No.	Terminal	X=(μ m)	Y=(μ m)
151	C ₂₃	-3110	-160
152	C ₂₂	-3110	-240
153	C ₂₁	-3110	-320
154	C ₂₀	-3110	-400
155	C ₁₉	-3110	-480
156	C ₁₈	-3110	-560
157	C ₁₇	-3110	-640
158	C ₁₆	-3110	-720
159	COMI	-3110	-800
160	T ₂	-3110	-970
161	T ₁	-3110	-1110
162	SCL	-3110	-1260
163	CLI	-3110	-1410
164	P/S	-3110	-1560
165	RES	-3110	-1700
ALIGNMENT	A1	-3130	-1920
ALIGNMENT	A2	3130	-1920
ALIGNMENT	B1	3130	1900
ALIGNMENT	B2	-3130	1900

■ BLOCK DIAGRAM



TERMINAL DESCRIPTION

No.	Symbol	I/O	F u n c t i o n																				
8,25	V _{DD}	Power	V _{DD} =+5V (Less than 4.5V should be apply when voltage tripler using.)																				
17	V _{SS}	GND	V _{SS} = 0V																				
26 27 28 29 23,30	V ₁ V ₂ V ₃ V ₄ V ₅	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. V _{DD} ≥ V ₁ ≥ V ₂ ≥ V ₃ ≥ V ₄ ≥ V ₅ When internal power supply is on, internal circuits generated and supply following LCD bias voltage to V ₁ ~ V ₄ terminals. <table><tr><td>Term.</td><td>V₁</td><td>V₂</td><td>V₃</td><td>V₄</td></tr><tr><td>Volt.</td><td>V₅ +4/5V_{LCD}</td><td>V₅ +3/5V_{LCD}</td><td>V₅ +2/5V_{LCD}</td><td>V₅ +1/5V_{LCD}</td></tr></table> <div>(V_{LCD} =V_{DD} -V₅)</div>	Term.	V ₁	V ₂	V ₃	V ₄	Volt.	V ₅ +4/5V _{LCD}	V ₅ +3/5V _{LCD}	V ₅ +2/5V _{LCD}	V ₅ +1/5V _{LCD}										
Term.	V ₁	V ₂	V ₃	V ₄																			
Volt.	V ₅ +4/5V _{LCD}	V ₅ +3/5V _{LCD}	V ₅ +2/5V _{LCD}	V ₅ +1/5V _{LCD}																			
19 20 21 22	C1 ⁺ C1 ⁻ C2 ⁺ C2 ⁻	O	Step up capacitor connecting terminals. In case of tripler operation, connect the capacitor between C1 ⁺ and C1 ⁻ , C2 ⁺ and C2 ⁻ . In case of doubler operation, connect the capacitor between C2 ⁺ and C2 ⁻ , connect C2 ⁺ to C1 ⁺ , and C1 ⁻ should be open.																				
18	V _{OUT}	O	Step up voltage output terminal. Connect the step up capacitor between this terminal and V _{SS} .																				
24	VR	I	Voltage adjust terminal. V ₅ level is adjusted by external bleeder resistance connect between V _{DD} and V ₅ terminal.																				
161,160	T ₁ , T ₂	I	LCD bias voltage control terminals. ※ Don't Care <table><tr><td>T₁</td><td>T₂</td><td>Step up cir.</td><td>Voltage Adj.</td><td>V/F Cir.</td></tr><tr><td>L</td><td>※</td><td>Available</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr></table>	T ₁	T ₂	Step up cir.	Voltage Adj.	V/F Cir.	L	※	Available	Available	Available	H	L	Not Avail.	Available	Available	H	H	Not Avail.	Not Avail.	Available
T ₁	T ₂	Step up cir.	Voltage Adj.	V/F Cir.																			
L	※	Available	Available	Available																			
H	L	Not Avail.	Available	Available																			
H	H	Not Avail.	Not Avail.	Available																			
9 ~ 16	D ₀ ~ D ₇	I/O	Tri-state bilateral. Data I/O terminal when 8-bit parallel operation.																				
5	A0	I	Connect to the Address bus of MPU. The data on the D ₀ to D ₇ is distinguished Display data or Instruction by this signal. <table><tr><td>A0</td><td>H</td><td>L</td></tr><tr><td>Dist.</td><td>Display Data</td><td>Instruction</td></tr></table>	A0	H	L	Dist.	Display Data	Instruction														
A0	H	L																					
Dist.	Display Data	Instruction																					
165	RES	I	Reset terminal. When the RES terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of RES.																				
2	CS	I	Chip select terminal. Data input/output are available during CS="L".																				
7	RD (E)	I	<When interface with 80 type MPU> RD signal of 80 type MPU input terminal. Active "L". During this signal "L", the data bus becomes as output terminal. <When interface with 68 type MPU> Enable clock of 68 type MPU input terminal. Active "H".																				



No.	Symbol	I/O	F u n c t i o n																		
6	WR (R/W)	I	<p><When interface with 80 type MPU> Connect the 80 type MPU WR signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal.</p> <p><When interface with 68 type MPU> Read/write control signal of 68 type MPU input terminal.</p> <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Read</td><td>Write</td></tr></table>	R/W	H	L	State	Read	Write												
R/W	H	L																			
State	Read	Write																			
4	C86	I	<p>Select the MPU interface type.</p> <table><tr><td>C86</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>68 Type</td><td>80 Type</td></tr></table> <p>C86 terminal should be fixed to V_{DD} or V_{SS}.</p>	C86	H	L	Status	68 Type	80 Type												
C86	H	L																			
Status	68 Type	80 Type																			
3	SI	I	Serial data input terminal.																		
162	SCL	I	Serial data clock signal input terminal. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.																		
164	P/S	I	<p>Serial or parallel interface select terminal.</p> <table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial CLK</td></tr><tr><td>"H"</td><td>CS</td><td>A0</td><td>D₀~D₇</td><td>RD、WR</td><td>—</td></tr><tr><td>"L"</td><td>CS</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr></table> <p>*RAM data and status read operation is impossible when select the serial interface.</p> <ul style="list-style-type: none">• When select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L".• When select the serial interface (P/S="L"), RD and WR must be fix "H" or "L", and D₀ to D₇ becomes to the high impedance state.	P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK	"H"	CS	A0	D ₀ ~D ₇	RD、WR	—	"L"	CS	A0	SI	Write only	SCL
P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK																
"H"	CS	A0	D ₀ ~D ₇	RD、WR	—																
"L"	CS	A0	SI	Write only	SCL																
163	CLI	I	External clock input terminal.																		
1	DREQ	O	Data request signal output terminal.(at the scroll ON) Active"H".																		

No.	Symbol	I/O	F u n c t i o n																				
31 ~ 46	C ₀ ~ C ₁₅	O	LCD drive output terminals. ● Common output terminals : C ₀ to C ₃₁ ● Segment output terminals : SEG ₀ to SEG ₉₅ ▪ Segment output terminal Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM.																				
47 ~ 142	SEG ₀ ~ SEG ₉₅																						
158 ~ 143	C ₁₆ ~ C ₃₁																						
			<table><tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal</th><th>Reverse</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V₂</td></tr><tr><td>L</td><td>V₅</td><td>V₃</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V₂</td><td>V_{DD}</td></tr><tr><td>L</td><td>V₃</td><td>V₅</td></tr></table> ▪ Common Output Terminal Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data.	RAM Data	FR	Output Voltage		Normal	Reverse	H	H	V _{DD}	V ₂	L	V ₅	V ₃	L	H	V ₂	V _{DD}	L	V ₃	V ₅
RAM Data	FR	Output Voltage																					
		Normal	Reverse																				
H	H	V _{DD}	V ₂																				
	L	V ₅	V ₃																				
L	H	V ₂	V _{DD}																				
	L	V ₃	V ₅																				
			<table><tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V₅</td></tr><tr><td>L</td><td>V_{DD}</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V₁</td></tr><tr><td>L</td><td>V₄</td></tr></table>	Scan data	FR	Output Voltage	H	H	V ₅	L	V _{DD}	L	H	V ₁	L	V ₄							
Scan data	FR	Output Voltage																					
H	H	V ₅																					
	L	V _{DD}																					
L	H	V ₁																					
	L	V ₄																					
159	COMI	O	Icon common output terminal. Icon common output when Icon Display instruction execution.																				
			<table><tr><th></th><th>Icon Display ON</th><th>Icon Display OFF</th></tr><tr><td>State</td><td>COM₃₂</td><td>V₁ or V₄</td></tr></table>		Icon Display ON	Icon Display OFF	State	COM ₃₂	V ₁ or V ₄														
	Icon Display ON	Icon Display OFF																					
State	COM ₃₂	V ₁ or V ₄																					



■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction except the status read are inhibited.

The busy flag output from D₇ terminal when status read instruction is executed.

If enough cycle time over than t_{CYC} indicated in the bus timing characteristics is kept, no need to check the busy flag and it realized high performance for the MPU.

(1-2) Line Counter

The Line Counter is reset at the FR signal changing and counts up by synchronizing common signal cycle and generate the line address which addressing the read out line of Display Data RAM.

(1-3) Column Address Counter

The column address counter is 8-bit presettable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to (A0)_H when the Display Data Read/Write instruction is executed. This counter auto-increments (+1) up to (A0)_H but accessing to the display data RAM over than (6F)_H is forbidden.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM correspondence to the Segment Driver.

(1-4) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the data by changing the page, the page address set instruction is required. Page address "4"(D₂="H" and D₁=D₀="L") is Icon RAM area, the data only for the D₀ is valid.

(1-5) Display Data RAM

Display Data RAM consists of 3,696 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

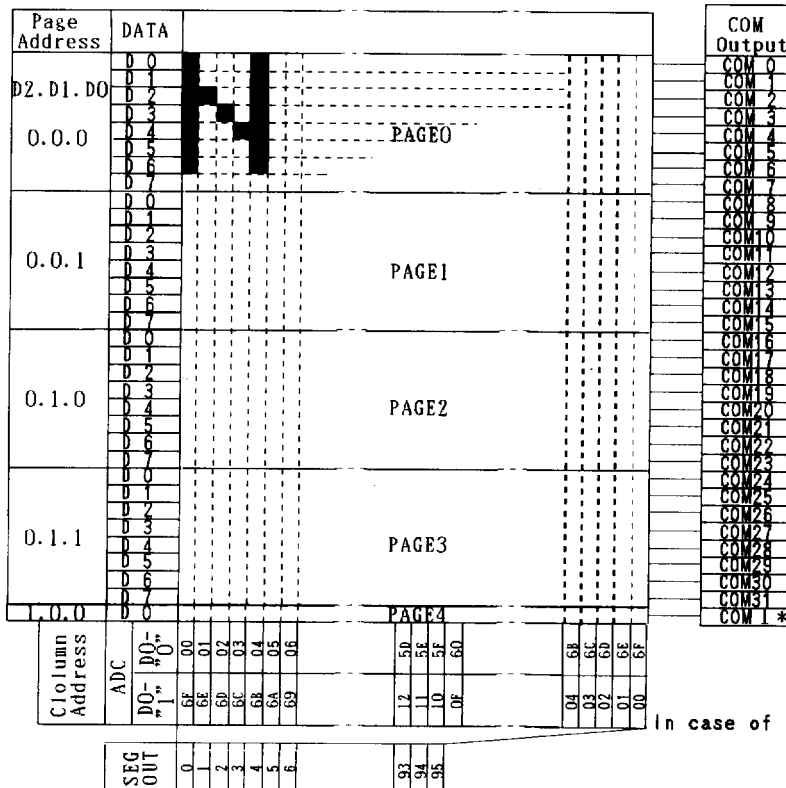
When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM output 112-bit parallel data addressed by the line counter, and these data are set into the Display Data Latch.

This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize re-writing.

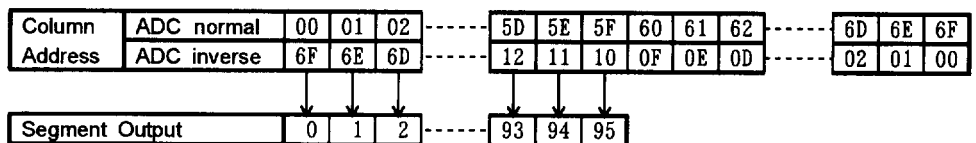
The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.



Correspondence with Display Data RAM and Address
(COM1 can be in case 1/33 of Duty Set.)

Correspondence with column address and LCD output
(When the "On" states, the relation between column address and LCD outputs are shifting)

● No Scroll(same as scroll "Off" state)



● 15 bits scroll

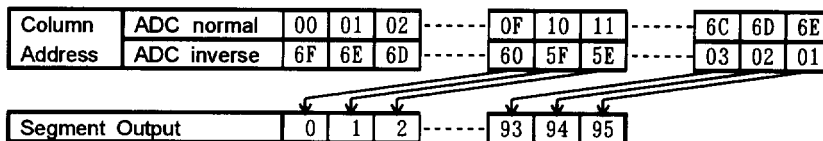


Fig. 1



(1-6) Common and Segment Driver Assignment

The scanning order can be assigned by setting A3 of the Output Assignment Register as shown Table 1.
The location of Segment Drivers are fixed at any time.

Table 1

Register	PAD No.	Common Output Terminals			
A3	Pin name	46	31	158	143
0		C ₁₅	C ₀	C ₁₆	C ₃₁
1		COM15 <----- COM0		COM16 -----> COM31	
		COM16 -----> COM31		COM15 <----- COM0	

The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COM1 is fixed to COM₃₂ timing regardless the other Common Driver assignment.

(1-7) Reset Circuits

The NJU6583 performs following initialization when the RES input is put on the "L" level.

Initialization

- ① Display Off
- ② Normal Display(Non-inverse display)
- ③ Icon Display Reset
- ④ ADC Select : Normal (ADC Instruction D₀ ="0")
- ⑤ Read Modify Write Mode Off
- ⑥ Internal Power supply(Step up) circuits Off
- ⑦ Clear the serial interface register
- ⑧ Set the address (00)_H to the Column Address Counter
- ⑨ Set the page "0" to the Page Address Register
- ⑩ Select the D₃ of the Output Assignment register to "0"
- ⑪ Set the EVR register to (00)_H
- ⑫ Scroll Off
- ⑬ Set the 8x8bit Mode to the Scroll ,Set the speed 4 to the Scroll speed.
- ⑭ Release the All page to the Scroll page.

5

The RES terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface Example". The reset signal require over than 10us RES="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of RES signal, the normal operation is starting.
In case of the internal power supply(Step up) circuits do not use, the RES terminal must be "L" when external power supply turn on. RES="L" input reset internal register and set above default, but oscillation circuits and output terminals like as D₀ through D₇ are no influence.

No initialization by RES when power turns on, will make Hung up condition, therefore please initialize by the RES when power turns on. By the reset Instruction performs only ⑧ through ⑪, ⑬, ⑭ mentioned in above.

The noise into the RES terminal should be cared when of the application design to avoid the error function.



(1-8) LCD Driving

(a) LCD Driving Circuits

NJU6583 incorporate 129 LCD Drivers like as 96 Segment drivers, 32 Common drivers and 1 Icon common driver. Common drivers incorporate the shift register which scanning the common display signal. The combination among the Display data, COM scan signal and FR signal define the LCD driving output voltage. The output wave form is mentioned in the Fig. 8.

(b) Line Data Latch Circuits

Line Data Latch stores 112-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver. The Line Data Latch Circuits latches COMn+1 data at COMn timing to performs smooth data shifting. (Fig. 2)

The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits

The clock for Line Counter and latch signal for the Latch Circuits are generated from display clock. The line address is renewed by synchronizing with display clock and 112 bits display data are latched into display latch circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Line Data Shift Circuits

When the scroll "On" state the Line Data Shift Circuits shift maximum 15 bits toward the SEG 0 which input the line data from Line Data Latch Circuits, then output to Display Data Latch Circuits.

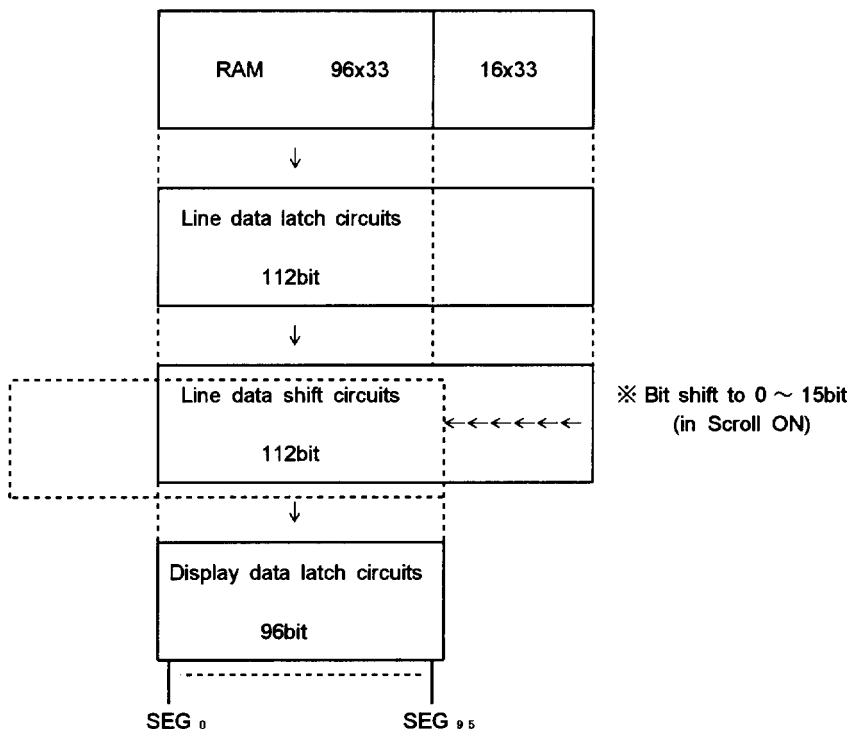
In case of scroll "Off" state, the data input to the Line Data Shift Circuits output to the Display Data Latch without shift.

(e) Display Data Latch Circuits

The Display Data Latch Circuits temporally stores 96 bits display data (which) shift 0 to 15 bits by the Line Data Shift Circuits and output to the segment drivers.

Output RAM Data to Segment

< Data Format >



< Timing >

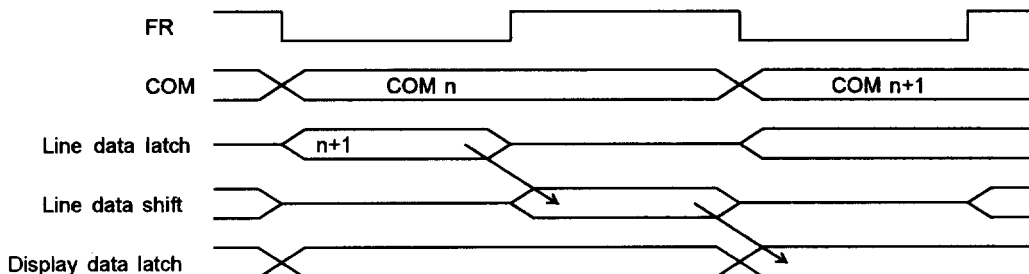


Fig. 2

(f) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock and Driving Signal FR. The Frame Signal FR has a function to generate the 2 frame alternative driving method waveform for the LCD panel.

(g) Common Timing Generation

The common timing is generated by display clock.

Waveform of Display Timing

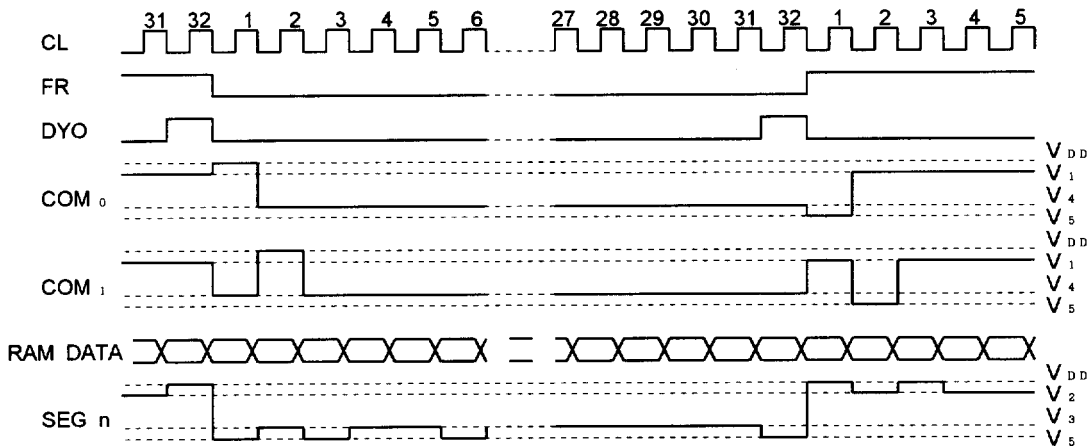


Fig. 3

(h) Fundamental Clock

The Fundamental Clock is input the CLI terminal to external. It is used as display timing signal source and the clock for step up circuits for LCD driving. The fundamental clocks output frequency is divided by 192 which is used as display clock CL.

(i) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Tripler or Doubler) Circuits, Regulation Circuits, and Voltage Follower. Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the large size LCD panel application. If the contrast is no good in those application, please use external power supply supplied more high current.

The suitable values of the capacitors connecting to the V1 to V5 terminals and the step up circuit, the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption in the LCD panel is changeable with the display pattern. Therefore a trial with actual module should be practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction.

When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, voltage follower circuits are off. In this time, the bias voltage of V1, V2, V3, V4, and V5 for the LCD supply from outside, terminals C1+, C1-, C2+, C2-, and VR are open. The status of internal power supply can select by T1 and T2 terminal. The external power supply can be used together with some of internal power supply function.

Table 3.

(*:Don't Care)

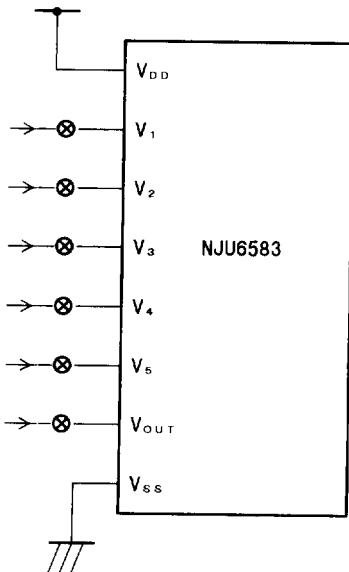
T ₁	T ₂	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term.
L	*	○	○	○	-		
H	L	×	○	○	V _{OUT}	OPEN	
H	H	×	×	○	V ₅ , V _{OUT}	OPEN	OPEN

When (T₁, T₂)=(H, L), the terminal for step up circuits of C1+, C1-, C2+, C2- are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T₁, T₂)=(H, H), terminals for step up circuits and VR are open, and supply the LCD driving voltage from outside due to the Step up circuits and Voltage adjust circuits are stop its operation.



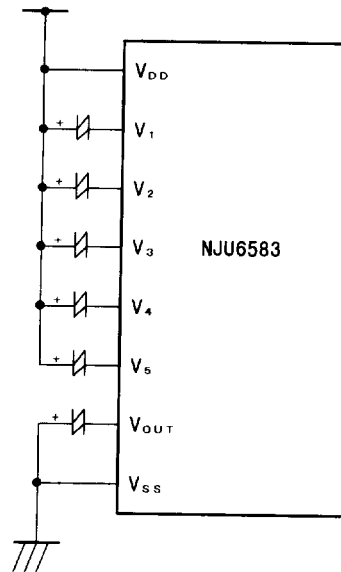
○ Examples for application circuits of the internal Power Supply

(1) None of the internal power supply functions.



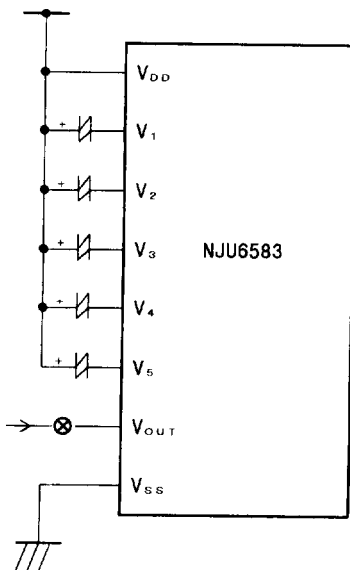
(2) All of the internal power supply functions.
(Step up, Voltage Adj., Buffer(V/F))

(T1, T2) = (L, *) *: Don't care.



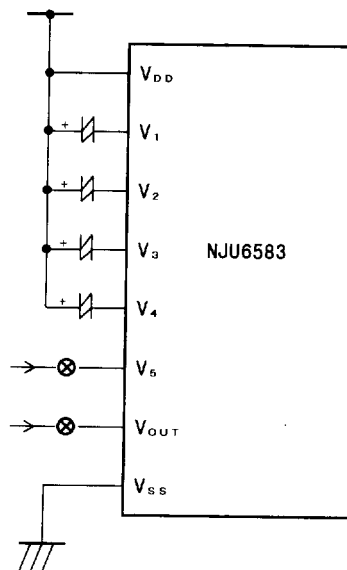
(3) Some of the internal power supply functions.
(Voltage Adjust., Buffer(V/F))

(T1, T2) = (H, L)



(4) Some of the internal power supply functions.
(Buffer(V/F))

(T1, T2) = (H, H)



* ⊗ : These switches should be open during the power save mode.

5

(2) Instruction

The NJU6583 distinguish the signal on the data bus by combination of $\overline{A0}$, \overline{RD} and \overline{WR} . Normally, the busy check is not required as the NJU6583 is operating so first because of the decode of the instruction and execution are performed only depend on the internal timing which not depend on the external clock. In case of serial interface, the data input as MSB first serially.

The Table. 3 shows the instruction codes of the NJU6583.

Table 3. Instruction Code

Instruction		Code											Description
		A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Add. Register
(3)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status			0	0	0	0	0	Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								Read the Data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0	Inverse the On and Off Display 0:Normal 1:Inverse
(10)	Whole Display On	0	1	0	1	0	1	0	0	1	0	0	Whole Display Turns On 0:Normal 1:Whole Disp. On
(11)	Icon Display	0	1	0	1	0	1	0	1	0	1	0	Set the Duty Ratio 0:No Icon 1:With Icon
(12)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(15)	ComOutput / Scroll Set Up	0	1	0	1	1	0	0	A3	M	S1	S0	Set the COM (A3) and Scroll (M,S0,S1)
(16)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0	0:Int. Power Supply Off 1:Int. Power Supply On
(17)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal(external) power supply is turn on
(18)	EVR Register Set	0	1	0	1	0	0	Setting Data					Set the V _s output level to the EVR register
(19)	Power Save (Dual Command)	0	1	0	1	0	1	0	1	1	1	0	Set the Power save Mode
(20)	Scroll Page Set	0	1	0	0	1	*	*	P3	P2	P1	P0	Set the Scroll Page P*=0:Used Scroll P*=1:No Scroll
(21)	Scroll On / Off Set	0	1	0	1	0	1	0	1	0	0	0	Scroll ON/OFF 0:OFF 1:ON
(22)	Data Request Reset	0	1	0	0	0	1	0	0	0	0	0	Reset the Data Request Signal

(*:Don't Care)



(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off

1: Display On

(b) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 4 is a Icon display data area which available only for the D₀.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	*	A ₂	A ₁	A ₀

(*:Don't Care)

A ₂	A ₁	A ₀	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

(c) Column Address

When MPU access the Display Data RAM, page address set(refer(b) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting. This counter auto-increment up to (A0)_H, but accessing to the display data RAM over than (6F)_H is forbidden.

After writing 1 page data, page address setting is required due to page address doesn't increase automatically.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Higher Order	0	1	0	0	0	0	1	A ₇	A ₆	A ₅	A ₄
Lower Order	0	1	0	0	0	0	0	A ₃	A ₂	A ₁	A ₀

A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Column Address
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
.
0	1	1	0	1	1	1	1	6F



(d) Status Read

This instruction read out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.

The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.

0 : Counterclockwise Output(Inverse) Column Address 95-n \leftrightarrow Segment Driver n

1 : Clockwise Output (Normal) Column Address n \leftrightarrow Segment Driver n

(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.

0 : Whole Display "On"

1 : Whole Display "Off"

(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initialization period by $\overline{\text{RES}}$ signal or reset instruction.

0 : —

1 : Initialization Period

(e) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without any address setting after the start address setting.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	WRITE DATA							

(f) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page address. The column address increase "1" automatically when reading, therefore, the MPU can read the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read is required after column address set as explain in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data can not be readout.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	READ DATA							



(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

R/W											
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇								D ₀
0	1	0	1	0	1	0	0	0	0	0	D

D 0: Clockwise Output (Normal)

1: Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Data RAM is no changed by this instruction execution.

R/W											
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇								D ₀
0	1	0	1	0	1	0	0	1	1	1	D

D 0: Normal RAM data "1" correspond to "On"

1: Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction executes the all pixel turns on regardless the contents of the Display Data RAM. In this time, the contents of Display Data RAM is no change and is kept. This instruction takes over precedence over the "Normal or Inverse On/Off Set Instruction".

R/W											
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇								D ₀
0	1	0	1	0	1	0	0	1	0	0	D

D 0: Normal Display

1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the power save mode(refer to the (r) Power Save) .

5

(j) Icon Display

This instruction set the 1/33 duty for the Icon Display. The COM1 terminal operate as COM₃₂ and output the icon display data stored in D₀ of Display Data RAM page 4(refer to the Fig. 1).

R/W											
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇								D ₀
0	1	0	1	0	1	0	1	0	1	0	D

D 0: 1/32 Duty

1: 1/33 Duty

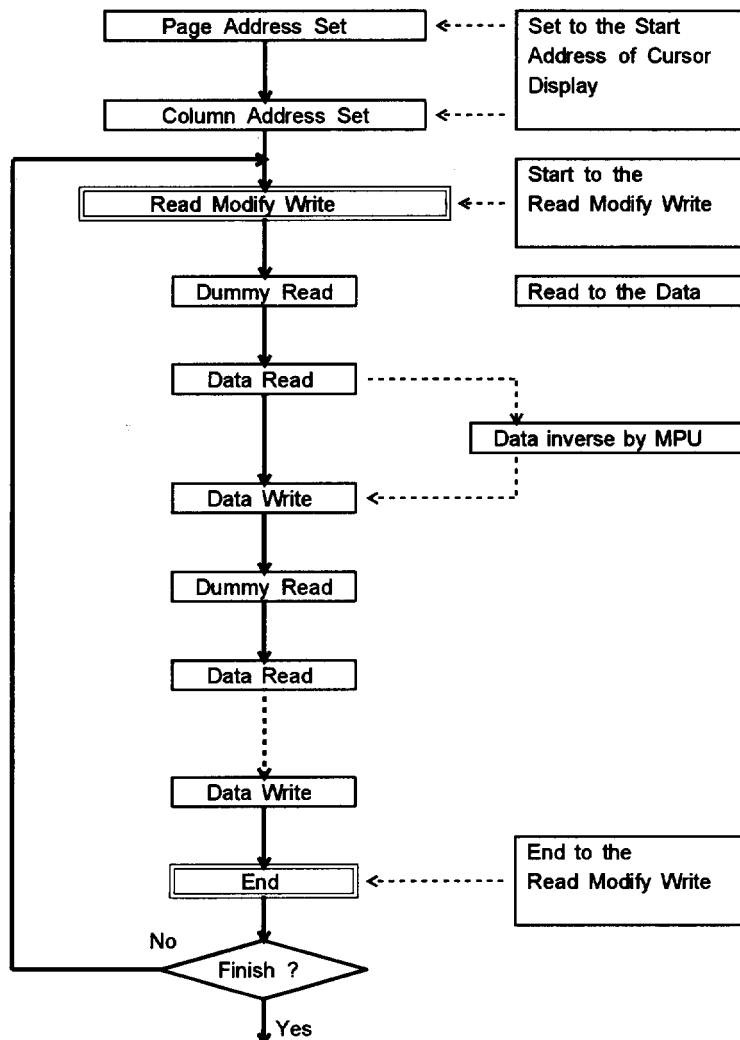
(k) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the Read Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction is executed, but the address is no change when the Display Data Read Instruction is executed. This status is continued during End instruction execution. When the End instruction is entered the column address back to the address where the Read Modify Write instruction entering. By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

A0		RD		WR		D ₇					D ₀	
0	1	0	0	1	1	1	0	0	0	0	0	0

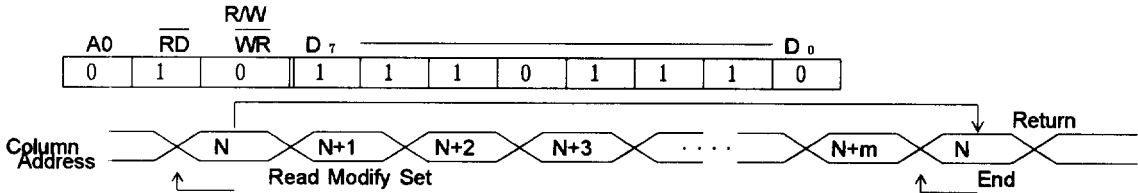
Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

(l) Sequence of cursor display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.



(n) Reset

This instruction executes the following initialization.

Initialization

- ① Set the Address (00)_H to the Column Address Counter.
- ② Set the page "0" to the Page Address Register.
- ③ Select the D₃ of the Output Assignment register to "0"
- ④ Set the EVR register to (00)_H
- ⑤ Set the 8x8bit Mode to the Scroll, Set the speed 4 to the Scroll speed.
- ⑥ Release the All page to the Scroll page.

In this time, there are no influence to the Display Data RAM.

A0	\overline{RD}	\overline{WR}	D ₇								D ₀
0	1	0	1	1	1	0	0	0	1	0	

The reset signal input to the \overline{RES} terminal must be required for the initialization when the power turns on. Substitution of Reset Instruction for the reset signal input to the \overline{RES} terminal is not allowed.

(o) COM Output / Scroll Set Up

This instruction set the Common Driver scanning order and Scroll states.

A0	\overline{RD}	\overline{WR}	D ₇ _____ D ₀							
0	1	0	1	1	0	0	A ₃	M	S1	S0

A₃ : Set the Common Driver scanning order. (Refer to 1-6)

M : Set the Scroll Dot of 1-Characters

0 : 8x8 Dot Mode

1 : 16x16 Dot Mode

S0,S1 : Set the Scroll Speed in 4-step

	Scroll Speed	S1	S0	
fast ↑↓ slow	4	0	0 32.6 dot/sec
	3	0	1 16.3 dot/sec
	2	1	0 8.1 dot/sec
	1	1	1 4.1 dot/sec

<CL1=400kHz,1/32Duty>

(p) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is required.

A0	\overline{RD}	\overline{WR}	D ₇								D ₀
0	1	0	0	0	1	0	0	1	0	D	

D 0: Internal Power Supply Off

1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q) LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 ~ V4 and output LCD driving waveform through the COM/SEG terminals.

A0	RD	R/W	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1	1

NJU6583 contains operational amplifiers for LCD bias voltage V1 ~ V4. These amplifiers current are reduced in order to realize low power consumption. Because of this reduction, LCD driving voltage V1 ~ V4 might be unstable just after the internal power supply is turned on.

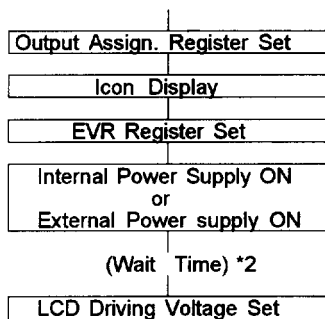
LCD Driving Voltage Set instruction is prepared for this unstableness.

● LCD driving power supply ON/OFF sequences

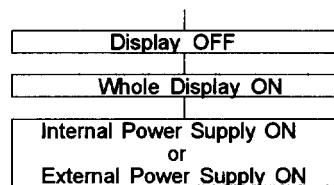
The following sequences are required when the power supply is tuned on/of.

When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence mentioned in (s) is required.

Turn ON sequence



Turn OFF sequence

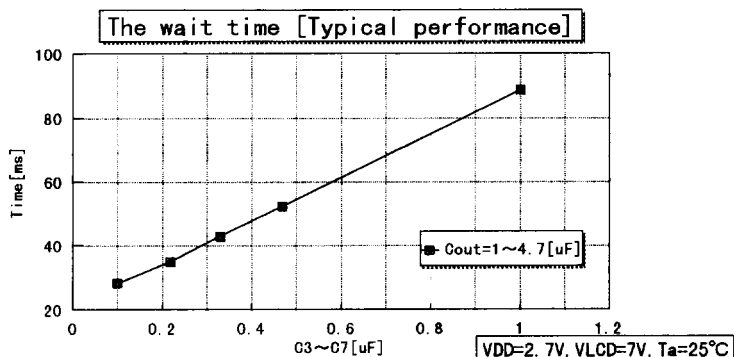


*1 This instruction is required in both cases of the internal and external power supply.

Until "LCD driving voltage Set" execution, NJU6583 operating current is higher than usual state and all COM/ SEG terminals output V_{DD} level continuously except LCD driving waveform.

*2 The wait time depends on the C₃ ~ C₇, C_{OUT} capacitors((4) (d)Fig.5), V_{DD} and V_{LCD} voltage.

Therefore a test on actual module should be practiced. Refer to the following graph.




(r) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this instruction execute, the internal Electrical Variable Resistor(EVR) to change the V_s output voltage, generate one voltage from 32 voltage state. The range of V_s output level can be adjusted by the external resistance. For more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

R/W											
A0	\overline{RD}	\overline{WR}	D ₇ _____								D ₀
0	1	0	1	0	0	A ₄	A ₃	A ₂	A ₁	A ₀	

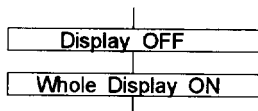
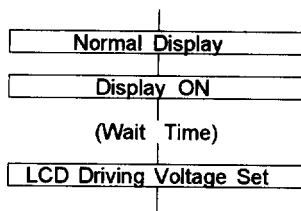
A ₄	A ₃	A ₂	A ₁	A ₀	V _{LCD}	V _{LCD} = V _{DD} - V _S When EVR does EVR register to
0	0	0	0	0	Low	
		:				
		:				
1	1	1	1	1	High	

(s) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits put on the power save mode and the operating current is reduced as same as stand by current. The internal status in the Power Save Mode is as follows;

- ① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
- ② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
- ③ Keeping the display data and operating mode as before the power save mode.
- ④ All of LCD driving bias voltage fixed to the V_{DD} level.

The power save and its release should be performed according to the following sequences.

Power Save Sequence

Power Save Release Sequence


*1 Power save mode requires dual-instruction. After the second instruction" whole Display ON", the power save mode starts.

*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.

*3 Until "LCD driving voltage set" execution, NJU6583 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.

*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.

*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

(t) Scroll Page Set

This instruction sets some Scroll Pages at the same time.

In case of 16x16 dots scroll mode, $P_3 \sim P_0$ data must be set from the following table.

R/W		D ₇ ~ D ₀										<16x16 Dot Scroll Mode>			
A0	\overline{RD}	\overline{WR}										P ₃	P ₂	P ₁	P ₀
0	1	0	0	1	*	*	P ₃	P ₂	P ₁	P ₀		0	0	1	1
0 : No Scroll												1			
1 : Scroll												1			
												1			

(u) Scroll On/Off

This instruction sets the horizontal scroll On/Off.

When this instruction execute, the scroll performs under the condition set by both of COM Output, Scroll Set Up and Scroll Page Set instruction. When stop the scroll by this instruction, the scroll is not stopped immediately but after 7 dots (8x8 dots mode) or 15 dots (16x16 dots mode) shift performs completely.

R/W		D ₇ ~ D ₀													
A0	\overline{RD}	\overline{WR}										P ₃	P ₂	P ₁	P ₀
0	1	0	1	0	1	0	1	0	0	0	D				
D 0: Scroll OFF															
1: Scroll ON															

(v) Data Request Reset

One character shift performs completely during the scroll operation, the DREQ terminal output the Data Request signal to the MPU. After rewrite the display data in the RAM, reset the DREQ terminal by this instructions required.

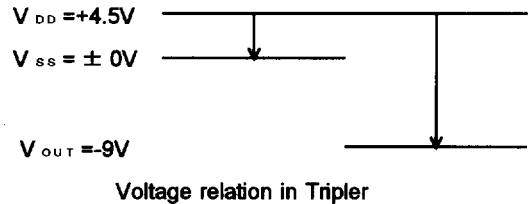
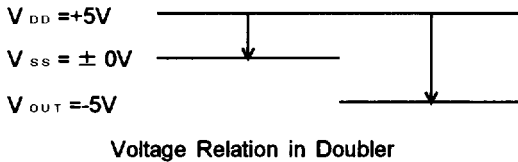
The timing of Data Request signal set is :

- In case of 16x16 dot mode : timing of COM₁₄ , COM₃₀
- In case of 8x8 dot mode : timing of COM₆ , COM₁₄ , COM₂₂ , COM₃₀

(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage (V_{DD} common) of the voltage $V_{DD} - V_{SS}$ is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT} . In case of the voltage doubler operation, connect the two capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{OUT} , then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using an oscillation circuit output as its clock signal, therefore, the oscillation circuit operation is required when step up operation. The voltage relation regarding the step up circuit is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 4.5V.



(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_S through the voltage adjust circuit. The output voltage of V_S is adjusted by changing the R_a and R_b within the range of $|V_S| < |V_{OUT}|$. The output voltage can be calculated by the following formula.

$$V_S = V_{DD} - (1 + R_b/R_a) \cdot V_{REG} \quad \text{..... ①}$$

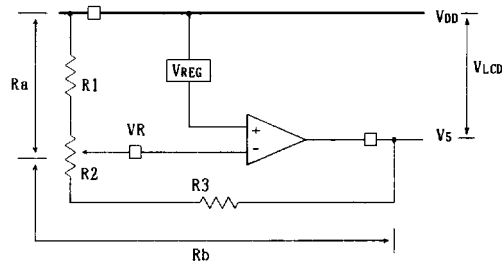


Fig. 4

Where, the V_{REG} is a constant voltage in the NJU6583 like as $V_{REG} \approx 2.5V$.

To adjust the output voltage from V_S , connect the variable resistance among VR , V_{DD} and V_S as shown in Fig. 4. When fine tuning for V_S is needed, combine with the fixed resistance of $R1$, $R3$ and variable resistance of $R2$ is recommended as shown in Fig. 4.

Design example for $R1$, $R2$ and $R3$ (reference)

- $R1 + R2 + R3 = 5M \Omega$ (Determined by the current flown between $V_{DD} - V_S$)
- Variable voltage range by the $R2$. $-2.5V \sim -4.5V$ ($V_{DD} - V_S \rightarrow 7V \sim 9V$)
(Determined by the LCD electrical characteristics)

$R1$, $R2$ and $R3$ are calculated by above conditions and the formula of ① to mentioned below;

$$\begin{aligned} R1 &= 1.388M \Omega \\ R2 &= 0.388M \Omega \\ R3 &= 3.214M \Omega \end{aligned}$$

The voltage adjust circuit has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuit serially.

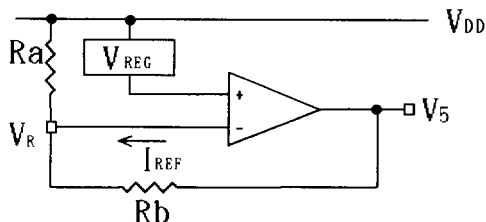
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_5 which controls LCD display contrast can adjust by the instruction. The EVR function is executed to set the 5 bits data into the EVR resistor and determine the one output voltage status out of 32 prefixed voltage status.

When execute the EVR function, set the T_1 and T_2 except the "H, H" and execute the Internal Power Supply On instruction.

[External parts constants setting example when EVR function using / reference]


(1) Determine the V_5 voltage range controlled by EVR.

LCD Driving Voltage $V_{DD} - V_5$ 7V ~ 9V

The range of V_5 2V

(2) Determine the Rb.

$R_b = [\text{The range of } V_5] / I_{REF}$

(32 status $I_{REF} \approx 5 \mu A$ constant current)

$R_b = 2V / 5 \mu A = 400k \Omega$

* $T_a = 25^\circ C$ $V_{DD} - V_{OUT} = 9V$

(3) Adjust the Ra

$$R_a = \frac{V_{REG}}{([LCD \text{ Driving Voltage}] - V_{REG}) / R_b}$$

$$R_a = \frac{2.5 V}{(7V - 2.5V) / 400k \Omega} = 222k \Omega$$

(4) Adjust the Ra

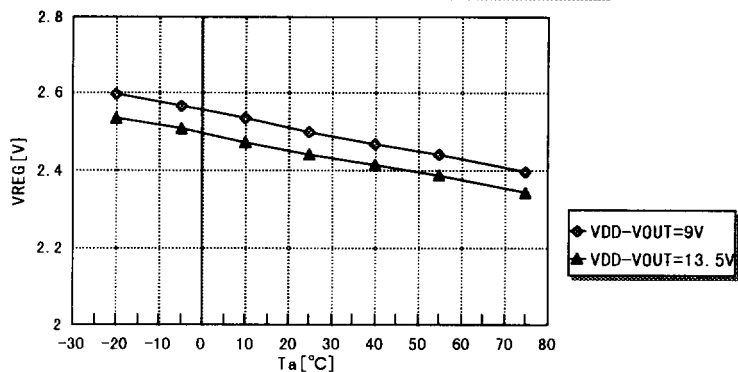
Adjust the Ra to good contrast of LCD display after the (D_4, D_3, D_2, D_1, D_0) of EVR register set to (1, 0, 0, 0, 0) or (0, 1, 1, 1, 1). When the EVR using, Ra use a variable resistance and contrast adjustment mentioned in (4) for each chip is required due to the I_{REF} is simple constant current source.

When the EVR function does not use, the (D_4, D_3, D_2, D_1, D_0) of EVR register set to (0, 0, 0, 0, 0) by the RES signal or the EVR Register Set instruction.

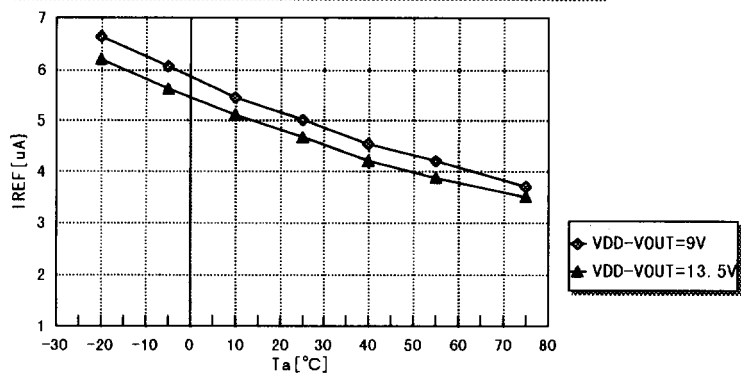


*) V_{REG} , I_{REF} depends on the voltage between V_{DD} and V_{OUT} , the operating temperature. Please refer to the following graphs.

VREG vs. Temperature (Typical performance)



IREF vs. Temperature (Typical performance)



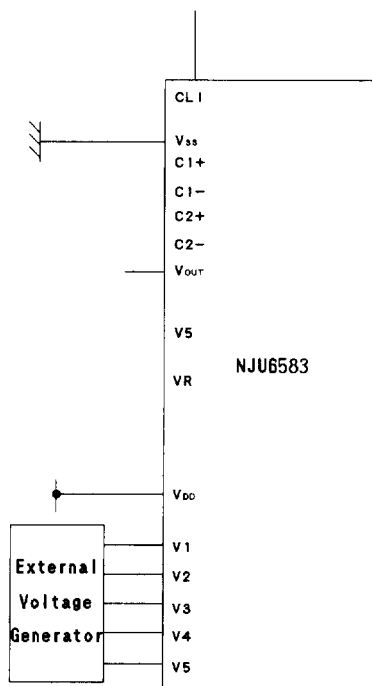
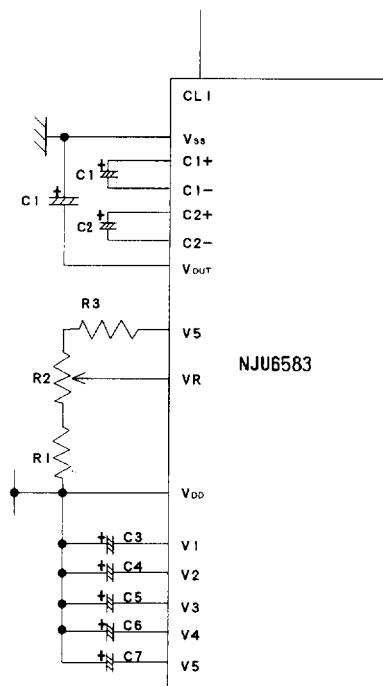
(d) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V_5 voltage by the bleeder resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 5 capacitor are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitor C3, C4, C5, C6, and C7 determine by combine with the actual LCD panel.

Using the internal Power Supply

Using the external Power Supply



Reference set up value
VLCD = VDD - V5 ≈ 7 ~ 9V

Item	Value
C1~C2	4.7~10μF
C3~C7	0.1~0.47μF
R1	1.388MΩ
R2	0.388MΩ
R3	3.214MΩ

Fig. 5

- *1 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.
- *2 Following connection of V_{OUT} is required when external power supply using.
 When $V_{SS} > V_5$ - $V_{OUT} = V_5$
 When $V_{SS} \leq V_5$ - $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6583 can interface by using both of 8 bit bilateral data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined the P/S terminal connected to "H" or "L" level as shown in Table 4. In case of the serial interface, status and RAM data read out is impossible.

Table 4

P/S	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	\overline{CS}	A0	\overline{RD}	\overline{WR}	C86	-	-	$D_0 \sim D_7$
L	Serial	\overline{CS}	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6583 can interface both of 68 or 80 type MPU directly by setting the parallel interface (P/S="H") and "H" or "L" of the C86 terminal as shown in Table 5.

Table 5

C86	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	$D_0 \sim D_7$
H	68 type MPU	\overline{CS}	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	\overline{CS}	A0	\overline{RD}	\overline{WR}	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6583 discriminate the signal on the data bus by the combination of A0, E, R/W, and (\overline{RD} , \overline{WR}) signals as shown in Table 6.

Table 6

Common	68 type	80 type		Function
A0	R/W	\overline{RD}	\overline{WR}	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to \overline{CS} ="L", and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal is MSB first like as the order of D_7, D_6, \dots, D_0 , and the data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. When RES terminal becomes "L" or CS terminal becomes "H" in spite of the data less than 8 bits, NJU6583 recognizes wrong data as a instruction data. Therefore 8bits data is required for the input data. The time chart for the serial interface is shown in Fig. 6.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface

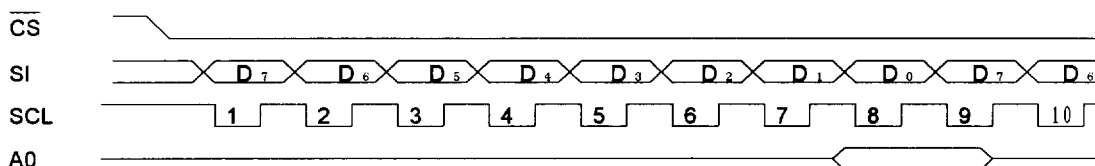


Fig. 6

(5-5) Access to the Display Data RAM and Internal Register.

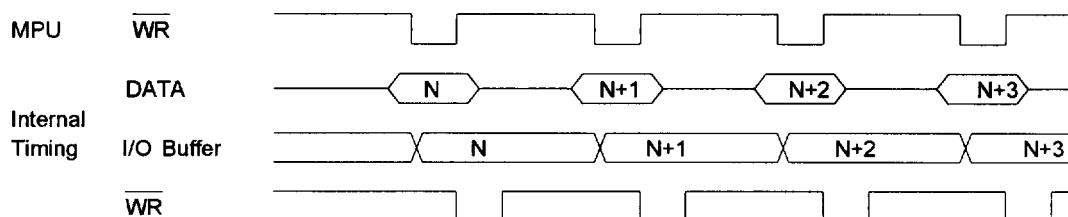
The NJU6583 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU read out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at next data read cycle. And when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6583 is available because of the limitation of access time of NJU6583 locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP operation cycle which equivalent to the waiting operation is useful.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 7.

● Write Operation



● Read Operation

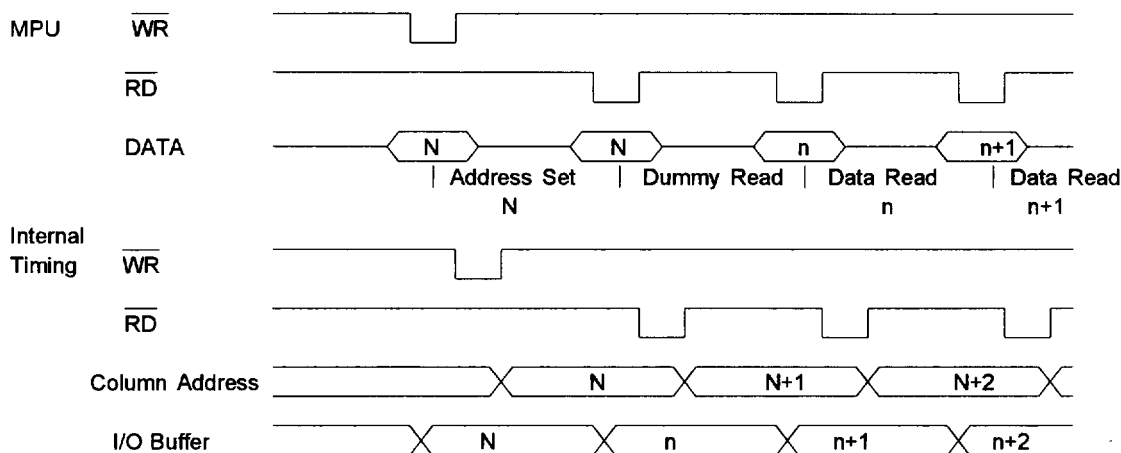


Fig. 7

(5-6) Chip Select

CS is Chip Select terminals. The Chip Select is executed by the setting of \overline{CS} ="L". Only the select mode, the interface with MPU is available. In the non select period, the D_0 to D_7 are high impedance and A_0 , \overline{RD} , \overline{WR} , \overline{SI} and \overline{SCL} input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of \overline{CS} .

ABSOLUTE MAXIMUM RATINGS

(Ta=25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V _{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 4.5 (used Tripler)	V
Supply Voltage (2)	V _S	V _{DD} -13.5 ~ V _{DD} +0.3	V
Supply Voltage (3)	V ₁ ~V ₄	V _S ~ V _{DD} +0.3	V
Input Voltage	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Operating Temperature	T _{opr}	- 30 ~ + 80	°C
Storage Temperature	T _{stg}	- 55 ~ + 125 (Chip) - 55 ~ + 100 (TCP)	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V_S ; V_{DD} > V_{SS} ≥ V_{OUT} must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the Voltage converter.

ELECTRICAL CHARACTERISTICS (1)

(V_{DD}=5V ± 10%, V_{SS}=0V, Ta=-20 ~ +75 °C)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Operating Voltage(1)	Recommend	V _{DD}		4.5	5.0	5.5	V	5
	Available			2.4		5.5		
Operating Voltage(2)	Recommend	V _S		V _{DD} -13.5		V _{DD} -3.5	V	
	Available			V _{DD} -13.5				
	Available	V ₁ , V ₂	V _{LCD} =V _{DD} -V _S	V _{DD} -0.6xV _{LCD}		V _{DD}		
	Available	V ₃ , V ₄		V _S		V _{DD} -0.4xV _{LCD}		
Input Voltage	1	V _{IHC1}	A0, D ₀ ~D ₇ , RD, WR, CS, V _{DD} =2.7V	0.7xV _{DD}		V _{DD}	V	
		V _{IHC2}		0.8xV _{DD}		V _{DD}		
	2	V _{ILC1}	RES, C86, SI, SCL, P/S Terminals V _{DD} =2.7V	V _{SS}		0.3xV _{DD}		
		V _{ILC2}		V _{SS}		0.2xV _{DD}		
Output Voltage	1	V _{OHC11}	D ₀ ~D ₇ , DREQ Terminals I _{OH} =-1mA	0.8xV _{DD}		V _{DD}	V	
		V _{OHC12}		I _{OH} =-0.5mA V _{DD} =2.7V	0.8xV _{DD}	V _{DD}		
	2	V _{OLC11}	D ₀ ~D ₇ , DREQ Terminals I _{OL} =1mA	V _{SS}		0.2xV _{DD}		
		V _{OLC12}		I _{OL} =0.5mA V _{DD} =2.7V	V _{SS}	0.2xV _{DD}		

5


■ ELECTRICAL CHARACTERISTICS (2)

P A R A M E T E R		S Y M B O L	C O N D I T I O N S		M I N	T Y P	M A X	U N I T	Note	
Input Leakage Current		I _{L1}	All Input Terminals		-1.0		1.0	μA	6	
		I _{L0}	D ₀ ~D ₇ Terminals		-3.0		3.0			
Driver On-resistance		R _{ON1}	Ta=25°C	V _{DD} =2.7V		2.0	3.0	kΩ	7	
		R _{ON2}	V _{LCD} = 8.0V			3.0	4.5			
Stand-by Current		I _{DDQ}	During Power save Mode			0.05	5.0	μA	8	
Operating Current		I _{DD12}	Display V _{LCD} = 8.0V	V _{DD} =2.7V		30	(TBD)	μA		
		I _{DD14}				22	(TBD)			
		I _{DD21}	Accessing fcyc=200kHz	V _{DD} =2.7V		217	(TBD)			9
		I _{DD22}				77	(TBD)			
Input Terminal Capacitance		C _{IN}	Ta=25°C A0, D ₀ ~D ₇ , \overline{RD} , \overline{WR} , CS, RES, C86, S1, SCL, P/S, T1, T2 Terminals			10		pF		
Operation Clock		f _{CL1}	V _{DD} =5.0V		(TBD)	400	(TBD)	kHz		
Voltage Tripler	Input Voltage	V _{DD1}	V _{DD} -V _{SS}		2.4		5.5	V	10	
		V _{DD2}	V _{DD} -V _{SS} , used Tripler		2.4		4.5			
	Output Volt.	V _{OUT}	V _{SS} -V _{LCD} , used Tripler		-9.0			V		
	On -resistance	R _{TRI}	V _{DD} =3V; C=4.7μF used Tripler			640	(TBD)	Ω		
	Adjustment range of LCD Driving Volt	V _{OUT}	Tripler Circuit "OFF"		V _{DD} -13.5		V _{DD} -5.0	V	11	
	Voltage Follower	V ₅	Voltage Adjustment Circuit "OFF"		V _{DD} -13.5		V _{DD} -5.0	V		
	Operating Current	I _{OUT1}	V _{DD} =4.5V, V _{LCD} =8V			45	(TBD)	μA	12	
		I _{OUT2}	COM/SEG Term. Open, No Access			16	(TBD)			
		I _{OUT3}	Display check. pattern			14	(TBD)			
	Voltage Reg.		V _{REG}	Ta=25°C, V _{DD} -V _{OUT} =9V		(TBD)	2.5	(TBD)	V	13
Reference Current		I _{REF}	Ta=25°C, V _{DD} -V _{OUT} =9V		(TBD)	5.0	(TBD)	μA		

Note 5) NJU6583 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D_0 to D_7 terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set".

Note 8) Apply to no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X} .

Note 10) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V_s can be adjusted within the voltage follower operating range.

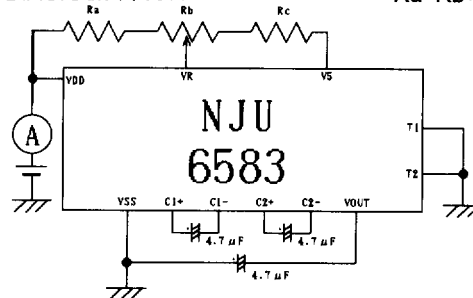
Note 12) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T1	T2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use (V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use (V_{OUT} , V_s)

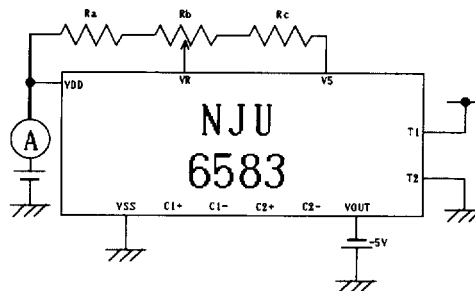
* = Don't Care

Note 13) Apply to the precision of Voltage on each EVR steps.

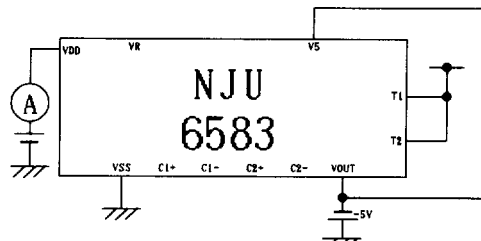
MEASUREMENT BLOCK DIAGRAM : I_{OUT1} $R_a + R_b + R_c = 2M \Omega$



: I_{OUT2} $R_a + R_b + R_c = 2M \Omega$



: I_{OUT3}





ELECTRICAL CHARACTERISTICS (3)

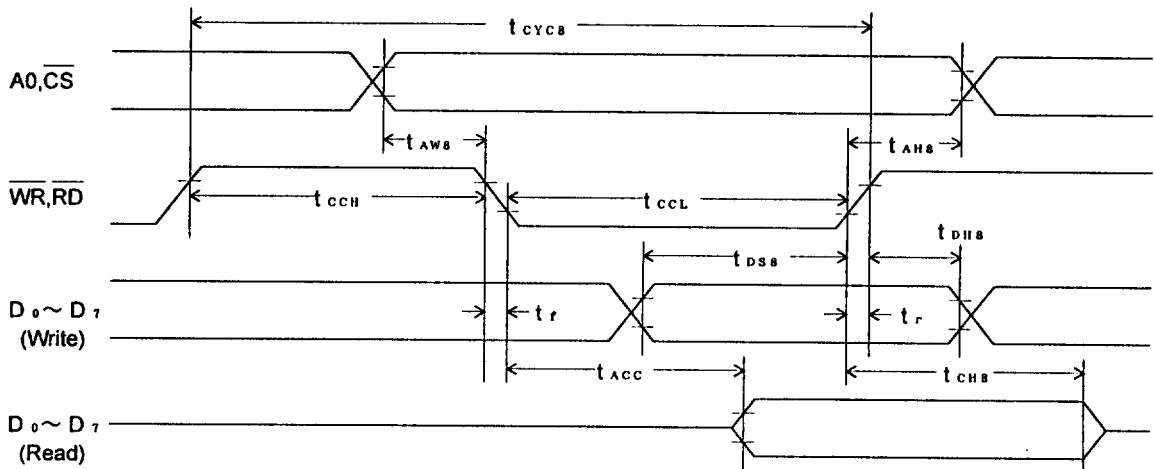
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	\overline{RES} Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}		10			us	15

Note 14) Specified from the rising edge of \overline{RES} to finish the internal circuit reset.

Note 15) Specified minimum pulse width of RES signal. Over than t_{RW} "L" input should be required for correct reset operation.

BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)


 $(V_{DD}=5.0V \pm 10\%, T_a=-20 \sim 75^\circ C)$

P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS	t_{AHs}	10		CL=100pF	ns
Address Set Up Time	Terminals	t_{AWs}	10			
System Cycle Time		t_{CVCS}	200			
Control Pulse Width	WR, "L"	$t_{CCL}(W)$	25			
	RD, "L"	$t_{CCL}(R)$	80			
	"H"	t_{CCH}	90			
Data Set Up Time	Do~D7 Terminals	t_{DSe}	60			
Data Hold Time		t_{DHs}	10			
RD Access Time		t_{ACCs}		70		
Output Disable Time		t_{OHs}	0	30		
Rise Time, Fall Time	CS, WR, RD, A0, Do~D7 Terminals	t_r, t_f		15		

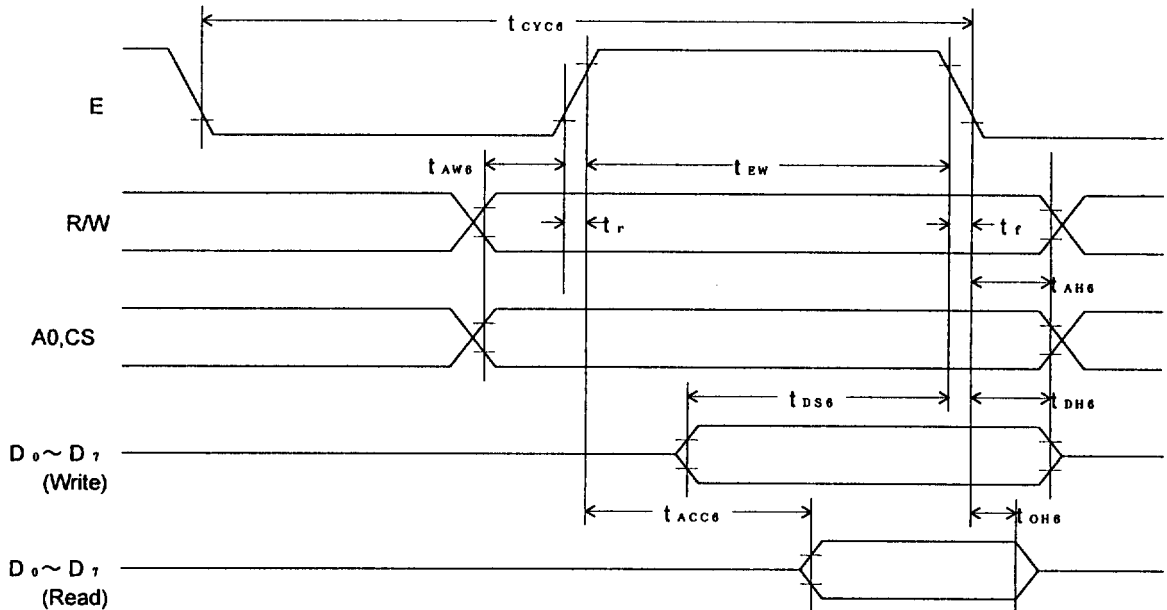
 $(V_{DD}=2.7V \sim 4.5V, T_a=-20 \sim 75^\circ C)$

P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS	t_{AHs}	25		CL=100pF	ns
Address Set Up Time	Terminals	t_{AWs}	25			
System Cycle Time		t_{CVCS}	450			
Control Pulse Width	WR, "L"	$t_{CCL}(W)$	50			
	RD, "L"	$t_{CCL}(R)$	200			
	"H"	t_{CCH}	220			
Data Set Up Time	Do~D7 Terminals	t_{DSe}	120			
Data Hold Time		t_{DHs}	35			
RD Access Time		t_{ACCs}		140		
Output Disable Time		t_{OHs}	0	35		
Rise Time, Fall Time	CS, WR, RD, A0, Do~D7 Terminals	t_r, t_f		15		

Note 15) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 16) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

• Read/Write operation sequence (68 Type MPU)


(V_{DD}=5.0V±10%, T_a=-20~75°C)

P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS, R/W Terminals	t _{AHs}	10		CL=100pF	ns
Address Set Up Time		t _{AWs}	10			
System Cycle Time		t _{cycs}	200			
Enable	E Terminal	t _{ew}	100			
Pulse Width			25			
Data Set Up Time	D ₀ ~D ₇ Terminals	t _{DSh}	60			
Data Hold Time		t _{DHs}	20			
Access Time		t _{accs}		70		
Output Disable Time		t _{ohs}	0	25		
Rise Time, Fall Time	A0, CS, R/W, E, D ₀ ~D ₇ Terminals	t _r , t _f		15		

(V_{DD}=2.7V~4.5V, T_a=-20~75°C)

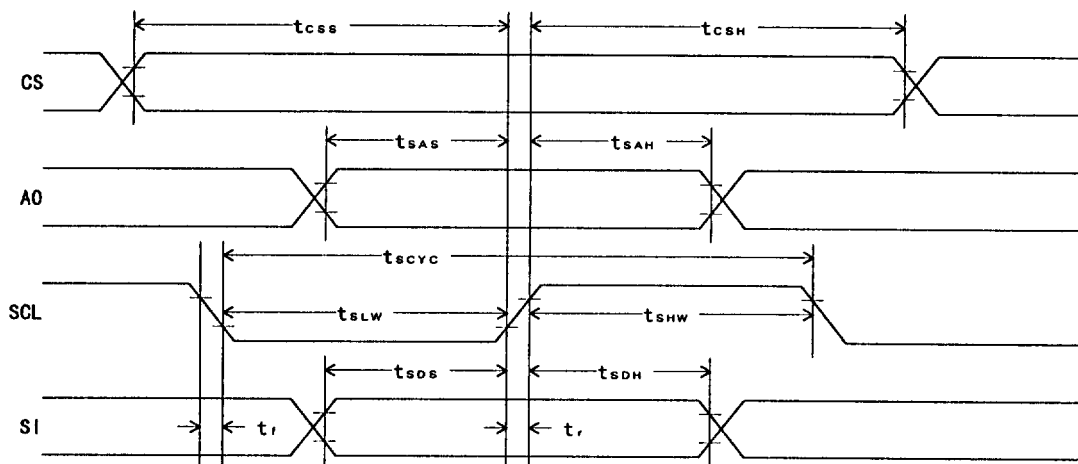
P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS, R/W Terminals	t _{AHs}	25		CL=100pF	ns
Address Set Up Time		t _{AWs}	25			
System Cycle Time		t _{cycs}	450			
Enable	E Terminal	t _{ew}	200			
Pulse Width			50			
Data Set Up Time	D ₀ ~D ₇ Terminals	t _{DSh}	120			
Data Hold Time		t _{DHs}	40			
Access Time		t _{accs}		140		
Output Disable Time		t _{ohs}	0	45		
Rise Time, Fall Time	A0, CS, R/W, E, D ₀ ~D ₇ Terminals	t _r , t _f		15		

Note 17) t_{cycs} indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.

Note 18) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 19) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

• Read/Write operation sequence (Serial Interface)



($V_{DD}=5.0V \pm 10\%$, $T_a=-20 \sim 75^\circ C$)

P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tscyc	500			ns
SCL "H" pulse width		tSHW	150			
SCL "L" pulse width		tSLW	150			
Address Set Up Time	A0 Terminal	tsas	120			
Address Hold Time		tsAH	200			
Data Set Up Time	SI Terminal	tsds	120			
Data hold Time		tsdH	50			
CS-SCL Time	CS Terminals	tcss	30			
		tcsH	400			
Rise Time, Fall Time	SCL, A0, CS SI, Terminals	tr, tf		15		

($V_{DD}=2.7V \sim 4.5V$, $T_a=-20 \sim 75^\circ C$)

P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tscyc	1000			ns
SCL "H" pulse width		tSHW	300			
SCL "L" pulse width		tSLW	300			
Address Set Up Time	A0 Terminal	tsas	250			
Address Hold Time		tsAH	400			
Data Set Up Time	SI Terminal	tsds	250			
Data hold Time		tsdH	100			
CS-SCL Time	CS Terminals	tcss	60			
		tcsH	800			
Rise Time, Fall Time	SCL, A0, CS SI, Terminals	tr, tf		15		

Note 20) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.

Note 21) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

■ LCD DRIVING WAVEFORM

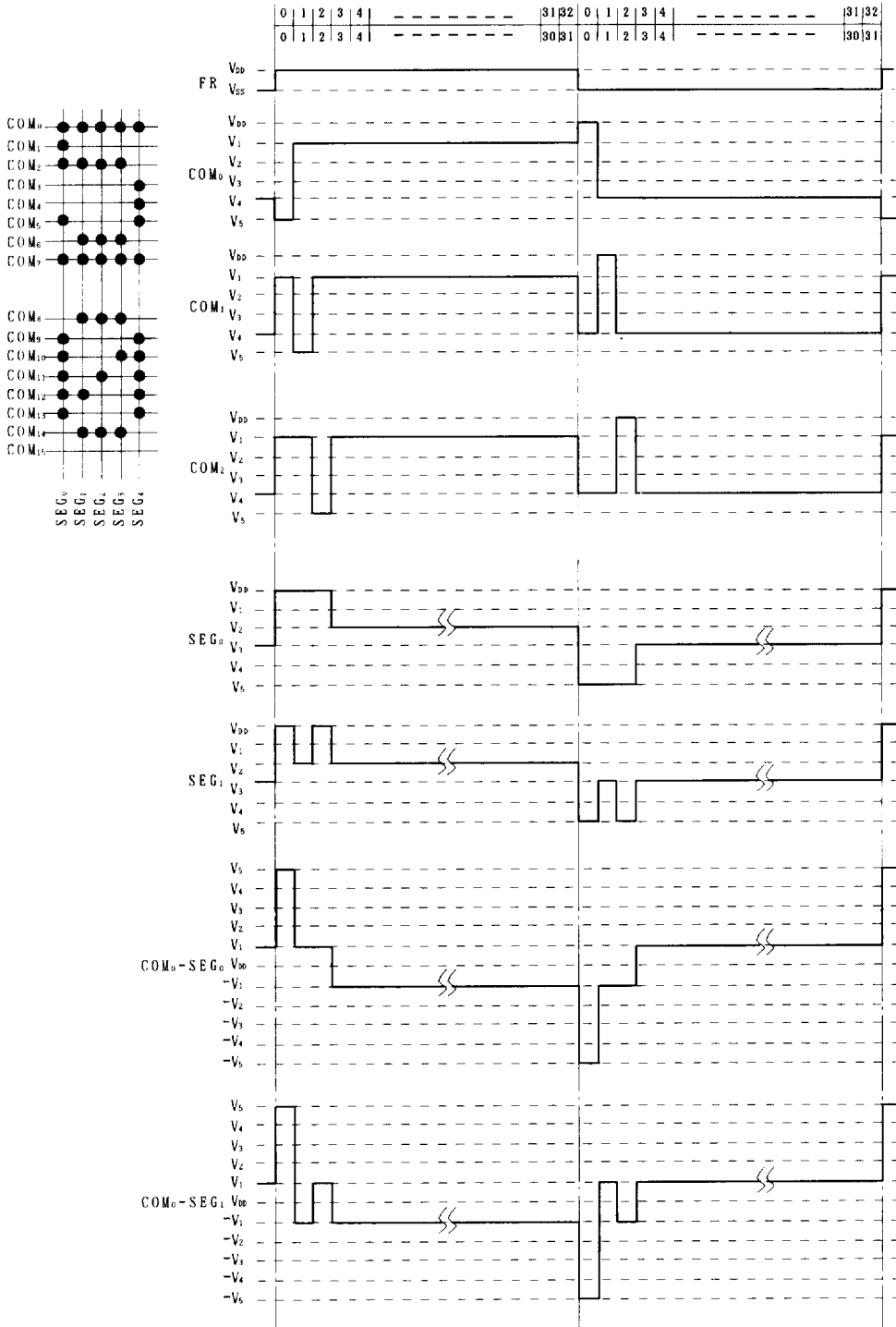


Fig. 8



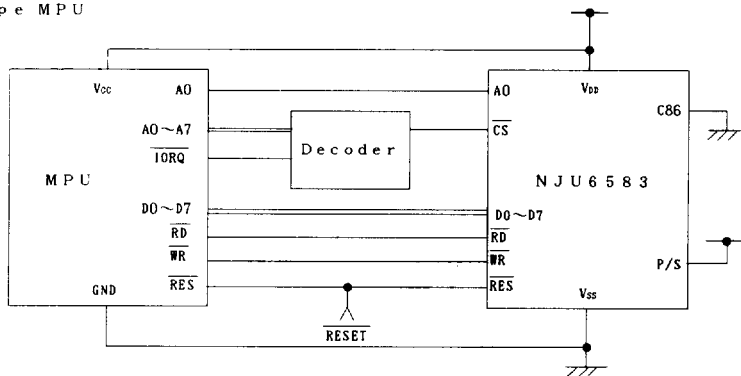
■ APPLICATION CIRCUIT

(1) Microprocessor Interface Examples

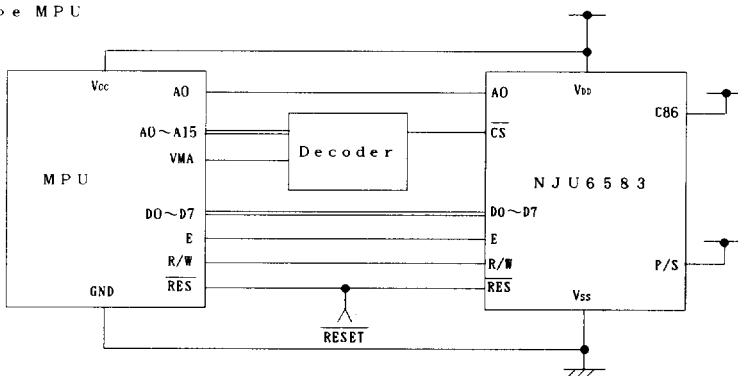
The NJU6583 can interface with both of 80 type and 68 type MPU by the serial format directly. Therefore minimum wiring for the MPU interface is available.

※ : C86 terminal must be fixed V_{DD} or V_{SS} .

● 80 Type MPU



● 68 Type MPU



● Serial Interface

