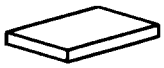
PRELIMINARY

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6580 is a bit map LCD driver to display graphics or characters.
It contains 1,904 bits display data RAM, microprocessor inter face circuits, instruction decoder, 96-segment and 17-common(1 out of 17-driver is prepared for Icon display)drivers.
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel mode.
The NJU6580 automatically performs 7 or 15 dots horizontal smooth scroll, therefore the horizontal character scroll is easily controlled by the MPU.
17 x 96 dot graphics or 6-character 1-line by 16 x 16 dot character with icon are displayed by NJU6580 itself.
The wide operating voltage like as 2.4V to 5.5V and low operating current are useful to apply small sized battery operated items.

■ PACKAGE OUTLINE

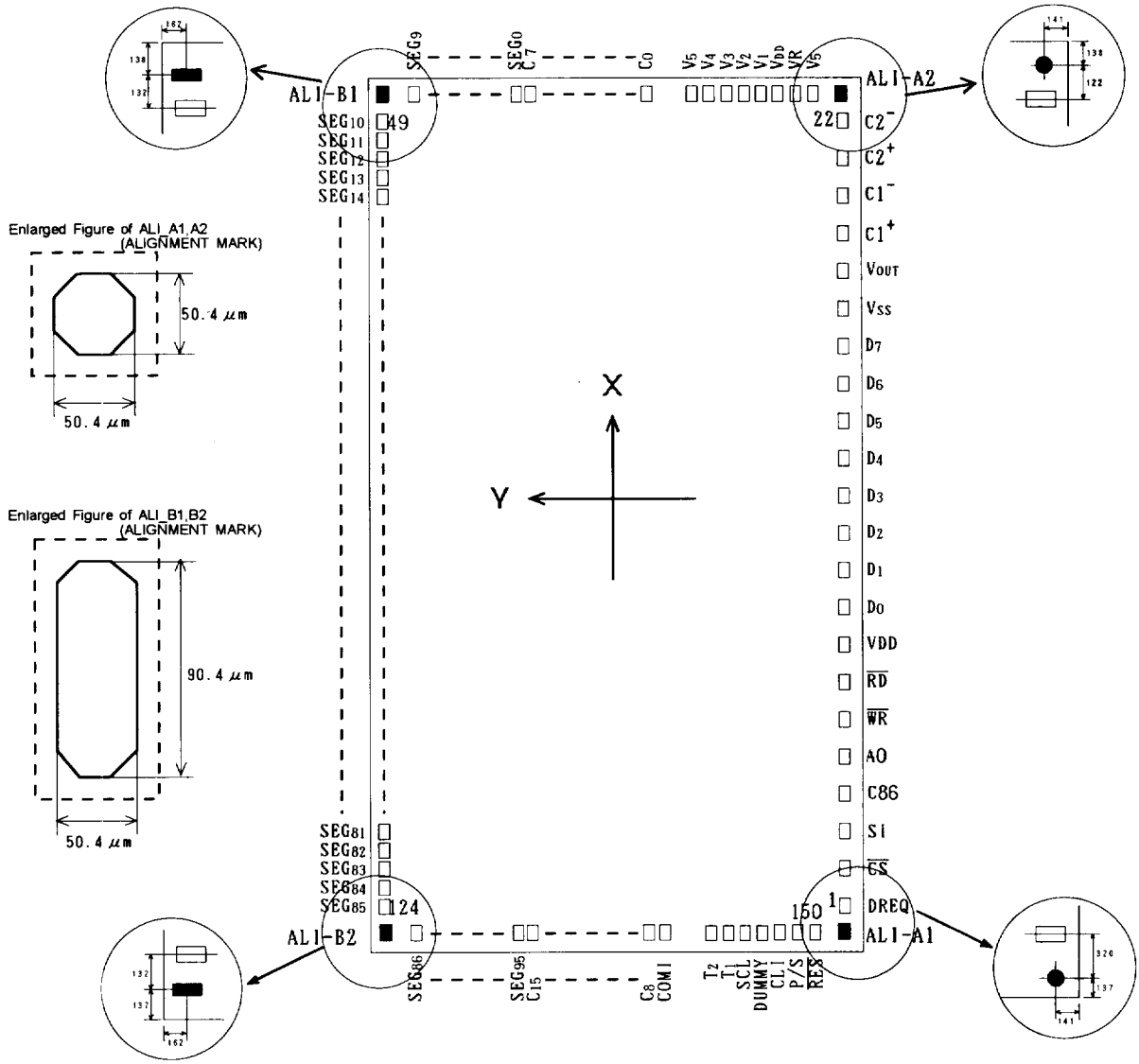


NJU6580C

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 1,904 bits
- LCD Drivers - 16-common + 1 Icon common x 96-segment
- Direct Interface with both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/16 or 1/17 Duty
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver Order Assignment, Power Saving, and Scroll ON/OFF.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage — 2.4V ~ 5.5V
- LCD Driving Voltage — 6.0V ~ 13.5V
- Package Outline — Chip / Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip Center	X=0um, Y=0um
Chip Size	X=6.54mm, Y=3.54mm
Chip Thickness	400um ± 30um
Bump Size	50um x 110um
Bump Height	25um TYP.
Bump Material	Au

■ : Four PADs illustrated with this mark are the alignment marks for COG.

■ PAD COORDINATES

Chip Size 6.54mm x 3.54mm(Chip Center X=0um,Y=0um)

PAD No.	Terminal	X=(μ m)	Y=(μ m)
1	DERQ	-2813	-1603
2	$\overline{CS}$	-2582	-1603
3	SI	-2435	-1603
4	C86	-2288	-1603
5	A0	-2141	-1603
6	$\overline{WR}$	-1993	-1603
7	$\overline{RD}$	-1846	-1603
8	V_{DD}	-1721	-1603
9	D_0	-1401	-1603
10	D_1	-901	-1603
11	D_2	-401	-1603
12	D_3	99	-1603
13	D_4	599	-1603
14	D_5	1099	-1603
15	D_6	1599	-1603
16	D_7	2099	-1603
17	V_{SS}	2450	-1603
18	V_{OUT}	2562	-1603
19	$C1^+$	2674	-1603
20	$C1^-$	2786	-1603
21	$C2^+$	2898	-1603
22	$C2^-$	3010	-1603
23	V_5	3106	-1415
24	VR	3106	-1303
25	V_{DD}	3106	-1191
26	V_1	3106	-1079
27	V_2	3106	-967
28	V_3	3106	-855
29	V_4	3106	-743
30	V_5	3106	-631
31	C_0	3106	-365
32	C_1	3106	-285
33	C_2	3106	-205
34	C_3	3106	-125
35	C_4	3106	-45
36	C_5	3106	35
37	C_6	3106	115
38	C_7	3106	195
39	SEG_0	3106	275
40	SEG_1	3106	355
41	SEG_2	3106	435
42	SEG_3	3106	515
43	SEG_4	3106	595
44	SEG_5	3106	675
45	SEG_6	3106	755
46	SEG_7	3106	835
47	SEG_8	3106	915
48	SEG_9	3106	995
49	SEG_{10}	3000	1602
50	SEG_{11}	2920	1602

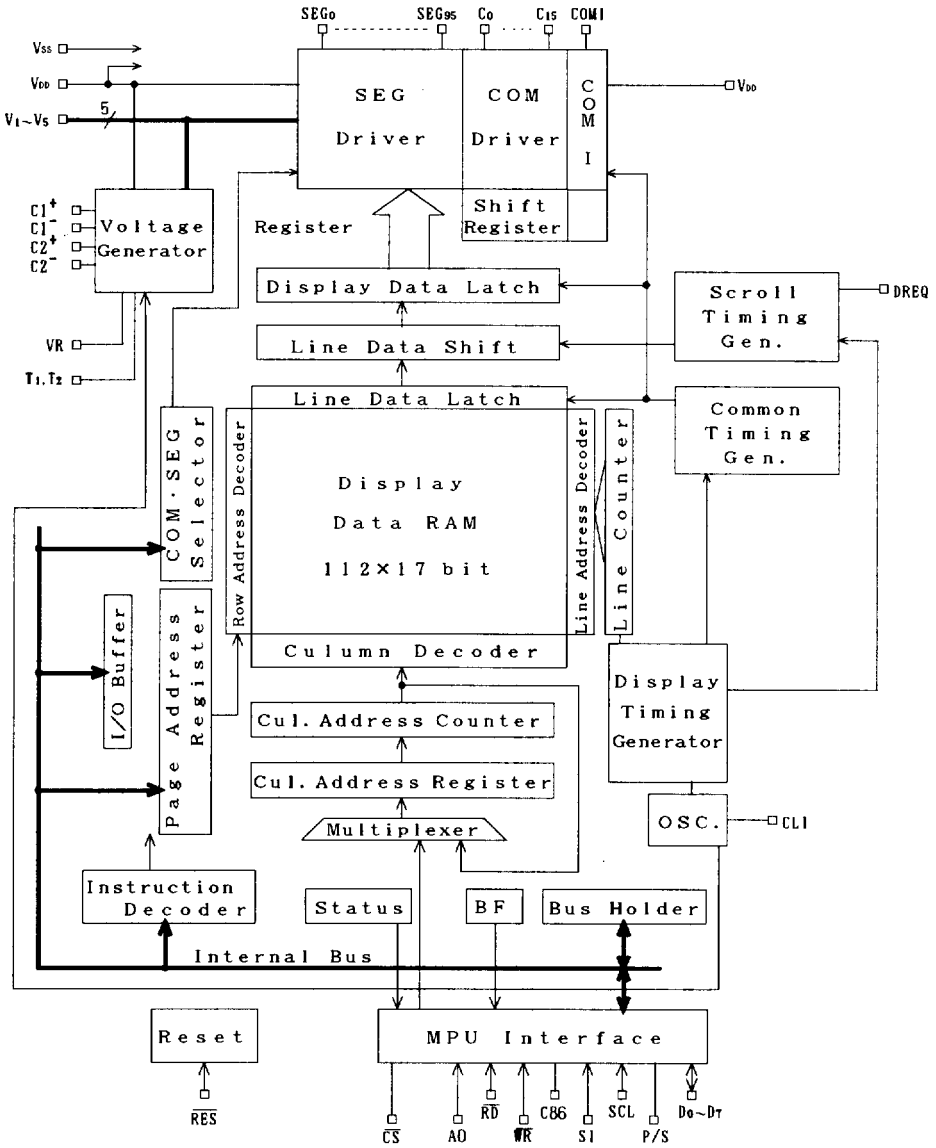
PAD No.	Terminal	X=(μ m)	Y=(μ m)
51	SEG_{12}	2840	1602
52	SEG_{13}	2760	1602
53	SEG_{14}	2680	1602
54	SEG_{15}	2600	1602
55	SEG_{16}	2520	1602
56	SEG_{17}	2440	1602
57	SEG_{18}	2360	1602
58	SEG_{19}	2280	1602
59	SEG_{20}	2200	1602
60	SEG_{21}	2120	1602
61	SEG_{22}	2040	1602
62	SEG_{23}	1960	1602
63	SEG_{24}	1880	1602
64	SEG_{25}	1800	1602
65	SEG_{26}	1720	1602
66	SEG_{27}	1640	1602
67	SEG_{28}	1560	1602
68	SEG_{29}	1480	1602
69	SEG_{30}	1400	1602
70	SEG_{31}	1320	1602
71	SEG_{32}	1240	1602
72	SEG_{33}	1160	1602
73	SEG_{34}	1080	1602
74	SEG_{35}	1000	1602
75	SEG_{36}	920	1602
76	SEG_{37}	840	1602
77	SEG_{38}	760	1602
78	SEG_{39}	680	1602
79	SEG_{40}	600	1602
80	SEG_{41}	520	1602
81	SEG_{42}	440	1602
82	SEG_{43}	360	1602
83	SEG_{44}	280	1602
84	SEG_{45}	200	1602
85	SEG_{46}	120	1602
86	SEG_{47}	40	1602
87	SEG_{48}	-41	1602
88	SEG_{49}	-121	1602
89	SEG_{50}	-201	1602
90	SEG_{51}	-281	1602
91	SEG_{52}	-361	1602
92	SEG_{53}	-441	1602
93	SEG_{54}	-521	1602
94	SEG_{55}	-601	1602
95	SEG_{56}	-681	1602
96	SEG_{57}	-761	1602
97	SEG_{58}	-841	1602
98	SEG_{59}	-921	1602
99	SEG_{60}	-1001	1602
100	SEG_{61}	-1081	1602

PAD No.	Terminal	X=(μ m)	Y=(μ m)
101	SEG_{62}	-1161	1602
102	SEG_{63}	-1241	1602
103	SEG_{64}	-1321	1602
104	SEG_{65}	-1401	1602
105	SEG_{66}	-1481	1602
106	SEG_{67}	-1561	1602
107	SEG_{68}	-1641	1602
108	SEG_{69}	-1721	1602
109	SEG_{70}	-1801	1602
110	SEG_{71}	-1881	1602
111	SEG_{72}	-1961	1602
112	SEG_{73}	-2041	1602
113	SEG_{74}	-2121	1602
114	SEG_{75}	-2201	1602
115	SEG_{76}	-2281	1602
116	SEG_{77}	-2361	1602
117	SEG_{78}	-2441	1602
118	SEG_{79}	-2521	1602
119	SEG_{80}	-2601	1602
120	SEG_{81}	-2681	1602
121	SEG_{82}	-2761	1602
122	SEG_{83}	-2841	1602
123	SEG_{84}	-2921	1602
124	SEG_{85}	-3001	1602
125	SEG_{86}	-3107	995
126	SEG_{87}	-3107	915
127	SEG_{88}	-3107	835
128	SEG_{89}	-3107	755
129	SEG_{90}	-3107	675
130	SEG_{91}	-3107	595
131	SEG_{92}	-3107	515
132	SEG_{93}	-3107	435
133	SEG_{94}	-3107	355
134	SEG_{95}	-3107	275
135	C_{15}	-3107	195
136	C_{14}	-3107	115
137	C_{13}	-3107	35
138	C_{12}	-3107	-45
139	C_{11}	-3107	-125
140	C_{10}	-3107	-205
141	C_9	-3107	-285
142	C_8	-3107	-365
143	COMI	-3107	-445
144	T_2	-3107	-603
145	T_1	-3107	-750
146	SCL	-3107	-897
147	DUMMY	-3107	-1009
148	CLI	-3107	-1121
149	P/S	-3107	-1268
150	$\overline{RES}$	-3107	-1415

5

PAD No.	Terminal	X=(μ m)	Y=(μ m)
ALIGNMENT	A1	-3133	-1629
ALIGNMENT	A2	3132	-1629
ALIGNMENT	B1	3132	1608
ALIGNMENT	B2	-3133	1608

■ BLOCK DIAGRAM



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■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function
8,25	V_{DD}	Power	V_{DD} =+5V (Less than 4.5V should be apply when voltage tripler using.)
17	V_{SS}	GND	V_{SS} = 0V
26 27 28 29 23,30	V_1 V_2 V_3 V_4 V_5	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ When internal power supply is on, internal circuits generated and supply following LCD bias voltage to $V_1 \sim V_4$ terminals. Term. / Volt.: V_1 = V_5 +4/5V_{LCD}; V_2 = V_5 +3/5V_{LCD}; V_3 = V_5 +2/5V_{LCD}; V_4 = V_5 +1/5V_{LCD} ($V_{LCD} = V_{DD} - V_5$)
19 20 21 22	$C1^+$ $C1^-$ $C2^+$ $C2^-$	O	Step up capacitor connecting terminals. In case of tripler operation, connect the capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$. In case of doubler operation, connect the capacitor between $C2^+$ and $C2^-$, connect $C2^+$ to $C1^+$, and $C1^-$ should be open.
18	V_{OUT}	O	Step up voltage output terminal. Connect the step up capacitor between this terminal and V_{SS}.
24	VR	I	Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance connect between V_{DD} and V_5 terminal.
145,144	T_1 ,T_2	I	LCD bias voltage control terminals. ※ Don't Care T_1 / T_2 / Step up cir. / Voltage Adj. / V/F Cir.: L / ※ / Available / Available / Available H / L / Not Avail. / Available / Available H / H / Not Avail. / Not Avail. / Available
9 ~ 16	$D_0 \sim D_7$	I/O	Tri-state bilateral. Data I/O terminal when 8-bit parallel operation.
5	A0	I	Connect to the Address bus of MPU. The data on the D_0 to D_7 is distinguished Display data or Instruction by this signal. A0: H = Display Data; L = Instruction
150	$\overline{RES}$	I	Reset terminal. When the $\overline{RES}$ terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of $\overline{RES}$.
2	$\overline{CS}$	I	Chip select terminal. Data input/output are available during $\overline{CS}$="L".
7	$\overline{RD}$ (E)	I	<When interface with 80 type MPU> $\overline{RD}$ signal of 80 type MPU input terminal. Active"L". During this signal "L", the data bus becomes as output terminal. <When interface with 68 type MPU> Enable clock of 68 type MPU input terminal. Active "H".

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No.	Symbol	I/O	Function
6	$\overline{WR}$ (R/$\overline{W}$)	I	<When interface with 80 type MPU> Connect the 80 type MPU $\overline{WR}$ signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal. <When interface with 68 type MPU> Read/write control signal of 68 type MPU input terminal. R/$\overline{W}$: H = Read, L = Write
4	C86	I	Select the MPU interface type. C86: H = 68 Type, L = 80 Type C86 terminal should be fixed to V_{DD} or V_{SS}.
3	SI	I	Serial data input terminal.
146	SCL	I	Serial data clock signal input terminal. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.
149	P/S	I	Serial or parallel interface select terminal. P/S: "H" — Chip Select: $\overline{CS}$ — Data/Command: A0 — Data: D_0~D_7 — Read/Write: $\overline{RD}$、$\overline{WR}$ — Serial CLK: — P/S: "L" — Chip Select: $\overline{CS}$ — Data/Command: A0 — Data: SI — Read/Write: Write only — Serial CLK: SCL *RAM data and status read operation is impossible when select the serial interface. ・ When select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L". ・ When select the serial interface (P/S="L"), $\overline{RD}$ and $\overline{WR}$ must be fix "H" or "L", and D_0 to D_7 becomes to the high impedance state.
148	CLI	I	External clock input terminal.
1	DREQ	O	Data request signal output terminal.(at the scroll ON) Active"H".
147	DUMMY		DUMMY terminal. Normally open.

5

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>31
～
38</td><td>C_0
～
C_7</td><td rowspan="4">O</td><td rowspan="4">LCD drive output terminals.
● Common output terminals : C_0 to C_{15}
● Segment output terminals : SEG_0 to SEG_{95}
・ Segment output terminal
Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM.
<table><tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal</th><th>Reverse</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr><tr><td>L</td><td>V_5</td><td>V_3</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr><tr><td>L</td><td>V_3</td><td>V_5</td></tr></table>
・ Common Output Terminal
Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data.
<table><tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr><tr><td>L</td><td>V_{DD}</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr><tr><td>L</td><td>V_4</td></tr></table></td></tr>
<tr><td>39
～
134</td><td>SEG_0
～
SEG_{95}</td></tr>
<tr><td>135
～
142</td><td>C_{15}
～
C_8</td></tr>
<tr><td></td><td></td></tr>
<tr><td>143</td><td>COMI</td><td>O</td><td>Icon common output terminal.
Icon common output when Icon Display instruction execution.
<table><tr><th></th><th>Icon Display ON</th><th>Icon Display OFF</th></tr><tr><td>State</td><td>COM_{16}</td><td>V_1 or V_4</td></tr></table></td></tr>
</table>

(Terminal 147 is NC)

5

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction except th e status read are inhibited.

The busy flag output from D_7 terminal when status read instruction is executed.

If enough cycle time over than t_{cyc} indicated in the bus timing characteristics is kept, no need to check th e busy flag and it realized high performance for the MPU.

(1-2) Line Counter

The Line Counter is reset at the FR signal changing and counts up by synchronizing common signal cycle and generate the line address which addressing the read out line of Display Data RAM.

(1-3) Column Address Counter

The column address counter is 8-bit presettable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to $(A0)_H$ when the Display Data Read/Write instruction is execute d. This counter auto-increments (+1) up to $(A0)_H$ but accessing to the display data RAM over than $(6F)_H$ i s forbidden.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Dat a RAM correspondence to the Segment Driver.

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(1-4) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the data by changing the page, the page address set instruction is required. Page address "2"(D_1 ="H" and D_0 ="L") is Icon RAM area, the data only for the D_0 is valid.

(1-5) Display Data RAM

Display Data RAM consists of 1,904 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

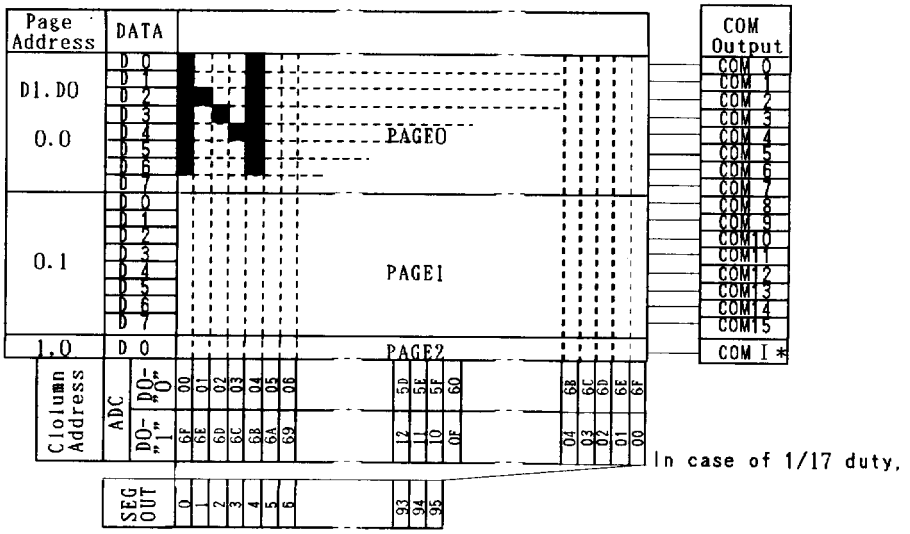
When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM output 112-bit parallel data addressed by the line counter, and these data are set in to the Display Data Latch.

This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize rew riting.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.



Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/17 Duty Set)

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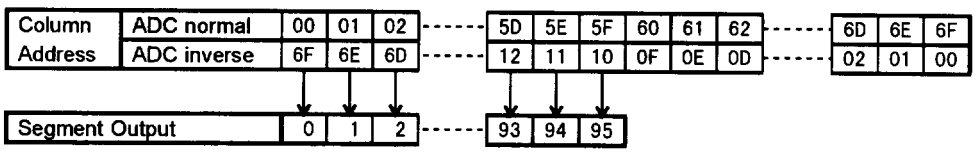
Correspondence with column address and LCD output
(When the "On" states, the relation between column address and LCD outputs are shifting)

● No Scroll(same as scroll "Off" state)



● 15 bits scroll

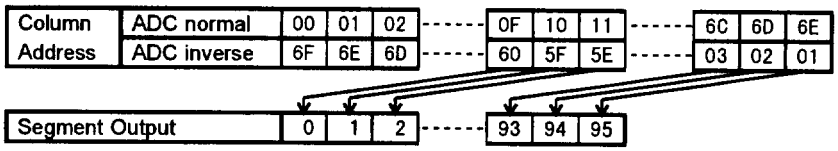


Fig. 1

(1-6) Common and Segment Driver Assignment

The scanning order can be assigned by setting A3 of the Output Assignment Register as shown Table 1. The location of Segment Drivers are fixed at any time.

Table 1

Register		Common Output Terminals			
A3	PAD No.	38	31	142	135
	Pin name	C_7	C_0	C_8	C_{15}
0	→	COM_7 ←	COM_0	COM_8 →	COM_{15}
1	→	COM_8 →	COM_{15}	COM_7 ←	COM_0

The Icon display is regardless with this function, therefore the Icon Display instruction must be exe cuted when the Icon display is needed. In this time, the Icon display driver COMI is fixed to COM_{16} timing regardless the other Common Driver assignment.

(1-7) Reset Circuits

The NJU6580 performs following initialization when the $\overline{RES}$ input is put on the "L" level.

Initialization

① Display Off
② Normal Display(Non-inverse display)
③ Icon Display Reset
④ ADC Select : Normal (ADC Instruction D_0 ="0")
⑤ Read Modify Write Mode Off
⑥ Internal Power supply(Step up) circuits Off
⑦ Clear the serial interface register
⑧ Set the address $(00)_H$ to the Column Address Counter
⑨ Set the page "0" to the Page Address Register
⑩ Select the D_3 of the Output Assignment register to "0"
⑪ Set the EVR register to $(00)_H$
⑫ Scroll Off
⑬ Set the 8x8bit Mode to the Scroll ,Set the speed 4 to the Scroll speed.
⑭ Release the All page to the Scroll page.

The $\overline{RES}$ terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface E xample". The reset signal require over than 10us $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{RES}$ signal, the normal operation is starting.

In case of the internal power supply(Step up) circuits do not use, the $\overline{RES}$ terminal must be "L" when external power supply turn on. $\overline{RES}$="L" input reset internal register and set above default, but oscillation circuits an d output terminals like as D_0 through D_7 are no influence.

No initialization by $\overline{RES}$ when power turns on, will make Hung up condition, therefore please initialize by the $\overline{RES}$ when power turns on. By the reset Instruction performs only ⑧ through ⑪ , ⑬ , ⑭ mentioned in above.

The noise into the $\overline{RES}$ terminal should be cared when of the application design to avoid the error function.

(1-8) LCD Driving

(a) LCD Driving Circuits

NJU6580 incorporate 113 LCD Drivers like as 96 Segment drivers, 16 Common drivers and 1 Icon common d river. Common drivers incorporate the shift register which scanning the common display signal.
The combination among the Display data, COM scan signal and FR signal define the LCD driving output volta ge. The output wave form is mentioned in the Fig. 8.

(b) Line Data Latch Circuits

Line Data Latch stores 112-bit of one line display data for each common cycle which read out from the Dis play Data RAM temporary and transfer this data to the LCD Driver. The Line Data Latch Circuits latches CO Mn+1 data at COMn timing to performs smooth data shifting. (Fig. 2)
The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display D ata RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits

The clock for Line Counter and latch signal for the Latch Circuits are generated from display clock. The line address is renewed by synchronizing with display clock and 112 bits display data are latched into display latc h circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer t o the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Line Data Shift Circuits

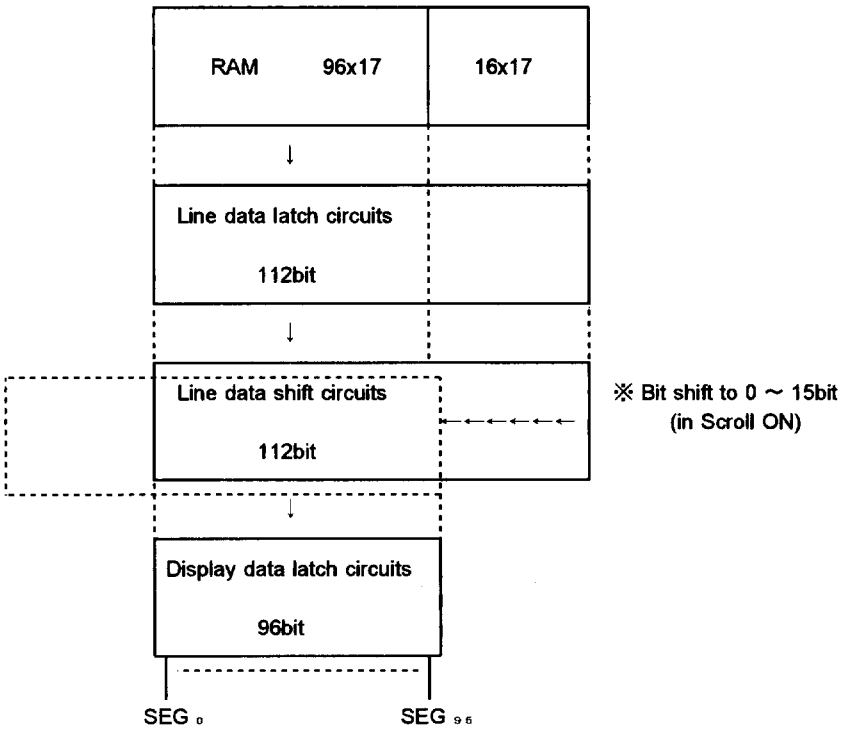
When the scroll "On" state the Line Data Shift Circuits shift maximum 15 bits toward the SEG。 which input t he line data from Line Data Latch Circuits, then output to Display Data Latch Circuits.
In case of scroll "Off" state, the data input to the Line Data Shift Circuits output to the Display Data Latch with out shift.

(e) Display Data Latch Circuits

The Display Data Latch Circuits temporally stores 96 bits display data (which) shift 0 to 15 bits by the Line Da ta Shift Circuits and output to the segment drivers.

Output RAM Data to Segment

< Data Format >



< Timing >

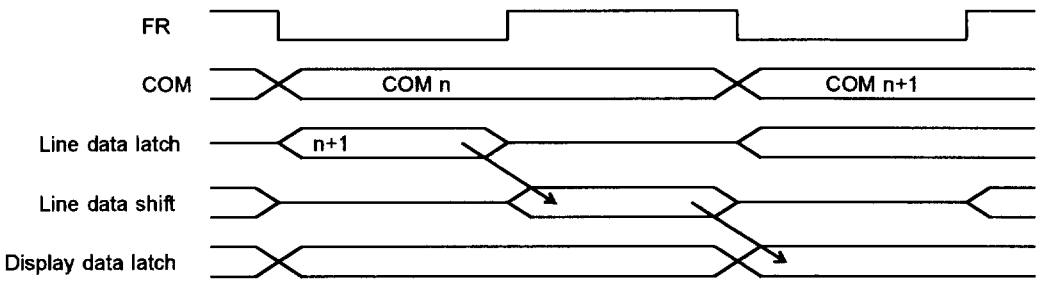


Fig. 2

(f) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock and Dr iving Signal FR. The Frame Signal FR has a function to generate the 2 frame alternative driving method wav eform for the LCD panel.

(g) Common Timing Generation

The common timing is generated by display clock.

· Waveform of Display Timing

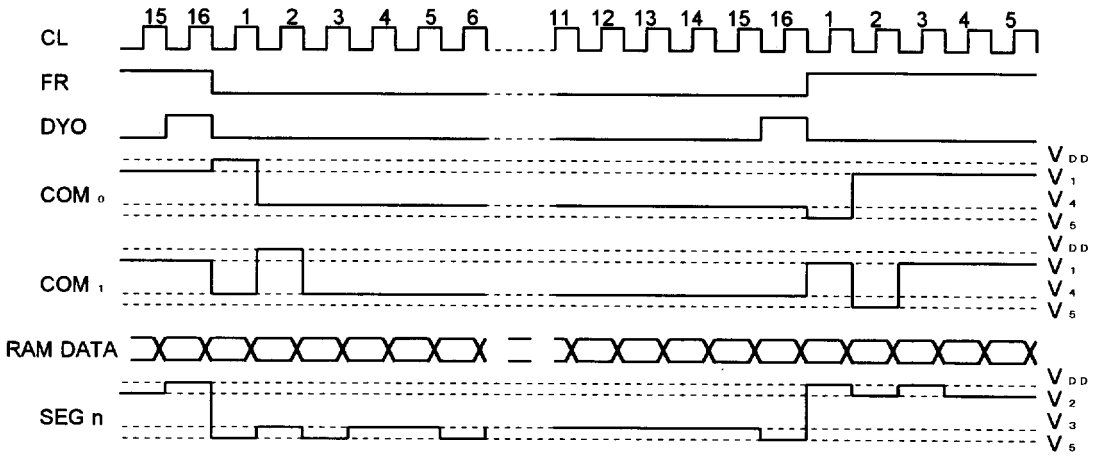


Fig. 3

(h) Fundamental Clock

The Fundamental Clock is input the CLI terminal to external. It is used as display timing signal source and th e clock for step up circuits for LCD driving. The fundamental clocks output frequency is divided by 384 which is used as display clock CL.

(i) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Tripler or Doubler) Circuits, Regulation Circuits, and Voltage Followe r. Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the large size LCD panel application. If the contrast is no good in those application, please use external power suppl y supplied more high current.

The suitable values of the capacitors connecting to the V1 to V5 terminals and the step up circuit, the feedb ack resistors for V5 operational amplifier depend on the LCD panel. And the power consumption in the LCD panel is changeable with the display patarn. Therefore a trial with actual module should be practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, vol tage follower circuits are off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD suppl y from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$,and VR are open. The status of internal power supply c an select by T_1 and T_2 terminal. The external power supply can be used together with some of internal po wer supply function.

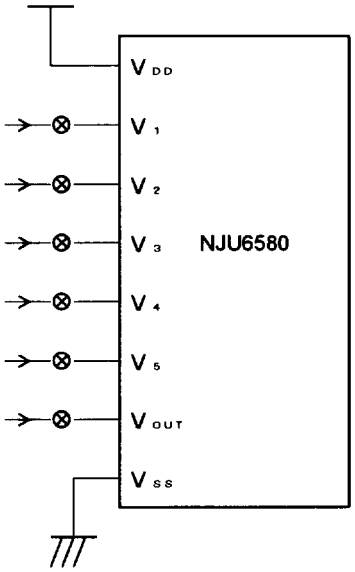
Table 3. (*:Don't Care)

T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term.
L	*	O	O	O	-		
H	L	×	O	O	V_{OUT}	OPEN	
H	H	×	×	O	V_5, V_{OUT}	OPEN	OPEN

When (T_1, T_2)=(H, L), the terminal for step up circuits of $C1^+$,$C1^-$ $C2^+$,$C2^-$ are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T_1, T_2)=(H, H), terminals for step up circuits and VR are open, and supply the LCD driving voltage from o utside due to the Step up circuits and Voltage adjust circuits are stop its operation.

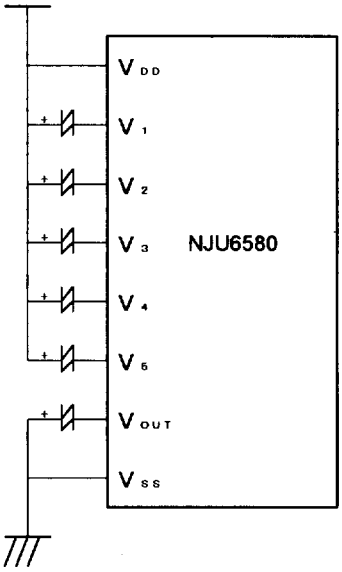
○ Examples for application circuits of the internal Power Supply

(1)None of the internal power supply functions.



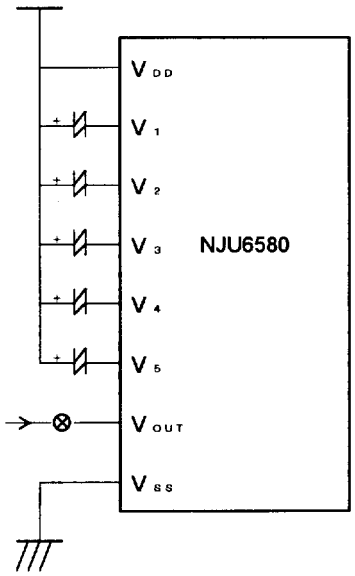
(2) All of the internal power supply functions.
(Step up, Voltage Adj., Buffer(V/F))

(T1,T2)=(L,*) * : Don't care.



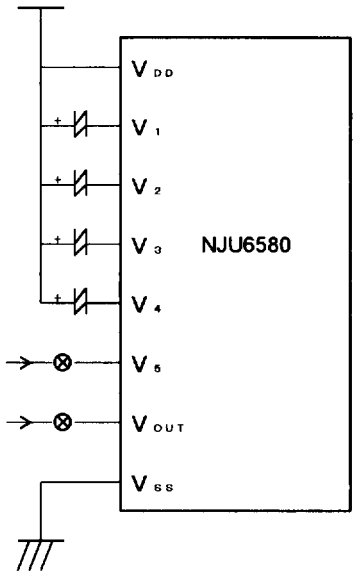
(3)Some of the internal power supply functions.
(Voltage Adjust., Buffer(V/F))

(T1,T2) = (H,L)



(4)Some of the internal power supply functions.
(Buffer(V/F))

(T1,T2) = (H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6580 distinguish the signal on the data bus by combination of A0, $\overline{RD}$ and $\overline{WR}$. Normally, the busy check is not required as the NJU6580 is operating so first because of the decode of the instruction and ex ecution are performs only depend on the internal timing which not depend on the external clock. In case o f serial interface, the data input as MSB first serially.

The Table. 3 shows the instruction codes of the NJU6580.

Table 3. Instruction Code

	Instruction	Code A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	*	*	Page Add.		Set the page of DD RAM to the Page Add. Register
(3)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								Read the Data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0 1	Inverse the On and Off Display 0:Normal 1:Inverse
(10)	Whole Display On	0	1	0	1	0	1	0	0	1	0	0 1	Whole Display Turns On 0:Normal 1:Whole Disp. On
(11)	Icon Display	0	1	0	1	0	1	0	1	0	1	0 1	Set the Duty Ratio 0:No Icon 1:With Icon
(12)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(15)	ComOutput / Scroll Set Up	0	1	0	1	1	0	0	A3	M	S1	S0	Set the COM (A3) and Scroll (M,S0,S1)
(16)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0 1	0:Int. Power Supply Off 1:Int. Power Supply On
(17)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal(external) power supply is turn on
(18)	EVR Register Set	0	1	0	1	0	0	Setting Data					Set the V_5 output level to the EVR register
(19)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power save Mode
(20)	Scroll Page Set	0	1	0	0	1	*	*	*	*	P1	P0	Set the Scroll Page P*=0:Used Scroll P*=1:No Scroll
(21)	Scroll On / Off Set	0	1	0	1	0	1	0	1	0	0	0 1	Scroll ON/OFF 0:OFF 1:ON
(22)	Data Request Reset	0	1	0	0	0	1	0	0	0	0	0	Reset the Data Request Signal

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 2 is a Icon display data area which available only for the D_0.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	1	*	*	A_1	A_0

(*:Don't Care)

A_1	A_0	Page
0	0	0
0	1	1
1	0	2

(c) Column Address

When MPU access the Display Data RAM, page address set(refer(b) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting.
This conver auto-increment up to $(A0)_H$, but accessing to the display data RAM over than $(6F)_H$ is forbidden. After writing 1 page data, page address setting is required due to page address doesn't increase automatically.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
Higher Order	0	1	0	0	0	0	1	A_7	A_6	A_5	A_4
Lower Order	0	1	0	0	0	0	0	A_3	A_2	A_1	A_0

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
			.					.
			.					.
0	1	1	0	1	1	1	1	6F

(d) Status Read

This instruction read out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.
0 :Counterclockwise Output(Inverse) Column Address 95-n ←→ Segment Driver n
1 :Clockwise Output (Normal) Column Address n ←→ Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On"
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initialization period by $\overline{RES}$ signal or reset instruction.
0 : —
1 : Initialization Period

(e) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increas e "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM witho ut any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
1	1	0	WRITE DATA						

(f) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page add ress. The column address increase "1" automatically when reading, therefore, the MPU can read the 8-bit da ta from the Display Data RAM without any address setting after the start address setting. One time of dumm y read is required after column address set as explain in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data can not be readout.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
1	0	1	READ DATA						

(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver out put. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no r estriction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	0	1	0	0	0	D

D 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Dat a RAM is no changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"
1: Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction executes the all pixel terns on regardless the contents of the Display Data RAM. In this time, the contents of Display Data RAM is no change and is kept. This instruction takes over precedence over th e "Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	0	1	0	0	1	0	D

D 0: Normal Display
1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the powe r save mode(refer to the (r) Power Save) .

(j) Icon Display

This instruction set the 1/33 duty for the Icon Display. The COMI terminal operate as COM_{32} and output th e icon display data stored in D_0 of Display Data RAM page 4(refer to the Fig. 1).

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	0	1	0	1	0	1	D

D 0: 1/16 Duty
1: 1/17 Duty

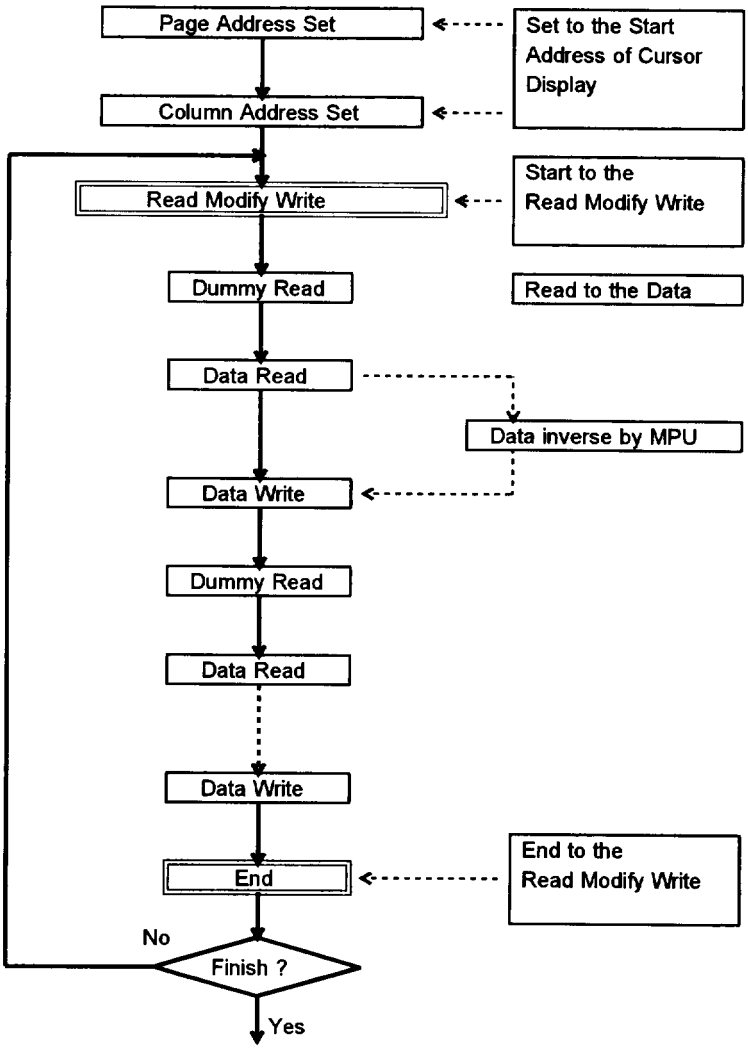
(k) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the Read Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction i s executed, but the address is no change when the Display Data Read Instruction is executed. This status is continued during End instruction execution. When the End instruction is entered the column address back t o the address where the Read Modify Write instruction entering. By this function, the load of MPU for examp le cyclic data writing operation like as cursor blink etc., can be reduced.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

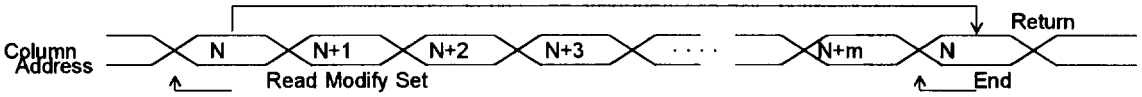
(l) Sequence of cursor display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
	0	1	0	1	1	1	0	1	1	1	0



(n) Reset

This instruction executes the following initialization.

Initialization

① Set the Address $(00)_H$ to the Column Address Counter.
② Set the page "0" to the Page Address Register.
③ Select the D_3 of the Output Assignment register to "0"
④ Set the EVR register to $(00)_H$
⑤ Set the 8x8bit Mode to the Scroll ,Set the speed 4 to the Scroll speed.
⑥ Release the All page to the Scroll page.

In this time, there are no influence to the Display Data RAM.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
	0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal must be required for the initialization when the power terns on. Substitution of Reset Instruction for the reset signal input to the $\overline{RES}$ terminal is not allowed.

(o) COM Output / Scroll Set Up

This instruction set the Common Driver scanning order and Scroll states.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
	0	1	0	1	1	0	0	A_3	M	S1	S0

A_3 : Set the Common Driver scanning order. (Refer to 1-6)
M : Set the Scroll Dot of 1-Characters
0 : 8x8 Dot Mode
1 : 16x16 Dot Mode
S0,S1 : Set the Scroll Speed in 4-step

	Scroll Speed	S1	S0	<CLI=400kHz, 1/16Duty>
fast	4	0	0	32.6 dot/sec
↑	3	0	1	16.3 dot/sec
↓	2	1	0	8.1 dot/sec
slow	1	1	1	4.1 dot/sec

(p) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is required.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
	0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q)LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 ~ V4 and output LCD driving waveform through the COM/SEG terminals.

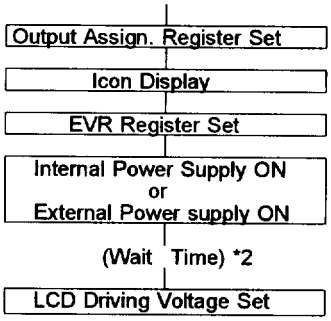
A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	1	0	1	1	0	1

NJU6580 contains operational amplifiers for LCD bias voltage V1 ~ V4. These amplifiers current are reduced in order to realize low power consumption. Because of this reduction, LCD driving voltage V1 ~ V4 might be unstable just after the internal power supply is turned on.
LCD Driving Voltage Set instruction is prepared for this unstableness.

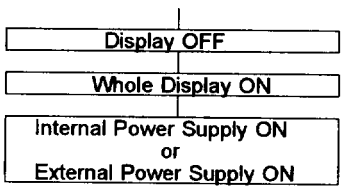
● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is tuned on/of.
When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence mentioned in (s) is required.

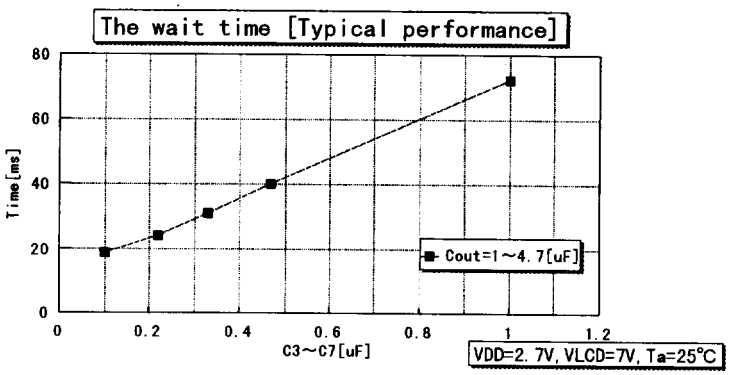
Turn ON sequence



Turn OFF sequence



*1 This instruction is required in both cases of the internal and external power supply.
Until "LCD driving voltage Set" execution, NJU6580 operating current is higher than usual state and all COM/ SEG terminals output V_{DD} level continuously except LCD driving waveform.
*2 The wait time depends on the C_3~ C_7, C_{OUT} capasitors((4) (d)Fig.5), V_{DD} and V_{LCD} voltage.
Therefore a test on actual module should be practiced. Refer to the following graph.



(r) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this inst ruction execute, the internal Electrical Variable Resistor(EVR) to change the V_5 output voltage, generate one voltage from 32 voltage state. The range of V_5 output level can be adjusted by the external resistance. F or more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

A0	$\overline{RD}$	R/$\overline{W}$ ($\overline{WR}$)	D_7							D_0
0	1	0	1	0	0	A_4	A_3	A_2	A_1	A_0

A_4	A_3	A_2	A_1	A_0	V_{LCD}
0	0	0	0	0	Low
		:			
		:			
1	1	1	1	1	High

$V_{LCD} = V_{DD} - V_5$

When EVR doesn't use, set the EVR register to (0,0,0,0,0).

(s) Power Save(Dual Command)

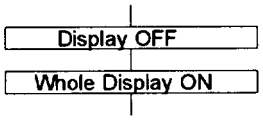
When both of Display Off and Whole Display On are executed, the internal circuits put on the power save mo de and the operating current is reduced as same as stand by current.
The internal status in the Power Save Mode is as follows;

① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
③ Keeping the display data and operating mode as before the power save mode.
④ All of LCD driving bias voltage fixed to the V_{DD} level.

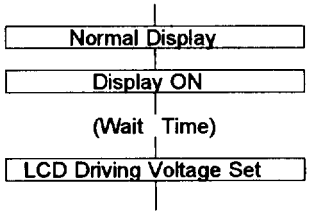
5

The power save and its release should be performed according to the following sequences.

Power Save Sequence



Power Save Release Sequence



*1 Power save mode requires dual-instruction. After the second instruction" whole Display ON", the power save mode starts.
*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.
*3 Until "LCD driving voltage set" execution, NJU6580 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.
*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.
*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

(t) Scroll Page Set

This instruction sets some Scroll Pages at the same time.

In case of 16x16 dots scroll mode, P_3 to P_0 data must be set from the following table.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	0	1	*	*	*	*	P_1	P_0

0 : No Scroll
1 : Scroll

(*:Don't Care)

<16 × 16 dot scroll mode>

P_1	P_0
1	1
0	0

(u) Scroll On/Off

This instruction sets the horizontal scroll On/Off.

When this instruction execute, the scroll performs under the condition set by both of COM Output, Scroll Set Up and Scroll Page Set instruction. When stop the scroll by this instruction, the scroll is not stopped immediat ely but after 7 dots (8x8 dots mode) or 15 dots (16x16 dots mode) shift performs completely.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	0	1	0	1	0	0	D

D 0: Scroll OFF
1: Scroll ON

(v) Data Request Reset

One character shift performs completely during the scroll operation, the DREQ terminal output the Data Requ est signal to the MPU. After rewrite the display data in the RAM, reset the DREQ terminal by this instructions required.

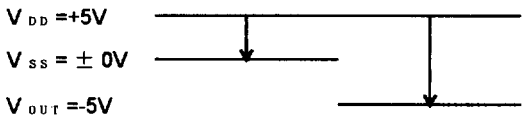
The timing of Data Request signal set is :

- In case of 16x16 dot mode : timing of COM_{14}
- In case of 8x8 dot mode : timing of COM_8, COM_{14}

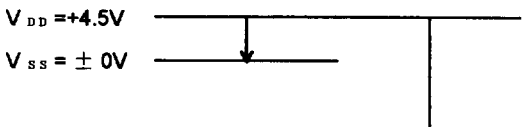
(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage(V_{DD} common) of the voltage V_{DD}-V_{SS} is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT}. In case of the voltage doubler operation, connect the two capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{OUT}, then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 4.5V.



Voltage Relation in Doubler



Voltage relation in Tripler

(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage can calculated by the following formula.

$$V_5 = V_{DD} - (1 + Rb/Ra) \cdot V_{REG} \quad \cdots\cdots ①$$

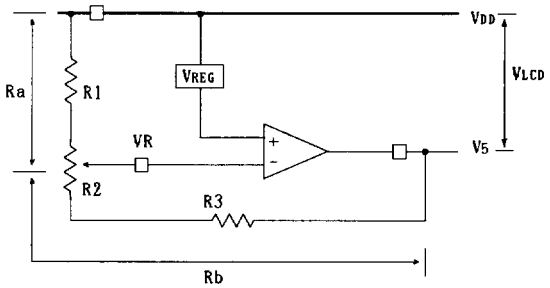


Fig. 4

Where, the V_{REG} is a constant voltage in the NJU6580 like as $V_{REG} \fallingdotseq 2.5V$.

To adjust the output voltage from V_5, connect the variable resistance among VR, V_{DD} and V_5 as shown in Fig. 4. When fine tuning for V_5 is needed, combine with the fixed resistance of R1, R3 and variable resistance of R2 is recommended as shown in Fig. 4.

Design example for R1, R2 and R3 (reference)

- R1+R2+R3=5M Ω (Determined by the current flown between V_{DD}-V_5)
- Variable voltage range by the R2. -2.5V ~ -4.5V (V_{DD}-V_5→ 7V ~ 9V)
  (Determined by the LCD electrical characteristics)

R1, R2 and R3 are calculated by above conditions and the formula of ① to mentioned below;

R1=1.388M Ω
R2=0.388M Ω
R3=3.214M Ω

The voltage adjust circuits has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuits serially.

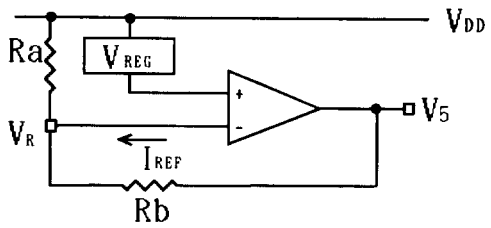
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_5 which controls LCD display contrast can adjust by the instruction. The EVR function is executed to set the 5 bits data into the EVR resistor and determine the one output voltage status out of 32 prefixed voltage status.

When execute the EVR function, set the T_1 and T_2 except the "H, H" and execute the Internal Power Supply On instruction.

[External parts constants setting example when EVR function using / reference]



(1) Determine the V_5 voltage range controlled by EVR.

LCD Driving Voltage	V_{DD}-V_5	7V ~ 9V
The range of V_5		2V

(2) Determine the Rb.

Rb = [The range of V_5] / I_{REF} (32 status I_{REF} ≒ 5 μA constant current)

Rb = 2V/5 μA = 400k Ω *Ta=25 ℃ V_{DD}-V_{OUT} =9V

(3) Adjust the Ra

$$Ra = \frac{V_{REG}}{([\text{LCD Driving Voltage}]-V_{REG})/Rb}$$

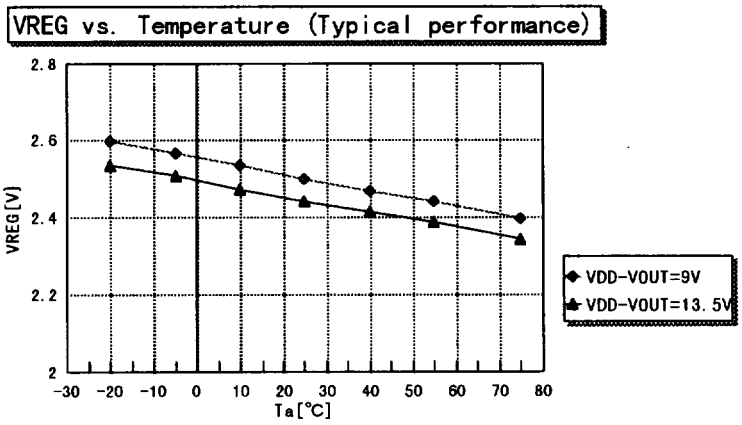
$$Ra = \frac{2.5\ V}{(7V-2.5V)/400k\ \Omega} = 222k\ \Omega$$

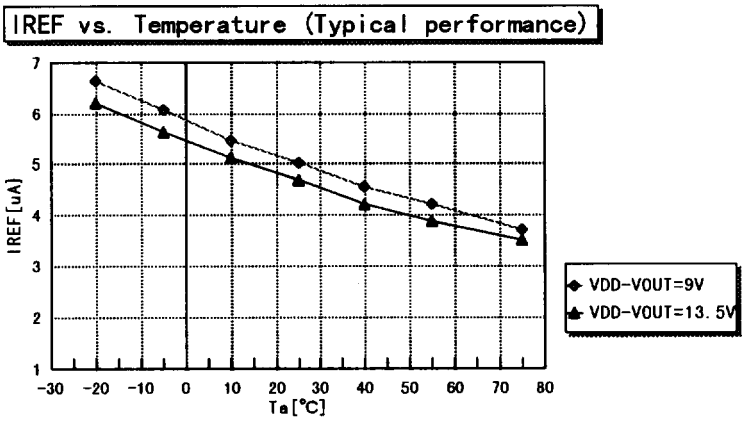
(4) Adjust the Ra

Adjust the Ra to good contrast of LCD display after the (D_4,D_3,D_2,D_1,D_0) of EVR register set to (1, 0, 0, 0, 0) or (0, 1, 1, 1, 1). When the EVR using, Ra use a variable resistance and contrast adjustment mentioned in (4) for each chip is required due to the I_{REF} is simple constant current source.

When the EVR function does not use, the (D_4,D_3,D_2,D_1,D_0) of EVR register set to (0, 0, 0, 0, 0) by the $\overline{RES}$ signal or the EVR Register Set instruction.

*) V_{REG}, I_{REF} depends on the voltage between V_{DD} and V_{OUT}, the operating temperature. Please refer to the following graphs.



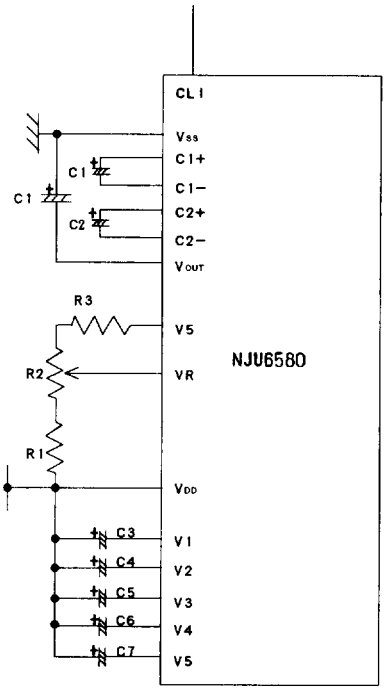


(d) LCD Driving Voltage Generation Circuits

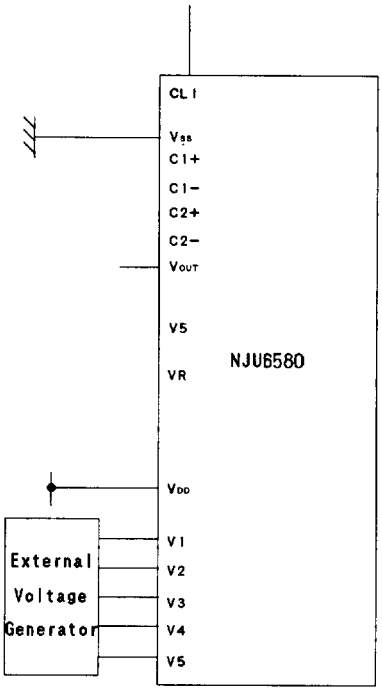
The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V_5 voltage by the bleeder resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 5 capacitor are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitor C3 to C7 determine by combine with the actual LCD panel.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

VLCD = VDD - V5 ≒ 7 ~ 9V

Item	Value
C1·C2	4.7~10μF
C3~C7	0.1~0.47μF
R1	1.388MΩ
R2	0.388MΩ
R3	3.214MΩ

Fig. 5

*1 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.

*2 Following connection of V_{OUT} is required when external power supply using.

When $V_{SS} > V_5$ – $V_{OUT} = V_5$

When $V_{SS} \leqq V_5$ – $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6580 can interface by using both of 8 bit bilateral data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined the P/S terminal connected to "H" or "L" level as shown in Table 4. In case of the serial interface, status and RAM data read out is impossible.

Table 4

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	-	-	$D_0 \sim D_7$
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6580 can interface both of 68 or 80 type MPU directly by setting the parallel interface (P/S="H") and "H" or "L" of the C86 terminal as shown in Table 5.

Table 5

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$
H	68 type MPU	$\overline{CS}$	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6580 discriminate the signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 6.

Table 6

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to $\overline{CS}$="L" , and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal is MSB first like as the order of D_7 to D_0, and the data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or $\overline{CS}$ terminal becomes "H" in spite of the data less then 8 bits, NJU6580 recognizes wrong data as a instruction data. Therefore 8bits data is required for the input data. The time chart for the serial interface is shown in Fig. 6. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface

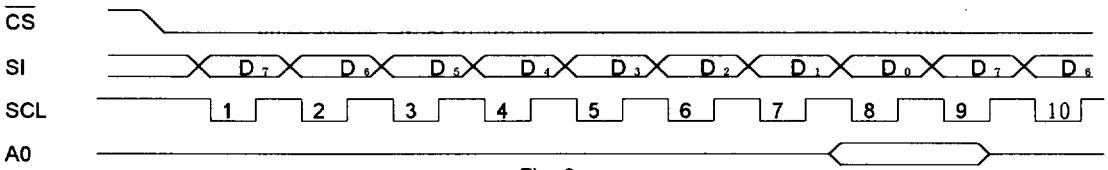


Fig. 6

(5-5) Access to the Display Data RAM and Internal Register.

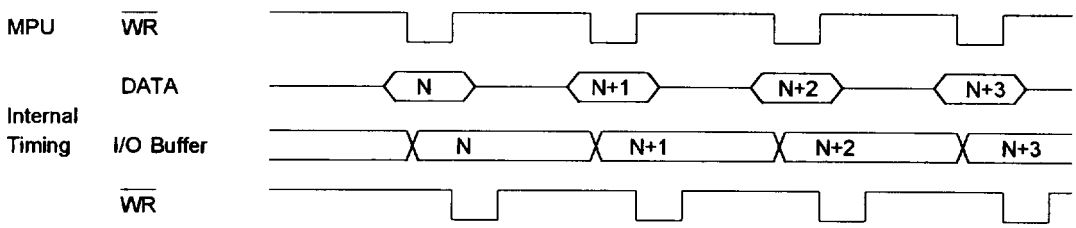
The NJU6580 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU read out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at next data read cycle. And when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6580 is available because of the limitation of access time of NJU6580 locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP operation cycle which equivalent to the waiting operation is useful.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 7.

● Write Operation



● Read Operation

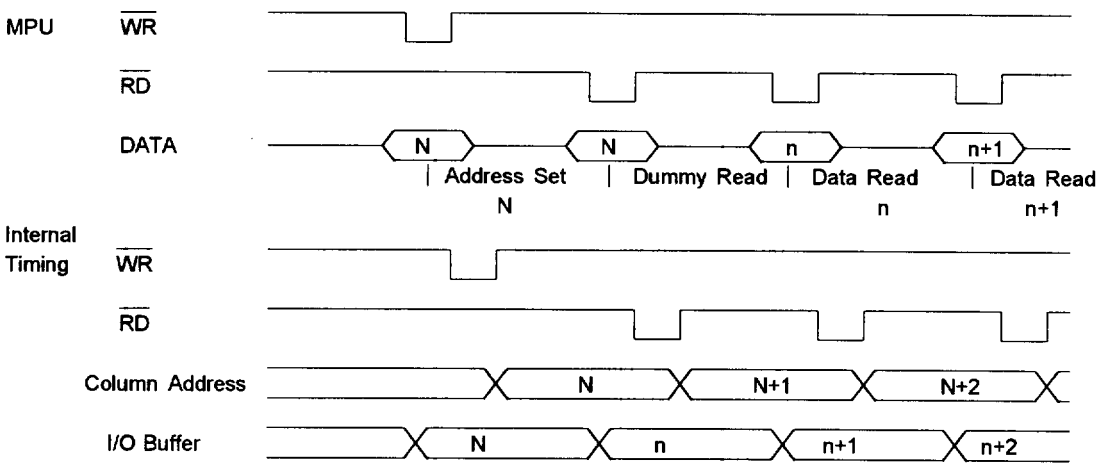


Fig. 7

(5-6) Chip Select

$\overline{CS}$ is Chip Select terminals. The Chip Select is executed by the setting of $\overline{CS}$="L" . Only the select mode, the interface with MPU is available. In the non select period, the D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, SI and SCL input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25 ℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	− 0.3 ～ + 7.0 − 0.3 ～ + 4.5 (used Tripler)	V
Supply Voltage (2)	V_5	V_{DD}−13.5 ～ V_{DD}+0.3	V
Supply Voltage (3)	V_1～V_4	V_5 ～ V_{DD}+0.3	V
Input Voltage	V_{IN}	− 0.3 ～ V_{DD}+0.3	V
Operating Temperature	Topr	− 30 ～ + 80	℃
Storage Temperature	Tstg	− 55 ～ + 125 (Chip) − 55 ～ + 100 (TCP)	℃

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the Voltage converter.

■ ELECTRICAL CHARACTERISTICS (1)

(V_{DD} =5V ± 10%, V_{SS} =0V, Ta=−20 ～ +75 ℃)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage (1)	Recommend	V_{DD}			4.5	5.0	5.5	V	5
	Available				2.4		5.5		
Operating Voltage (2)	Recommend	V_5			V_{DD}−13.5		V_{DD}−3.5	V	
	Available				V_{DD}−13.5				
	Available	V_1, V_2	V_{LCD}=V_{DD}−V_5		V_{DD}−0.6xV_{LCD}		V_{DD}		
	Available	V_3, V_4			V_5		V_{DD}−0.4xV_{LCD}		
Input Voltage	1	V_{IHC1}	A0, D_0～D_7,		0.7xV_{DD}		V_{DD}	V	
		V_{IHC2}	$\overline{RD}$, $\overline{WR}$, $\overline{CS}$,	V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
	2	V_{ILC1}	$\overline{RES}$, C86, SI, SCL, P/S Terminals		V_{SS}		0.3xV_{DD}		
		V_{ILC2}		V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		
Output Voltage	1	V_{OHC11}	D_0～D_7, DREQ Terminals	I_{OH}=−1mA	0.8xV_{DD}		V_{DD}	V	
		V_{OHC12}		I_{OH}=−0.5mA V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
	2	V_{OLC11}	D_0～D_7, DREQ Terminals	I_{OL}= 1mA	V_{SS}		0.2xV_{DD}		
		V_{OLC12}		I_{OL}= 0.5mA V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		

■ ELECTRICAL CHARACTERISTICS (2)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Input Leakage Current		I_{LI}	All Input Terminals		-1.0		1.0	uA	
		I_{LO}	D_0~D_7 Terminals		-3.0		3.0		6
Driver On-resistance		R_{ON1}	Ta=25℃			2.0	3.0	kΩ	7
		R_{ON2}	V_{LCD}= 8.0V	V_{DD}=2.7V		3.0	4.5		
Stand-by Current		I_{DDQ}	During power Save mode			0.05	5.0	uA	8
Operating Current		I_{DD12}	Display			30	(TBD)	uA	
		I_{DD14}	V_{LCD}= 8.0V	V_{DD}=2.7V		22	(TBD)		
		I_{DD21}	Accessing fcyc=200kHz			217	(TBD)		9
		I_{DD22}		V_{DD}=2.7V		77	(TBD)		
Input Terminal Capacitance		C_{IN}	Ta=25℃ A0, D_0~D_7, $\overline{RD}$, $\overline{WR}$, CS, RES, C86, SI, SCL, P/S, T1, T2 Terminals			10		pF	
Operation Clock		f_{CLI}	V_{DD}=5.0V		(TBD)	400	(TBD)	kHz	
Voltage Tripler	Input Voltage	V_{DD1}	V_{DD}-V_{SS}		2.4		5.5	V	
		V_{DD2}	V_{DD}-V_{SS}, used Tripler		2.4		4.5		10
	Output Volt.	V_{OUT}	V_{SS}-V_{LCD}, used Tripler		-9.0			V	
	On -resistance	R_{TRI}	V_{DD}=3V; C=4.7uF used Tripler			640	(TBD)	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Tripler Circuit "OFF"		V_{DD}-13.5		V_{DD}-5.0	V	11
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"		V_{DD}-13.5		V_{DD}-5.0	V	
	Operating Current	I_{OUT1}	V_{DD}=4.5V, V_{LCD}=8V			45	(TBD)	uA	12
		I_{OUT2}	COM/SEG Term. Open, No Access Display check. pattern			16	(TBD)		
		I_{OUT3}				14	(TBD)		
	Voltage Reg.	V_{REG}	V_{DD}-V_{out}=9V; Ta=25℃		(TBD)	2.5	(TBD)	V	13
	Reference Current	I_{REF}	V_{DD}-V_{out}=9V; Ta=25℃		(TBD)	5.0	(TBD)	uA	

Note 5) NJU6580 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D_0 to D_7 terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage set.

Note 8) Apply to no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 10) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

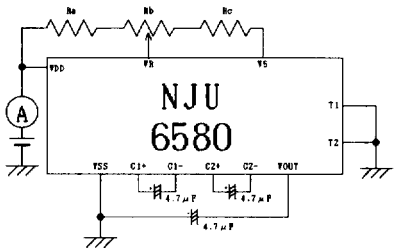
Note 12) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T1	T2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT}, V_6)

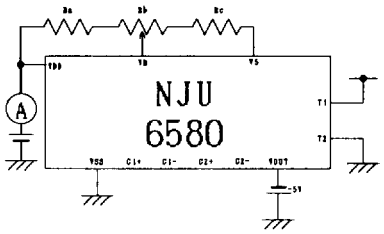
* = Don't Care

Note 13) Apply to the precision of Voltage on each EVR steps.

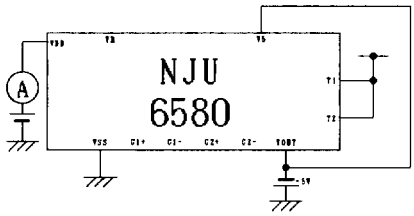
MEASUREMENT BLOCK DIAGRAM : I_{OUT1} Ra+Rb+Rc=2M Ω



: I_{OUT2} Ra+Rb+Rc=2M Ω



: I_{OUT3}



■ ELECTRICAL CHARACTERISTICS (3)

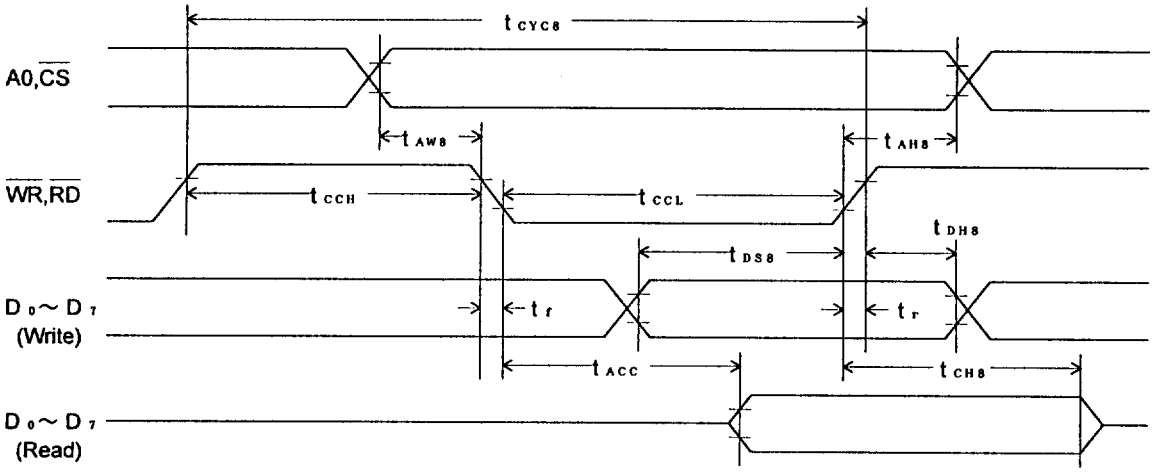
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}		10			us	15

Note 14) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.

Note 15) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

■ BUS TIMING CHARACTERISTICS

・ Read/Write operation sequence (80 Type MPU)



(V_{DD}=5.0V±10%, Ta=-20～75°C)

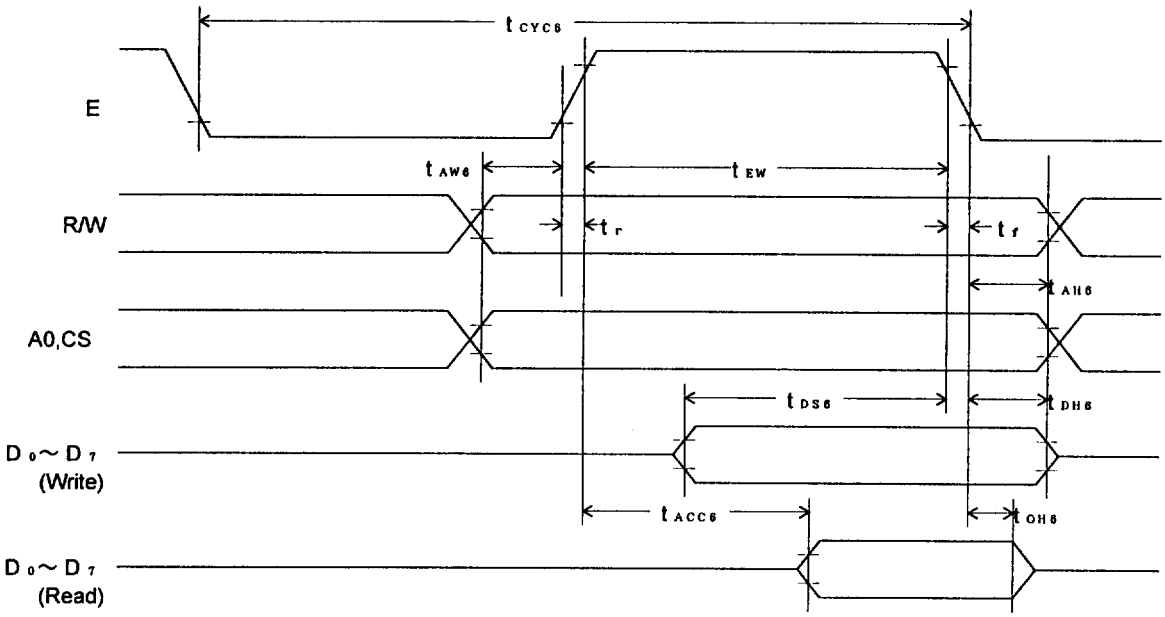
PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, CS Terminals	t_{AH8}	10			ns
Address Set Up Time			t_{AW8}	10			
System Cycle Time		WR, RD Terminals	t_{CYC8}	200			
Control Pulse Width	WR, "L"		t_{CCL} (W)	25			
	RD, "L"		t_{CCL} (R)	80			
	"H"		t_{CCH}	90			
Data Set Up Time		D0～D7 Terminals	t_{DS8}	60			
Data Hold Time			t_{DH8}	10			
RD Access Time			t_{ACC8}		70	CL=100pF	
Output Disable Time			t_{OH8}	0	30		
Rise Time, Fall Time		CS, WR, RD, A0, D0～D7 Terminals	t_r, t_f		15		

(V_{DD}=2.7V～4.5V, Ta=-20～75°C)

PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, CS Terminals	t_{AH8}	25			ns
Address Set Up Time			t_{AW8}	25			
System Cycle Time		WR, RD Terminals	t_{CYC8}	450			
Control Pulse Width	WR, "L"		t_{CCL} (W)	50			
	RD, "L"		t_{CCL} (R)	200			
	"H"		t_{CCH}	220			
Data Set Up Time		D0～D7 Terminals	t_{DS8}	120			
Data Hold Time			t_{DH8}	35			
RD Access Time			t_{ACC8}		140	CL=100pF	
Output Disable Time			t_{OH8}	0	35		
Rise Time, Fall Time		CS, WR, RD, A0, D0～D7 Terminals	t_r, t_f		15		

Note 15) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 16) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

· Read/Write operation sequence (68 Type MPU)



(VDD=5.0V±10%, Ta=-20～75°C)

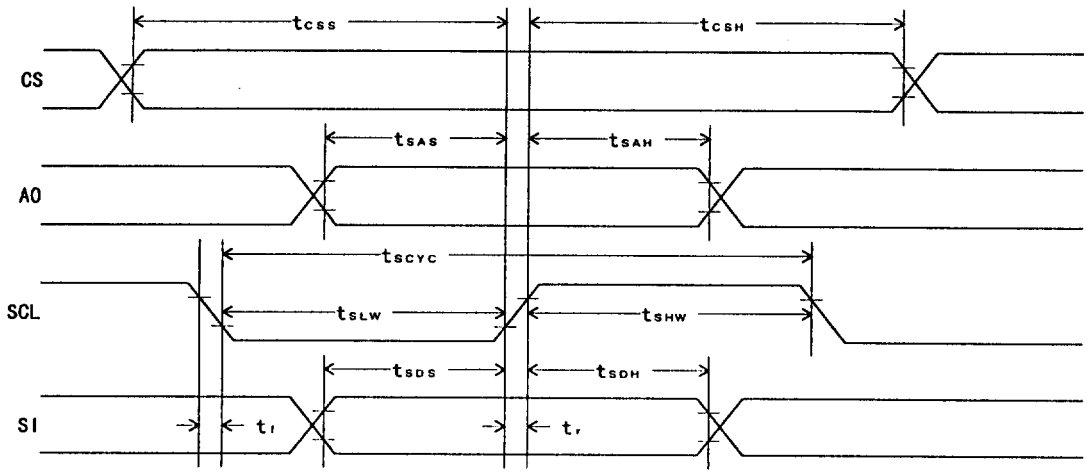
PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS, R/W Terminals	tAH6	10			ns
Address Set Up Time		tAW6	10			
System Cycle Time		tCYC6	200			
Enable Pulse Width	Read	tEW	100			
	Write		25			
Data Set Up Time	D0～D7 Terminals	tDS6	60			
Data Hold Time		tDH6	20			
Access Time		tACC6		70	CL=100pF	
Output Disable Time		tOH6	0	25		
Rise Time, Fall Time	A0, $\overline{CS}$, R/W, E, D0～D7 Terminals	tr, tf		15		

(VDD=2.7V～4.5V, Ta=-20～75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS, R/W Terminals	tAH6	25			ns
Address Set Up Time		tAW6	25			
System Cycle Time		tCYC6	450			
Enable Pulse Width	Read	tEW	200			
	Write		50			
Data Set Up Time	D0～D7 Terminals	tDS6	120			
Data Hold Time		tDH6	40			
Access Time		tACC6		140	CL=100pF	
Output Disable Time		tOH6	0	45		
Rise Time, Fall Time	A0, $\overline{CS}$, R/W, E, D0～D7 Terminals	tr, tf		15		

Note 17) t_{CYC6} indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.
Note 18) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 19) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

・ Read/Write operation sequence (Serial Interface)



(VDD=5.0V±10%, Ta=-20～75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC	500			ns
SCL "H" pulse width		tSHW	150			
SCL "L" pulse width		tSLW	150			
Address Set Up Time	A0 Terminal	tSAS	120			
Address Hold Time		tSAH	200			
Data Set Up Time	SI Terminal	tSDS	120			
Data hold Time		tSDH	50			
CS-SCL Time	CS Terminals	tCSS	30			
		tCSH	400			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	tr, tf		15		

(VDD=2.7V～4.5V, Ta=-20～75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC	1000			ns
SCL "H" pulse width		tSHW	300			
SCL "L" pulse width		tSLW	300			
Address Set Up Time	A0 Terminal	tSAS	250			
Address Hold Time		tSAH	400			
Data Set Up Time	SI Terminal	tSDS	250			
Data hold Time		tSDH	100			
CS-SCL Time	CS Terminals	tCSS	60			
		tCSH	800			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	tr, tf		15		

Note 20) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 21) Each timing is specified based on 0.2xVDD and 0.8xVDD.

■ LCD DRIVING WAVEFORM

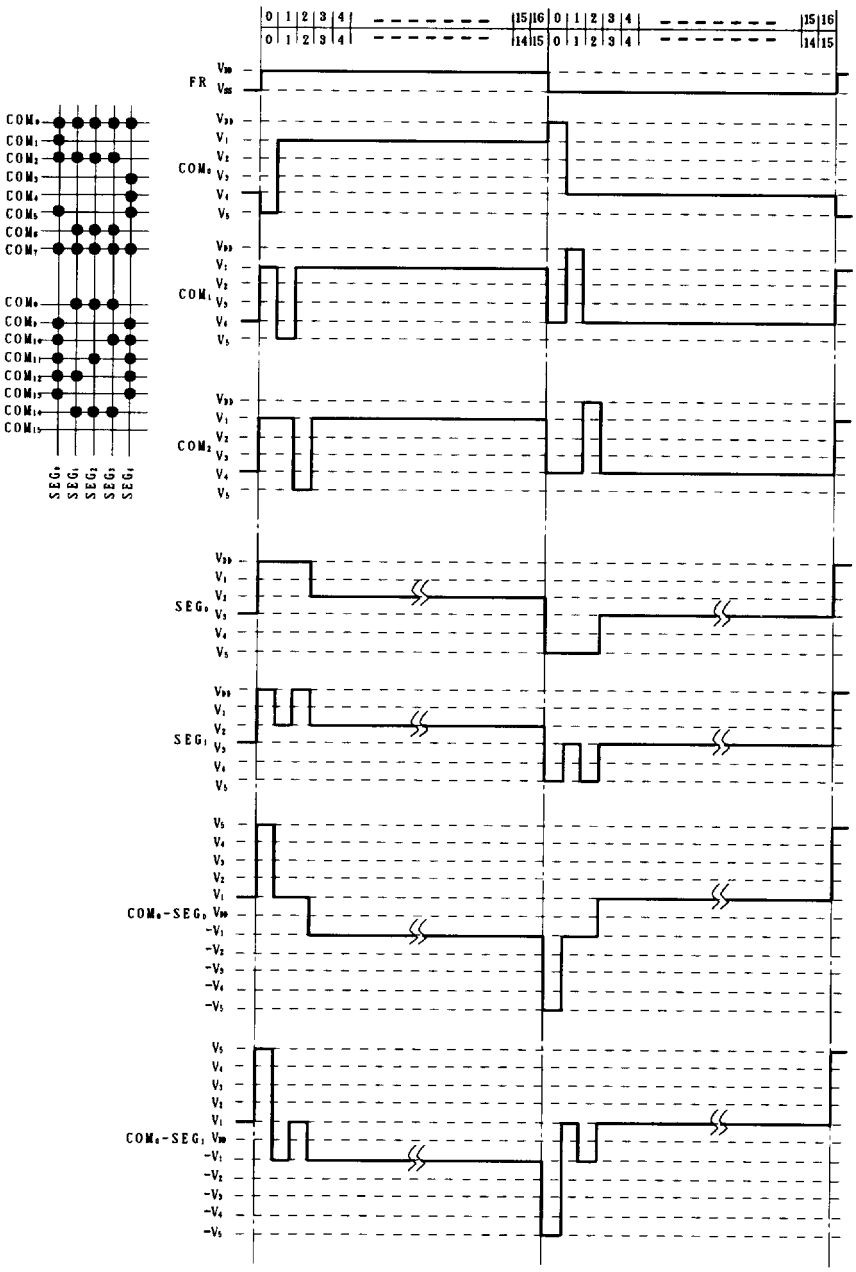


Fig. 8

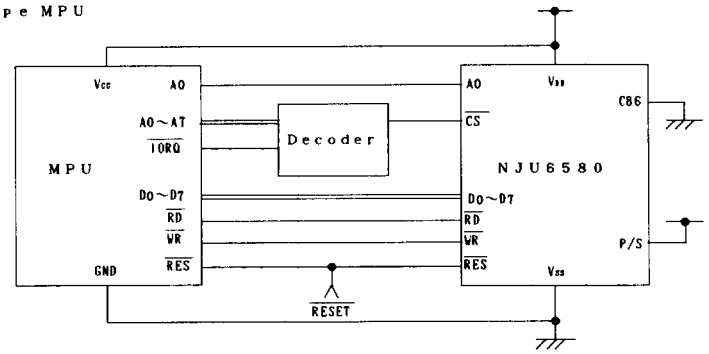
■ APPLICATION CIRCUIT

(1)Microprocessor Interface Examples

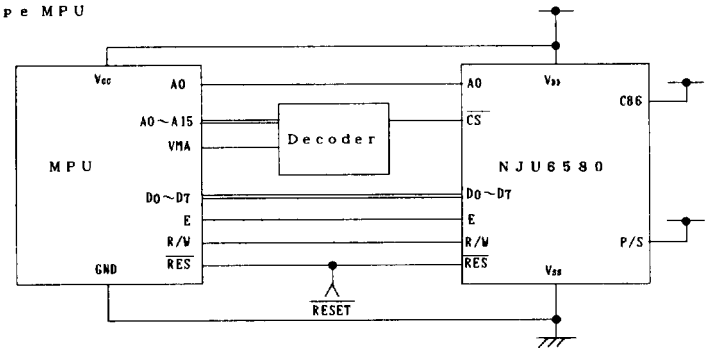
The NJU6580 can interface with both of 80 type and 68 type MPU by the serial format directly. Therefore minimum wiring for the MPU interface is available.

※ : C86 terminal must be fixed V_{DD} or V_{SS} .

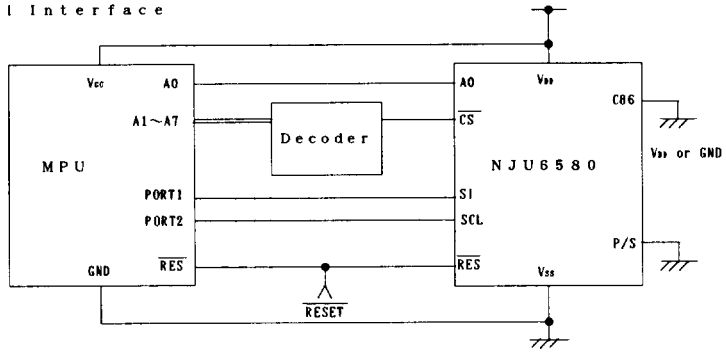
●80 Type MPU



●68 Type MPU



●Serial Interface



5