BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6579 is a bit map LCD driver to display graphics or characters.

It contains 8,710 bits display data RAM, microprocessor interface circuits, instruction decoder, 134-segment and 65-common (1 out of 65-driver is prepared for icon display) drivers.

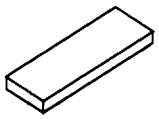
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel mode.

65 x 134 dots graphics or 8-character 4-line by 16 x 16 dot character with icon are displayed by NJU6579 itself.

Furthermore, NJU6579 contains accurate Electrical variable Resistors and is rectangle-shaped for COG and Slim TCP.

The wide operating voltage like as 2.4V to 5.5V and low operating current are useful to apply small sized battery operated items.

■ PACKAGE OUTLINE



NJU6579C

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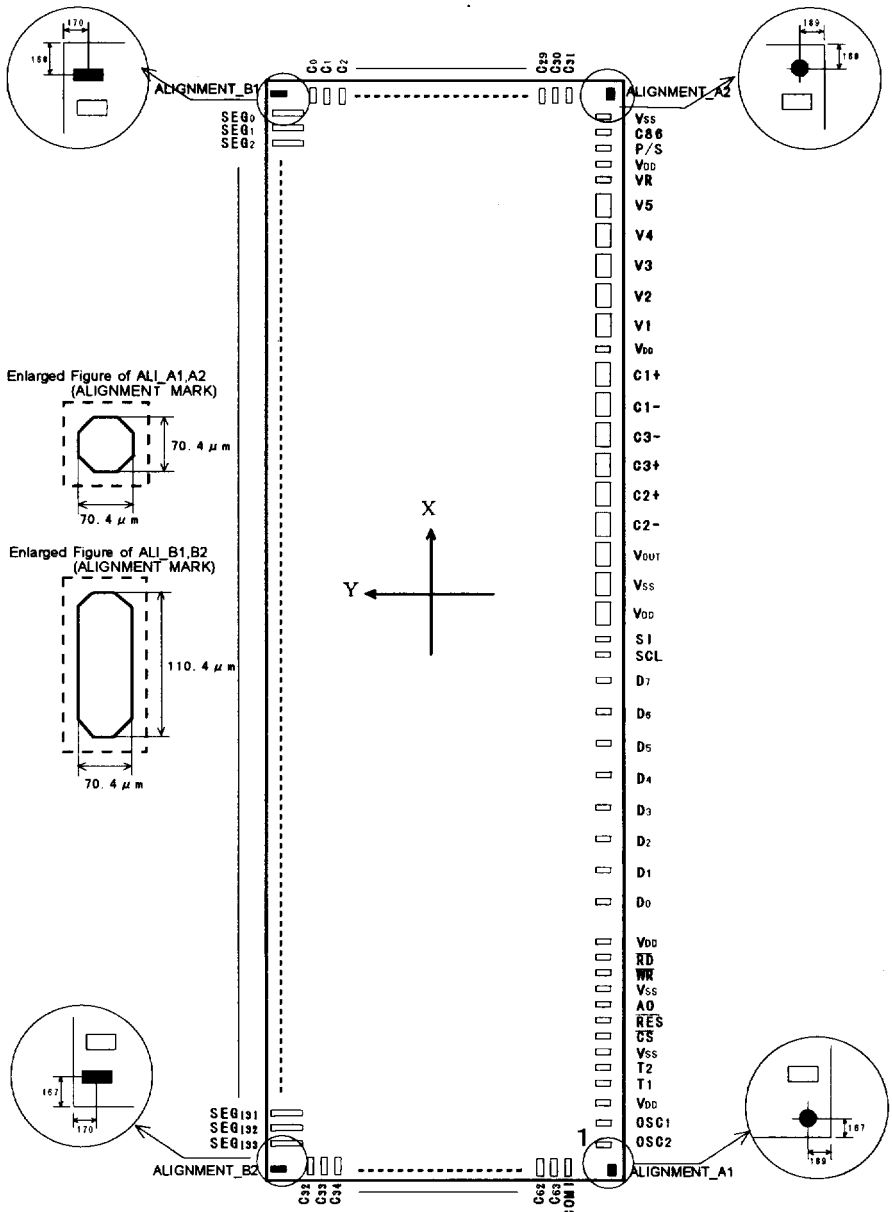
■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 8,710 bits
- 199 LCD Drivers - 65- common and 134-segment
- Direct Interface with both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/64 or 1/65 Duty
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Electrical Variable Resistor Function
- Low Power Consumption
- Operating Voltage --- 2.4V ~ 5.5V
- LCD Driving Voltage --- 6.0V ~ 13.5V
- Package Outline --- Chip / Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip Center	X=0um, Y=0um
Chip Size	X=11.36mm, Y=3.42mm
Chip Thickness	400um ± 30um
Pad Size	100um × 50um (PAD NO. 1～23, 33, 39～75, 210～242)
	210um × 100um (PAD NO. 24～32, 34～38)
	200um × 40um (PAD NO. 76～209)
Bump Height	25um TYP.
Bump Material	Au

■ : Four PADs illustrated with this mark are the alignment marks for COG.

■ PAD COORDINATES

Chip Size 11.36 mm x 3.42 mm(Chip Center X=0um,Y=0um)

NO.	Termi.	X= μm	Y= μm	No.	Termi.	X= μm	Y= μm	No.	Termi.	X= μm	Y= μm
1	OSC_2	-4512	-1515	51	C_{24}	5486	-645	101	SEG_{25}	2944	1464
2	OSC_1	-4432	-1515	52	C_{23}	5486	-565	102	SEG_{26}	2874	1464
3	V_{DD}	-4352	-1515	53	C_{22}	5486	-485	103	SEG_{27}	2804	1464
4	T_1	-4272	-1515	54	C_{21}	5486	-405	104	SEG_{28}	2734	1464
5	T_2	-4192	-1515	55	C_{20}	5486	-325	105	SEG_{29}	2664	1464
6	V_{SS}	-4112	-1515	56	C_{19}	5486	-245	106	SEG_{30}	2594	1464
7	$\overline{CS}$	-4032	-1515	57	C_{18}	5486	-165	107	SEG_{31}	2524	1464
8	$\overline{RES}$	-3952	-1515	58	C_{17}	5486	-85	108	SEG_{32}	2454	1464
9	A0	-3872	-1515	59	C_{16}	5486	-5	109	SEG_{33}	2384	1464
10	V_{SS}	-3792	-1515	60	C_{15}	5486	76	110	SEG_{34}	2314	1464
11	$\overline{WR}$	-3712	-1515	61	C_{14}	5486	156	111	SEG_{35}	2244	1464
12	RD	-3632	-1515	62	C_{13}	5486	236	112	SEG_{36}	2174	1464
13	V_{DD}	-3552	-1515	63	C_{12}	5486	316	113	SEG_{37}	2104	1464
14	D_0	-3257	-1515	64	C_{11}	5486	396	114	SEG_{38}	2034	1464
15	D_1	-2757	-1515	65	C_{10}	5486	476	115	SEG_{39}	1964	1464
16	D_2	-2257	-1515	66	C_9	5486	556	116	SEG_{40}	1894	1464
17	D_3	-1757	-1515	67	C_8	5486	636	117	SEG_{41}	1824	1464
18	D_4	-1257	-1515	68	C_7	5486	716	118	SEG_{42}	1754	1464
19	D_5	-757	-1515	69	C_6	5486	796	119	SEG_{43}	1684	1464
20	D_6	-257	-1515	70	C_5	5486	876	120	SEG_{44}	1614	1464
21	D_7	244	-1515	71	C_4	5486	956	121	SEG_{45}	1544	1464
22	SCL	591	-1515	72	C_3	5486	1036	122	SEG_{46}	1474	1464
23	SI	671	-1515	73	C_2	5486	1116	123	SEG_{47}	1404	1464
24	V_{DD}	831	-1515	74	C_1	5486	1196	124	SEG_{48}	1334	1464
25	V_{SS}	1071	-1515	75	C_0	5486	1276	125	SEG_{49}	1264	1464
26	V_{OUT}	1311	-1515	76	SEG_0	4694	1464	126	SEG_{50}	1194	1464
27	$C2^-$	1551	-1515	77	SEG_1	4624	1464	127	SEG_{51}	1124	1464
28	$C2^+$	1791	-1515	78	SEG_2	4554	1464	128	SEG_{52}	1054	1464
29	$C3^+$	2031	-1515	79	SEG_3	4484	1464	129	SEG_{53}	984	1464
30	$C3^-$	2271	-1515	80	SEG_4	4414	1464	130	SEG_{54}	914	1464
31	$C1^-$	2511	-1515	81	SEG_5	4344	1464	131	SEG_{55}	844	1464
32	$C1^+$	2751	-1515	82	SEG_6	4274	1464	132	SEG_{56}	774	1464
33	V_{DD}	2911	-1515	83	SEG_7	4204	1464	133	SEG_{57}	704	1464
34	V_1	3071	-1515	84	SEG_8	4134	1464	134	SEG_{58}	634	1464
35	V_2	3311	-1515	85	SEG_9	4064	1464	135	SEG_{59}	564	1464
36	V_3	3551	-1515	86	SEG_{10}	3994	1464	136	SEG_{60}	494	1464
37	V_4	3791	-1515	87	SEG_{11}	3924	1464	137	SEG_{61}	424	1464
38	V_5	4031	-1515	88	SEG_{12}	3854	1464	138	SEG_{62}	354	1464
39	VR	4191	-1515	89	SEG_{13}	3784	1464	139	SEG_{63}	284	1464
40	V_{DD}	4271	-1515	90	SEG_{14}	3714	1464	140	SEG_{64}	214	1464
41	P/S	4351	-1515	91	SEG_{15}	3644	1464	141	SEG_{65}	144	1464
42	C86	4431	-1515	92	SEG_{16}	3574	1464	142	SEG_{66}	74	1464
43	V_{SS}	4511	-1515	93	SEG_{17}	3504	1464	143	SEG_{67}	4	1464
44	C_{31}	5486	-1205	94	SEG_{18}	3434	1464	144	SEG_{68}	-66	1464
45	C_{30}	5486	-1125	95	SEG_{19}	3364	1464	145	SEG_{69}	-136	1464
46	C_{29}	5486	-1045	96	SEG_{20}	3294	1464	146	SEG_{70}	-206	1464
47	C_{28}	5486	-965	97	SEG_{21}	3224	1464	147	SEG_{71}	-276	1464
48	C_{27}	5486	-885	98	SEG_{22}	3154	1464	148	SEG_{72}	-346	1464
49	C_{26}	5486	-805	99	SEG_{23}	3084	1464	149	SEG_{73}	-416	1464
50	C_{25}	5486	-725	100	SEG_{24}	3014	1464	150	SEG_{74}	-486	1464

No.	Terminal	X= μm	Y= μm
151	SEG_{76}	-556	1464
152	SEG_{76}	-626	1464
153	SEG_{77}	-696	1464
154	SEG_{78}	-766	1464
155	SEG_{79}	-836	1464
156	SEG_{80}	-906	1464
157	SEG_{81}	-976	1464
158	SEG_{82}	-1046	1464
159	SEG_{83}	-1116	1464
160	SEG_{84}	-1186	1464
161	SEG_{85}	-1256	1464
162	SEG_{86}	-1326	1464
163	SEG_{87}	-1396	1464
164	SEG_{88}	-1466	1464
165	SEG_{89}	-1536	1464
166	SEG_{90}	-1606	1464
167	SEG_{91}	-1676	1464
168	SEG_{92}	-1746	1464
169	SEG_{93}	-1816	1464
170	SEG_{94}	-1886	1464
171	SEG_{95}	-1956	1464
172	SEG_{96}	-2026	1464
173	SEG_{97}	-2096	1464
174	SEG_{98}	-2166	1464
175	SEG_{99}	-2236	1464
176	SEG_{100}	-2306	1464
177	SEG_{101}	-2376	1464
178	SEG_{102}	-2446	1464
179	SEG_{103}	-2516	1464
180	SEG_{104}	-2586	1464
181	SEG_{105}	-2656	1464
182	SEG_{106}	-2726	1464
183	SEG_{107}	-2796	1464
184	SEG_{108}	-2866	1464
185	SEG_{109}	-2936	1464
186	SEG_{110}	-3006	1464
187	SEG_{111}	-3076	1464
188	SEG_{112}	-3146	1464
189	SEG_{113}	-3216	1464
190	SEG_{114}	-3286	1464
191	SEG_{115}	-3356	1464
192	SEG_{116}	-3426	1464
193	SEG_{117}	-3496	1464
194	SEG_{118}	-3566	1464
195	SEG_{119}	-3636	1464
196	SEG_{120}	-3706	1464
197	SEG_{121}	-3776	1464
198	SEG_{122}	-3846	1464
199	SEG_{123}	-3916	1464

No.	Terminal	X= μm	Y= μm
200	SEG_{124}	-3986	1464
201	SEG_{125}	-4056	1464
202	SEG_{126}	-4126	1464
203	SEG_{127}	-4196	1464
204	SEG_{128}	-4266	1464
205	SEG_{129}	-4336	1464
206	SEG_{130}	-4406	1464
207	SEG_{131}	-4476	1464
208	SEG_{132}	-4546	1464
209	SEG_{133}	-4616	1464
210	C_{32}	-5487	1276
211	C_{33}	-5487	1196
212	C_{34}	-5487	1116
213	C_{35}	-5487	1036
214	C_{36}	-5487	956
215	C_{37}	-5487	876
216	C_{38}	-5487	796
217	C_{39}	-5487	716
218	C_{40}	-5487	636
219	C_{41}	-5487	556
220	C_{42}	-5487	476
221	C_{43}	-5487	396
222	C_{44}	-5487	316
223	C_{45}	-5487	236
224	C_{46}	-5487	156
225	C_{47}	-5487	76
226	C_{48}	-5487	-5
227	C_{49}	-5487	-85
228	C_{50}	-5487	-165
229	C_{51}	-5487	-245
230	C_{52}	-5487	-325
231	C_{53}	-5487	-405
232	C_{54}	-5487	-485
233	C_{55}	-5487	-565
234	C_{56}	-5487	-645
235	C_{57}	-5487	-725
236	C_{58}	-5487	-805
237	C_{59}	-5487	-885
238	C_{60}	-5487	-965
239	C_{61}	-5487	-1045
240	C_{62}	-5487	-1125
241	C_{63}	-5487	-1205
242	COMI	-5487	-1285
ALIGNMENT	ALI_B1	-5513	-1521
ALIGNMENT	ALI_B2	5512	-1521
ALIGNMENT	ALI_A1	5512	1540
ALIGNMENT	ALI_A2	-5513	1540

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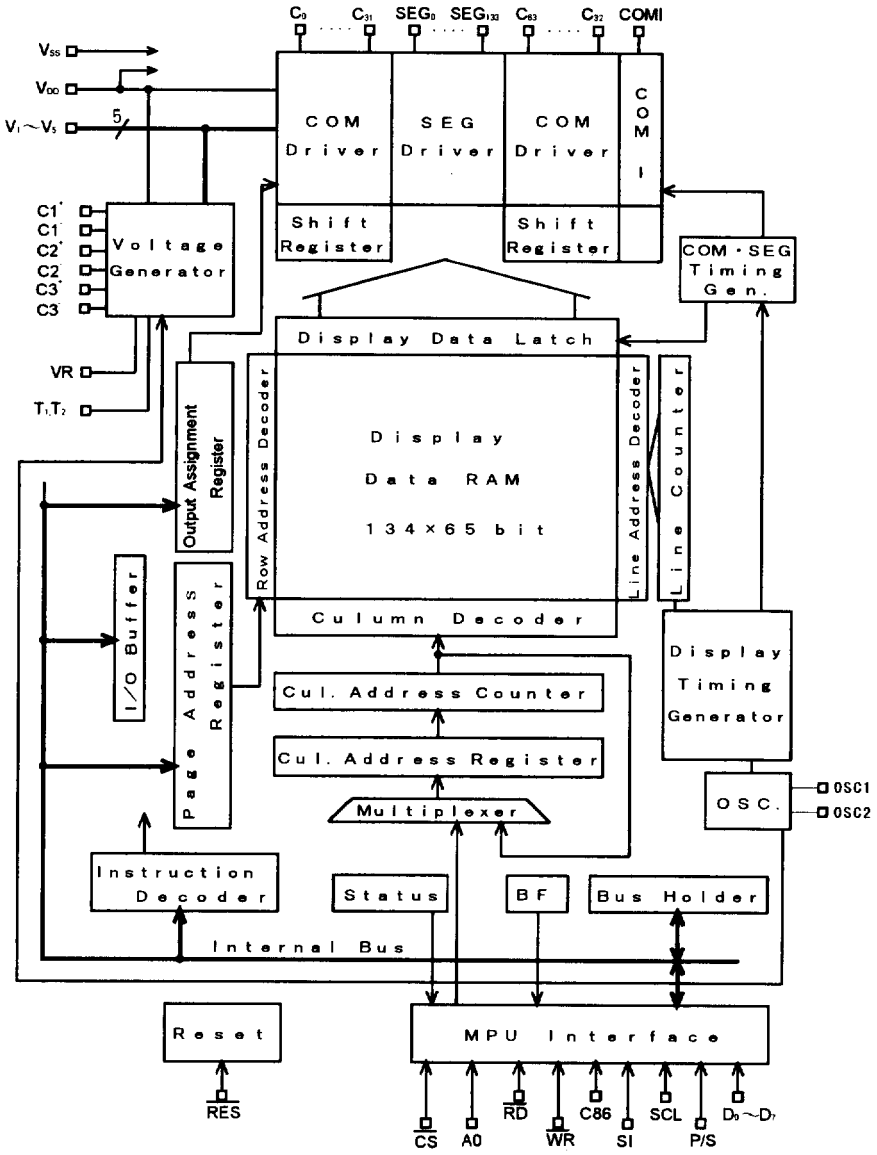
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function
3, 13, 24, 33, 40	V_{DD}	Power	V_{DD} =+3V. (Less then 4.5V should apply when voltage tripler using.) (Less then 3.3V should apply when voltage quadrupler using.)
6, 10, 25, 43	V_{SS}	GND	V_{SS} =0V
34 35 36 37 38	V_1 V_2 V_3 V_4 V_5	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ When internal power supply is on, internal circuits generated and supply following LCD bias voltage to $V_1 \sim V_4$ terminals. The ratio of LCD bias is selected by "LCD bias set" instruction.

Term.	V_1	V_2	V_3	V_4
Volt.	$V_5+6/7V_{LCD}$	$V_5+5/7V_{LCD}$	$V_5+2/7V_{LCD}$	$V_5+1/7V_{LCD}$

($V_{LCD}=V_{DD}-V_5$)

32 31 28 27 29 30	$C1^+$ $C1^-$ $C2^+$ $C2^-$ $C3^+$ $C3^-$	O	Step up capacitor connecting terminals. - In case of quadrupler operation, connect the capacitors between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, and $C3^+$ and $C3^-$. - In case of tripler operation, connect the capacitors between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, connect $C2^-$ to $C3^-$, and $C3^+$ is open. (or connect the capacitors between $C1^+$ and $C1^-$, $C3^+$ and $C3^-$, connect $C2^+$ to $C3^+$, and $C2^-$ is open.) - In case of doubler operation, connect the capacitor between $C1^+$ and $C1^-$, connect $C1^-$ to $C3^-$, and $C2^-$, $C2^+$, $C3^+$ are open.
26	V_{OUT}	O	Step up voltage output terminal. Connect the set up capacitor between this terminal and V_{SS}.
39	VR	I	Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance connect between V_{DD} and V5 terminal.
4 5	T_1 T_2	I	LCD bias voltage control terminals. ※ Don't Care

T_1	T_2	Step up cir.	Voltage Adj.	V/F Cir.
L	※	Available	Available	Available
H	L	Not Avail.	Available	Available
H	H	Not Avail.	Not Avail.	Available

14~21	$D_0 \sim D_7$	I/O	Tri-state bilateral Data I/O terminal when 8-bit parallel operation.
9	A0	I	Connect to the Address bus of MPU. The data on the D_0 to D_7 is distinguished Display data or Instruction by this signal.

A0	H	L
Dist.	Display Data	Instruction

8	$\overline{RES}$	I	Reset terminal. When the $\overline{RES}$ terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of $\overline{RES}$.
7	$\overline{CS}$	I	Chip select terminal. Data Input/Output are available during $\overline{CS}$ ="L".

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<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>12</td><td>$\overline{RD}$
(E)</td><td>I</td><td><When interface with 80 type MPU>
$\overline{RD}$ signal of 80 type MPU input terminal. Active"L".
During this signal "L", the data bus becomes as output terminal.
<When interface with 68 type MPU>
Enable clock of 68 type MPU input terminal. Active "H".</td></tr>
<tr><td>11</td><td>$\overline{WR}$
(R/W)</td><td>I</td><td><When interface with 80 type MPU>
Connect the 80 type MPU $\overline{WR}$ signal. Active "L".
The data on the data bus input synchronizing the rise edge of this signal.
<When interface with 68 type MPU>
Read/write control signal of 68 type MPU input terminal.
<table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Read</td><td>Write</td></tr></table></td></tr>
<tr><td>42</td><td>C86</td><td>I</td><td>Select the MPU interface type.
<table><tr><td>C86</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>68 Type</td><td>80 Type</td></tr></table></td></tr>
<tr><td>23</td><td>SI</td><td>I</td><td>Serial data input terminal .</td></tr>
<tr><td>22</td><td>SCL</td><td>I</td><td>Serial data clock signal input terminal.
SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.</td></tr>
<tr><td>41</td><td>P/S</td><td>I</td><td>Serial or parallel interface select terminal.
<table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial CLK</td></tr><tr><td>"H"</td><td>$\overline{CS}$</td><td>A0</td><td>D_0~D_7</td><td>$\overline{RD}$、$\overline{WR}$</td><td>—</td></tr><tr><td>"L"</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr></table>*RAM data and status read operation is impossible when select the serial interface.
・ When select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L".
・ When select the serial interface (P/S="L"), $\overline{RD}$ and $\overline{WR}$ must be fix "H" or "L", and D_0~D_7 becomes to the high impedance state.</td></tr>
<tr><td>2
1</td><td>OSC1
OSC2</td><td>I
I/O</td><td>Oscillation resistor connecting terminals.
Connect oscillation resistor Rf between OSC1 and OSC2. OSC2 is output terminal of the internal oscillation circuit.
Rf=1MΩ.</td></tr>
</table>

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<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>44
~
75</td><td>C 31
~
C 0</td><td rowspan="4">O</td><td rowspan="4">LCD drive output terminals.
Segment output terminals : SEG 0 to SEG 133
Common output terminals :C 0 to C 63

• Segment output terminal
Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM.
<table><tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal</th><th>Reverse</th></tr><tr><td rowspan="2">H</td><td>H</td><td>VDD</td><td>V2</td></tr><tr><td>L</td><td>V5</td><td>V3</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VDD</td></tr><tr><td>L</td><td>V3</td><td>V5</td></tr></table>
• Common Output Terminal
Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data.
<table><tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr><tr><td>L</td><td>VDD</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr><tr><td>L</td><td>V4</td></tr></table></td></tr>
<tr><td>76
~
209</td><td>SEG 0
~
SEG 133</td></tr>
<tr><td>210
~
241</td><td>C 32
~
C 63</td></tr>
<tr><td></td><td></td></tr>
<tr><td>242</td><td>COMI</td><td>O</td><td>Icon common output terminal.
Icon common output when Icon Display instruction execution.
<table><tr><th></th><th>Icon Display ON</th><th>Icon Display OFF</th></tr><tr><td>State</td><td>COM 64</td><td>V1 or V4</td></tr></table></td></tr>
</table>

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■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode. the busy flag(BF) is "1", and any instruction except the status read are inhibited .

The busy flag output from D_7 terminal when status read instruction is executed.

If enough cycle time over then t_{cyc} indicated in the bus timing characteristics is kept,no need to check the busy flag and it realized high performance for the MPU.

(1-2) Line Counter

The Line Counter is reset at the FR signal changing and counts up by synchronizing common signal cycle and generate the line address which addressing the read out line of Display Data RAM.

(1-3) Column Address Counter

The column address counter is 8-bit presentable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to $(85)_H$ when the Display Data Read/Write instruction is executed. The count up is stop at $(85)_H$, do not count up non existing address of over than $(86)_H$ by the count lock function. This count lock is released by new column address set.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction ADC, the column address decoder inverse the column address of Display Data RAM correspondence to the Segment Driver.

(1-4) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the data by changing the page, the page address set instruction is required. Page address "8" (D_3 ="H" D_2, D_1 ,D_0 ="L") is Icon RAM area, the data only for the D_0 is valid.

(1-5) Display Data RAM

Display Data RAM consists of 8,710 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM output 134 bit parallel data addressed by the line counter, and these data are set into the Display Data Latch.

This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize rewriting.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.

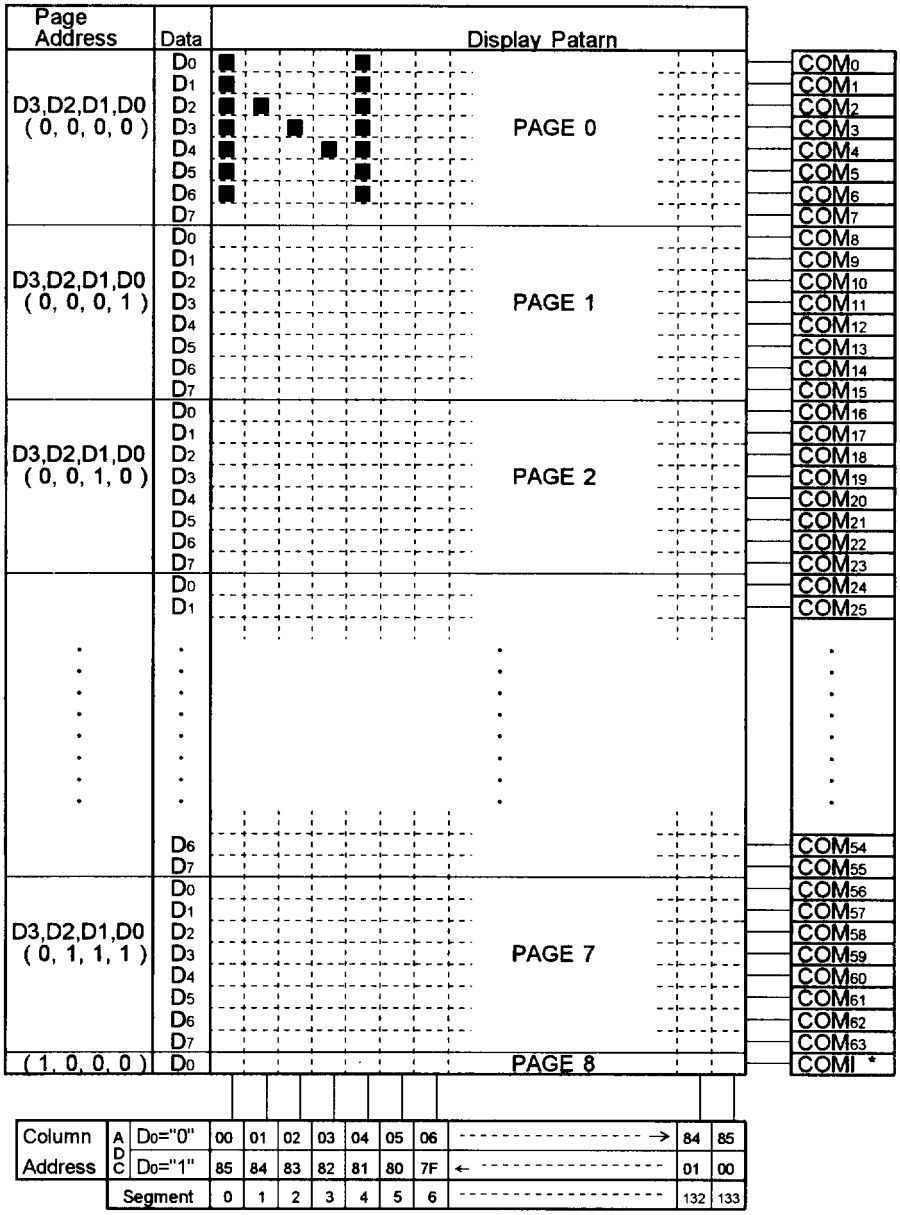


Fig.1 Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/65 Duty Set.)

(1-6) Common and Segment Driver Assignment

The scanning order can be assigned by setting A_3 of the Output Assignment Register as shown Table 1.

The location of Segment Drivers are fixed at any time.

Table 1

Register		COM Output Terminals			
A3	PAD No.	75	44	241	210
	Pin name	C_0	C_{31}	C_{63}	C_{32}
0	→	COM_0 ----------→	COM_{31}	COM_{63} ←----------	COM_{32}
1	→	COM_{63} ←----------	COM_{32}	COM_0 ----------→	COM_{31}

The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COMI is fixed to COM_{64} timing regardless the other Common Driver assignment.

(1-7) Reset Circuits

The NJU6579 performs following initialization when the $\overline{RES}$ input is put on the "L" level.

Initialization

① Display Off
② Normal Display(Non-inverse display)
③ Icon Display Reset
④ ADC Select : Normal (ADC Instruction D_0 ="0")
⑤ Read Modify Write Mode Off
⑥ Internal Power supply(Step up) circuits Off
⑦ Clear the serial interface register
⑧ Set the Column Address Counter to the address $(00)_H$
⑨ Set the Page Address Register to the page "0"
⑩ Select the D_3 of the Output Assignment Register to "0"
⑪ Set the EVR register to $(00)_H$

The $\overline{RES}$ terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface Example". The reset signal require over than 10us $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{RES}$ signal, the normal operation is starting.

In case of the internal power supply(Step up) circuits do not use, the $\overline{RES}$ terminal must be "L" when external power supply turn on. $\overline{RES}$="L" input reset internal register and set above default, but oscillation circuits and output terminals like as D_0 through D_7 are no influence.

No initialization by $\overline{RES}$ when power turns on, will make Hung up condition, therefore please initialize by the $\overline{RES}$ when power turns on. By the reset Instruction performs only ⑧ through ⑪ mentioned in above.

The noise into the $\overline{RES}$ terminal should be cared when of the application design to avoid the error function.

(1-8) LCD Driving

(a) LCD Driving Circuits

NJU6579 incorporates 199 LCD Drivers like as 134 Segment drivers, 64 Common drivers and 1 Icon common driver. 64 Common drivers incorporate the shift register which scanning the common display signal. The combination among the Display data, COM scan signal and FR signal define the LCD driving output voltage. The output wave form is mentioned in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 134-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver. The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits

The clock for Line Counter and latch signal for the Latch Circuits are generated from display clock(CL). The line address is renewed by synchronizing with display clock and 134 bits display data are latched into display latch circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR has a function to generate the two frame alternative driving method waveform for the LCD panel.

5

(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

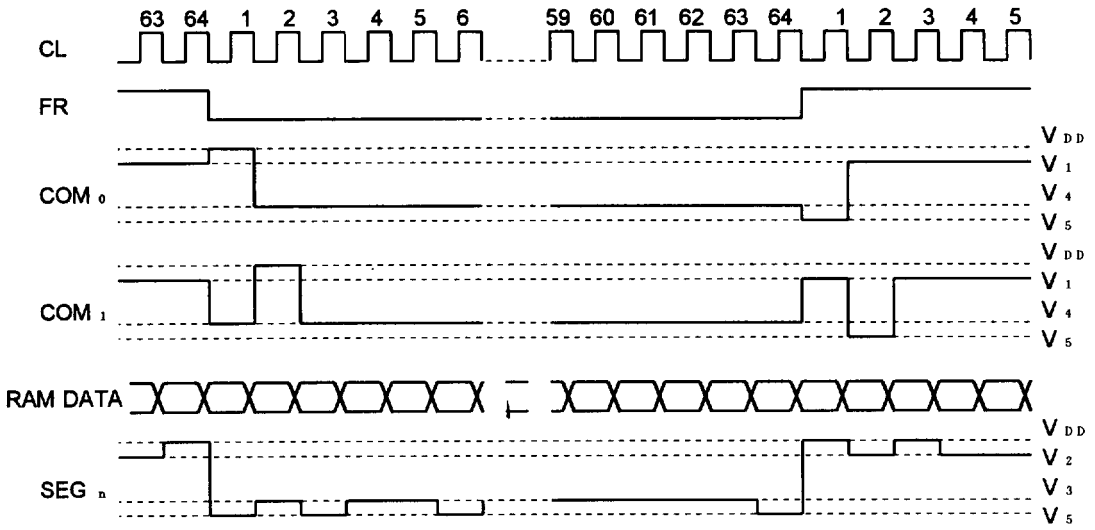


Fig. 2 Waveform of Display Timing

(f) Oscillation Circuits

The Oscillation Circuits, which requires external oscillation resistor Rf, is a low power CR oscillator and it is used as display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuits output frequency is divided by 4 which is used as display clock CL.

(g) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Doubler,Tripler or Quadrupler) Circuits, Regulation Circuits, and Voltage Follower. Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the large size LCD panel application. If the contrast is no good in those application, please use external power supply supplied more high current.

The suitable external ports (capasitors for V1 to V5 terminals and for step up circuit, resistors for V5 operational amplifier) depend on LCD size. Therefore, a test on actual module is practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, voltage follower circuits are off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD supply from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$,and VR are open. The status of internal power supply can select by T_1 and T_2 terminal. The external power supply can be used together with some of internal power supply function.

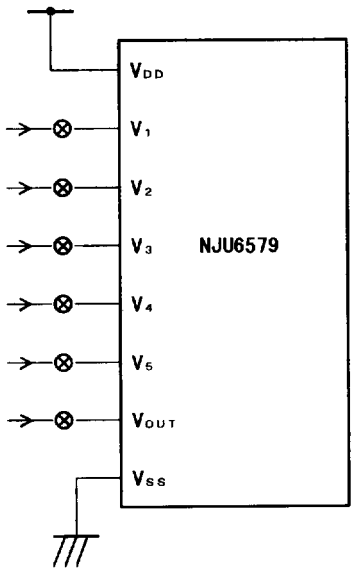
Table 3. (*:Don't Care)

T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2- C3+,C3-	VR Term.
L	*	○	○	○	-		
H	L	×	○	○	V_{OUT}	OPEN	
H	H	×	×	○	V_5, V_{OUT}	OPEN	OPEN

When (T_1, T_2)=(H, L), the terminal for step up circuits of $C1^+$,$C1^-$ $C2^+$,$C2^-$, $C3^+$, $C3^-$ are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T_1, T_2)=(H, H), terminals for step up circuits and VR are open, and supply the LCD driving voltage from outside due to the Step up circuits and Voltage adjust circuits are stop its operation.

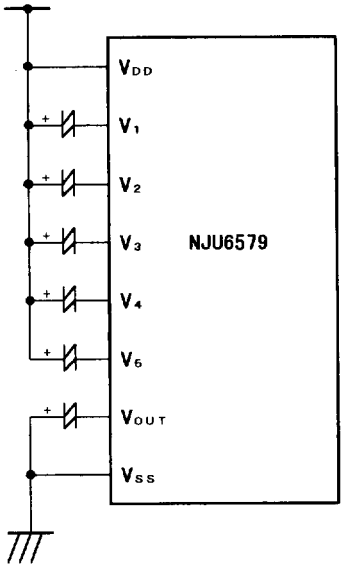
○ Examples for the internal Power Supply circuit application

(1)None of the internal power supply function.



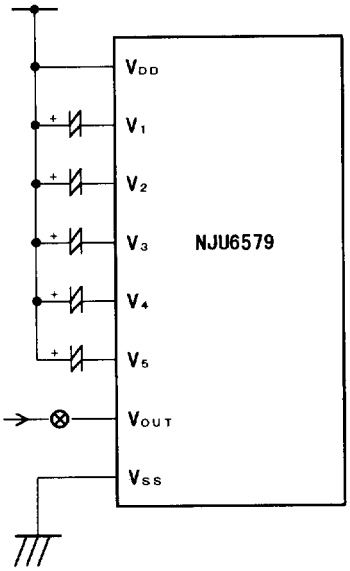
(2) All of the internal power supply functions.
(Step up, Voltage Adj., Buffer(V/F))

(T1, T2) = (L, *) *: Don't care.



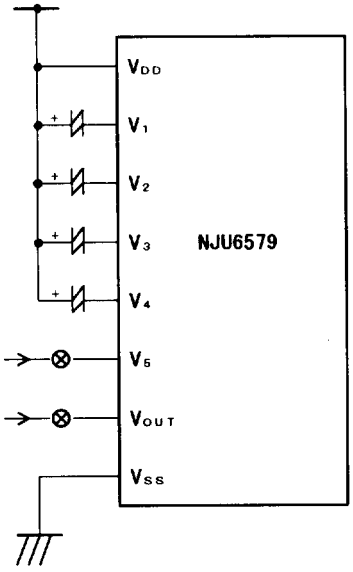
(3)Some of the internal power supply functions.
(Voltage Adjust., Buffer(V/F))

(T1,T2) = (H,L)



(4)Some of the internal power supply functions.
(Buffer(V/F))

(T1,T2) = (H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6579 distinguish the signal on the data bus by combination of A0,$\overline{RD}$ and $\overline{WR}$. Normally, the busy check is not required as the NJU6579 is operating so first because of the decode of the instruction and execution are performs only depend on the internal timing which not depend on the external clock. In case of serial interface, the data input as MSB first serially.

The Table. 4 shows the instruction codes of the NJU6579.

Table 4. Instruction Code

Instruction		Code												Description
		A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1		LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	Page Address					Set the page of DD RAM to the Page Add. Register
(3)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.					Set the Higher order 4 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.					Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status				0	0	0	0		Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data									Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data									Read the Data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1		Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0 1		Inverse the On and Off Display 0:Normal 1:Inverse
(10)	Whole Display On /Normal Display	0	1	0	1	0	1	0	0	1	0	0 1		Whole Display Turns On 0:Normal 1:Whole Disp. On
(11)	Icon Display	0	1	0	1	0	1	0	1	0	1	0 1		Set the Duty Ratio 0:1/64 Duty 1:1/65 Duty
(12)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0		Increment the Column Add. Register when writing but no-change when reading
(13)	End	0	1	0	1	1	1	0	1	1	1	0		Release from the Read Modify Write Mode
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0		Initialize the internal Circuits
(15)	Output Assignment Register Set	0	1	0	1	1	0	0	A_3	*	*	*		Set the scanning order of common drivers to the Register
(16)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0 1		0:Int. Power Supply Off 1:Int. Power Supply On
(17)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1		Set LCD Driving Voltage after the internal(external) power supply is turned on
(18)	EVR Register Set	0	1	0	1	0	0	0	Setting Data					Set the V_5 output level to the EVR register
(19)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1		Set the Power save Mode

5

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 8 is a Icon display data area which available only for the D_0.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	1	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

5

(c) Column Address

When MPU access the Display Data RAM, page address set(refer(b) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting.

After writing 1page data ,page address setting is required due to page address doesn't increase automatically.

The increment of the column address is stopped by the address of (86)$_H$ automatically, or the page address is no change even if the column address increase to (86)$_H$ and stop. In this time the page address is no change.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
Higher Order	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower Order	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				.				.
				.				.
1	0	0	0	0	1	0	1	85

(d) Status Read

This instruction read out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.
0 :Counterclockwise Output(Inverse) Column Address 133-n ←→ Segment Driver n
1 :Clockwise Output (Normal) Column Address n ←→ Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On"
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initialization period by $\overline{RES}$ signal or reset instruction.
0 : —
1 : Initialization Period

(e) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	WRITE DATA							

(f) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page address. The column address increase "1" automatically when reading, therefore, the MPU can read the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read is required after column address set as explain in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data can not be readout.

A0	$\overline{RD}$	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	READ DATA							

(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	0	0	D

D 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Data RAM is no changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"
1: Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction executes the all pixel terns on regardless the contents of the Display Data RAM. In this time, the contents of Display Data RAM is no change and is kept. This instruction takes over precedence over the "Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$ ($\overline{WR}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	0	D

D 0: Normal Display
1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the power save mode(refer to the (s) Power Save) .

(j) Icon Display

This instruction set the 1/65 duty for the Icon Display. The COMI terminal operate as COM $_{64}$ and output the icon display data stored in D $_0$ of Display Data RAM page 8 (refer to the Fig. 1).

A0	$\overline{RD}$	R/$\overline{W}$	D $_7$						D $_0$
0	1	0	1	0	1	0	1	0	1	D

D 0: 1/64 Duty
1: 1/65 Duty

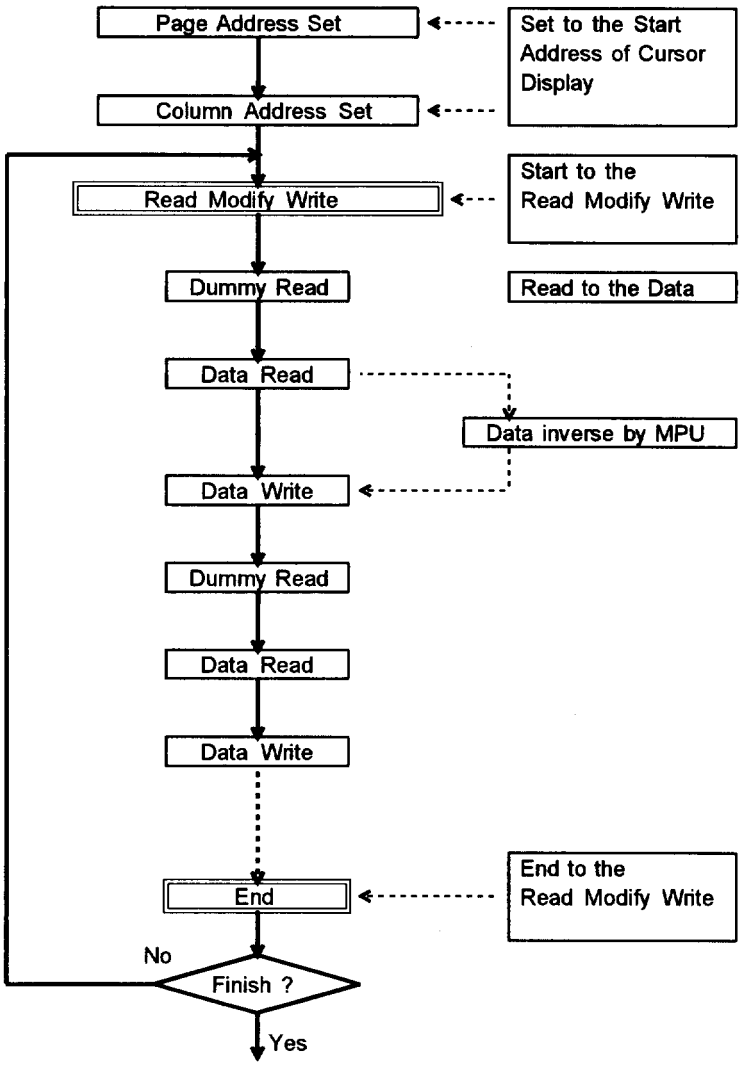
(k) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the Read Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction is executed, but the address is no change when the Display Data Read Instruction is executed. This status is continued during End instruction execution. When the End instruction is entered the column address back to the address where the Read Modify Write instruction entering. By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

A0	$\overline{RD}$	R/$\overline{W}$	D $_7$						D $_0$
0	1	0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

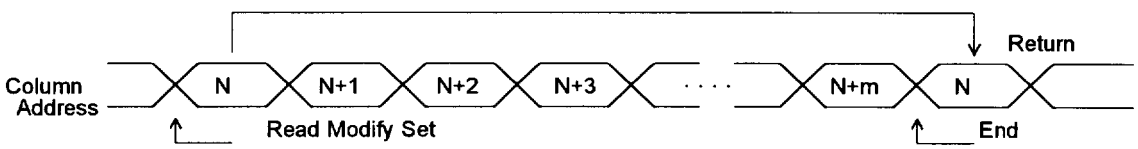
(l) Sequence of inverse display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7						D_0
0	1	0	1	1	1	0	1	1	1	0



(n) Reset

This instruction executes the following initialization.

Initialization

① Set the Column Address Counter to the Address (00)$_H$.
② Set the Page Address Register to the page "0" .
③ Select the D3 of the Output Assignment Register to "0".
④ Set the EVR Register to (00)$_H$.

In this time, there are no influence to the Display Data RAM.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal must be required for the initialization when the power terns on. Substitution of Reset Instruction for the reset signal input to the $\overline{RES}$ terminal is not allowed.

(o) Output Assignment Register

This instruction sets the common driver scanning order .

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	0	0	A3	*	*	*

(*:Don't Care)

A3: Set the scanning order .(Refer to 1-6)

(p) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is required.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q)LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 to V4 and output LCD driving waveform through the COM/SEG terminals.

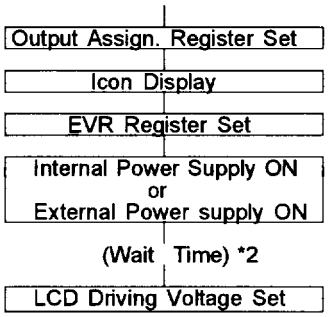
A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	1	0	1	1	0	1

NJU6579 contains operational amplifiers for LCD bias voltage V1 to V4. These amplifiers current are reduced in order to realize low power consumption. Because of this reduction, LCD driving voltage V1 to V4 might be unstable just after the internal power supply is turned on.
LCD Driving Voltage Set instruction is prepared for this unstableness.

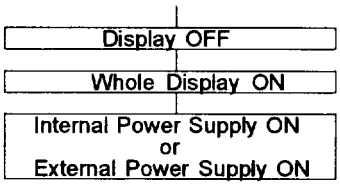
● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is tuned on/of.
When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence mentioned in (s) is required.

Turn ON sequence

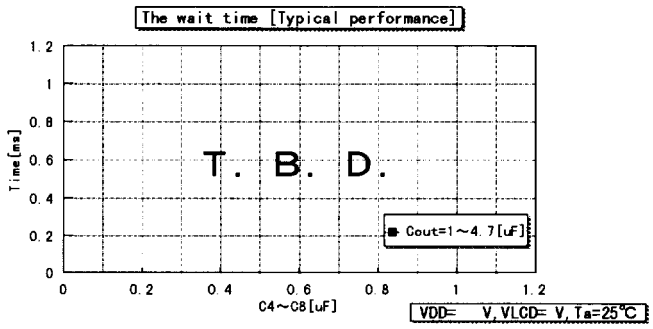


Turn OFF sequence



*1 This instruction is required in both cases of the internal and external power supply.
Until "LCD driving voltage Set" execution, NJU6579 operating current is higher than usual state and all COM/ SEG terminals output V_{DD} level continuously except LCD driving waveform.

*2 The wait time depends on the C_4, C_5, C_6, C_7, C_8 and C_{OUT} capasitors((4) (d)Fig.4), V_{DD} and V_{LCD} voltage.
Therefore a test on actual module should be practiced. Refer to the following graph.



(r) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this instruction execute, the internal Electrical Variable Resistor(EVR) to change the V_5 output voltage, generate one voltage from 16 voltage state. The range of V_5 output level can be adjusted by the external resistance. For more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	0	0	A3	A2	A1	A0

A3	A2	A1	A0	V_{LCD}
0	0	0	0	Low
	:			:
	:			:
1	1	1	1	High

$V_{LCD} = V_{DD} - V_5$

When EVR doesn't use, set the EVR register to (0,0,0,0).

(s) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits put on the power save mode and the operating current is reduced as same as stand by current.
The internal status in the Power Save Mode is as follows;

① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
③ Stop the external clock input. Then the terminal OSC_2 becomes floating status.
④ Keeping the display data and operating mode as before the power save mode.
⑤ All of LCD driving bias voltage fixed to the V_{DD} level.

The power save and its release should be performed according to the following sequences.

Power Save Sequence

Display OFF
↓
Whole Display ON

Power Save Release Sequence

Normal Display
↓
Display ON
↓
(Wait Time)
↓
LCD Driving Voltage Set

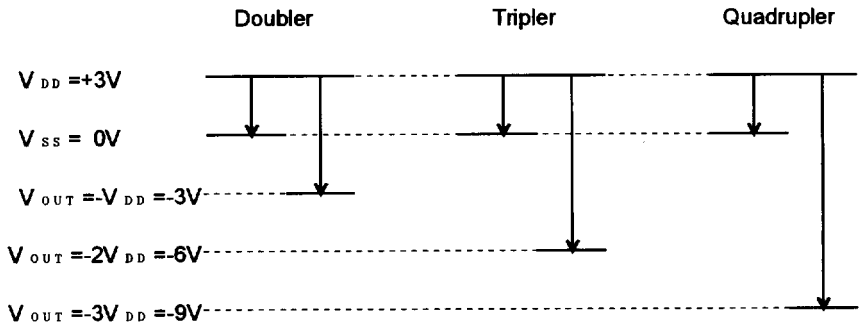
*1 Power save mode requires dual-instruction. After the second instruction" whole Display ON", the power save mode starts.
*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.
*3 Until "LCD driving voltage set" execution, NJU6579 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.
*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.
*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

(4) Internal Power Supply

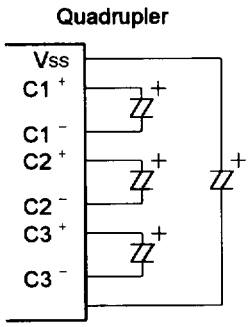
(a) Voltage quadrupler

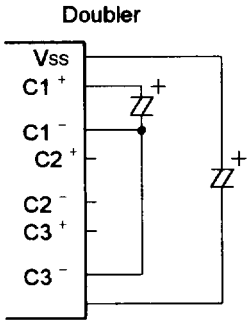
Four times negative voltage(V_{DD} common) of the voltage V_{DD}-V_{SS} is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, $C3^+$ and $C3^-$, V_{SS} and V_{OUT}.

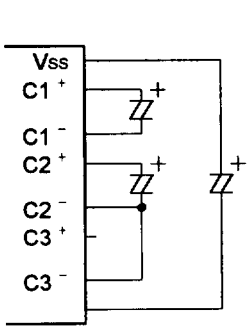
Step up circuits like as Voltage Doubler, Tripler and Quadrupler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage quadrupler operation, the operation voltage V_{DD} should be less than 3.3V.

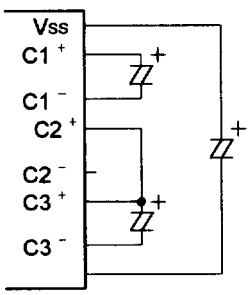


· Examples for connection with the capatitors









(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage can calculated by the following formula.

$$V_{LCD} = V_{DD} - V_5 = (1+Rb/Ra) \cdot V_{REG} \cdots\cdots ①$$

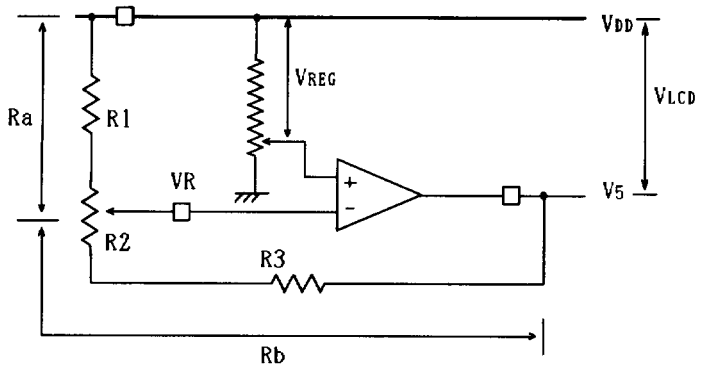


Fig. 3

V_{REG} is a standard voltage produced from internal bleeder resistance in Fig.3. V_{REG} is possible to be fine-adjusted by EVR functions mentioned in (c).

In order to adjust the output voltage from V_5, connect the variable resistance among VR, V_{DD} and V_5 as shown in Fig. 3. When fine tuning for V_5 is needed, combine with the fixed resistance of R1, R3 and variable resistance of R2 is recommended as shown in Fig. 3.

[Design example for R1, R2 and R3; V_{DD} =3V / reference]

- R1+R2+R3=5M Ω (Determined by the current flown between V_{DD} -V_5)
- Variable voltage range by the R2. -7V ~ -9V (V_{LCD} =V_{DD} -V_5 → 10V ~ 12V)
  (Determined by the LCD electrical characteristics)
- R1, R2 and R3 are calculated by above conditions and the formula of ① to mentioned below;
  R1=1.25M Ω
  R2=0.25M Ω
  R3=3.5M Ω

* If the power supply voltage between V_{DD} and V_{SS} changes, V5 changes too. Therefore the power supply voltage should be stabilized in order not to change V5.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_5 which controls LCD display contrast can adjust by the instruction. The EVR function is executed to set the 4 bits data into the EVR resistor and determine the one output voltage status out of 16 prefixed voltage status as the following table .

When execute the EVR function, set the T_1 and T_2 except the "H, H" and execute the Internal Power Supply On instruction.

EVR register		V_{REG}[V]	V_{LCD}
$(00)_H$	(0, 0, 0, 0)	$(135/150)\cdot(V_{DD}-V_{SS})$	Low
$(01)_H$	(0, 0, 0, 1)	$(136/150)\cdot(V_{DD}-V_{SS})$	
$(02)_H$	(0, 0, 1, 0)	$(137/150)\cdot(V_{DD}-V_{SS})$	
$(0D)_H$	(1, 1, 0, 1)	$(148/150)\cdot(V_{DD}-V_{SS})$	
$(0E)_H$	(1, 1, 1, 0)	$(149/150)\cdot(V_{DD}-V_{SS})$	
$(0F)_H$	(1, 1, 1, 1)	$(150/150)\cdot(V_{DD}-V_{SS})$	High

● Adjustable range of the LCD driving voltage when EVR function using

The adjustable range is decided by the resistors Ra,Rb and $V_{DD}-V_{SS}$ voltage.

[Design example for the adjustable range / reference]

- Condition V_{DD}=3.0V, V_{SS}=0V
  Ra=1MΩ , Rb=3MΩ (Ra:Rb=1:3)

The adjustable range and the step voltage are calculated at this condition as follows.

In case of $(00)_H$ in the EVR register,

$$V_{LCD} = ((Ra+Rb)/Ra)\cdot V_{REG}$$
$$= (4/1)\cdot[(135/150)\cdot 3.0]$$
$$= 10.8V$$

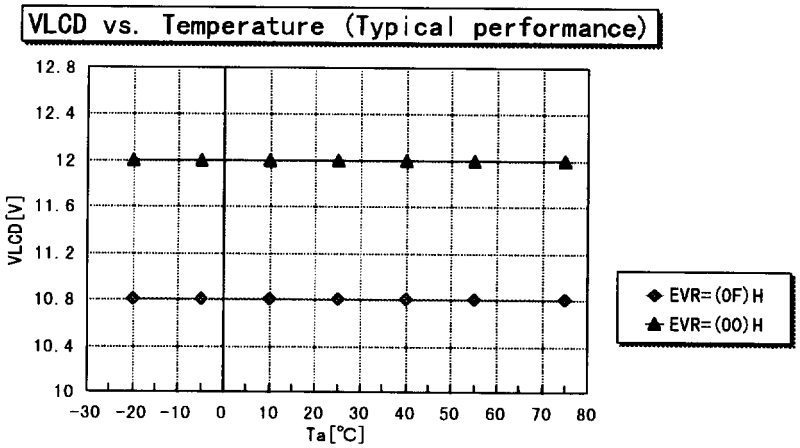
In case of $(0F)_H$ in the EVR register,

$$V_{LCD} = ((Ra+Rb)/Ra)\cdot V_{REG}$$
$$= (4/1)\cdot[(150/150)\cdot 3.0]$$
$$= 12.0V$$

	Min. $(00)_H$	Max. $(0F)_H$	
Adjustable Range	10.8 <----------	----------> 12.0	[V]
Step Voltage	80		[mV]

*) The V_{LDC} operating temperature. Please refer to the following graphs.

(condition) VDD = 3V
Ra=1M Ω , Rb=3M Ω (Ra:Rb = 1:3)
Voltage Quadrupler



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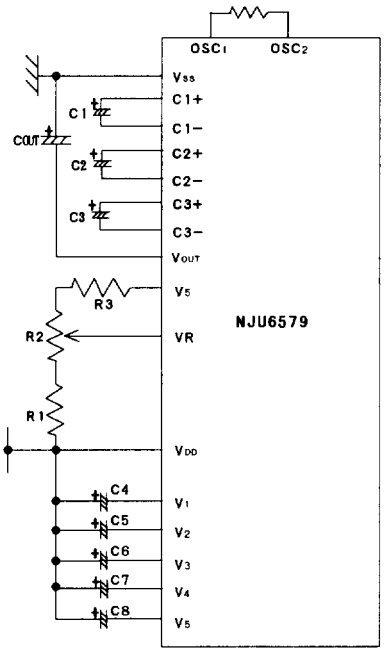
(d) LCD Driving Voltage Generation Circuits

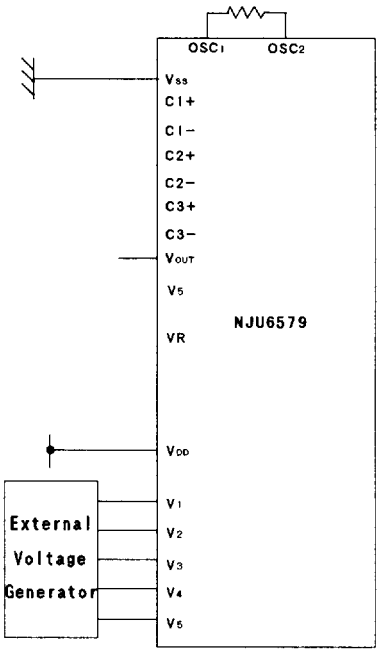
The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V_5 voltage by the bleeder resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 4, Five capacitors are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitors C3, C4, C5, C6, C7 and C8 determine by combine with the actual LCD panel.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

VLCD = VDD-V5 ≒10 ~12V

Item	Value
C_{OUT}	4.7~10μF
C1,C2C3	4.7~10μF
C4 to C8	0.1~0.47μF
R1	1.25MΩ
R2	0.25MΩ
R3	3.5MΩ

Fig. 4

*1 To avoid the malfunction, use a short wiring for the feed back resistance Rf of oscillation circuits.

*2 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.

*3 Following connection of VOUT is required when external power supply using.

When $V_{SS} > V_5$ -- $V_{OUT} = V_5$

When $V_{SS} \leqq V_5$ -- $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6579 can interface by using both of 8 bit bilateral data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined the P/S terminal connected to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out is impossible.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	-	-	$D_0 \sim D_7$
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6579 can interface both of 68 or 80 type MPU directly by setting the parallel interface (P/S="H") and "H" or "L" of the C86 terminal as shown in table 6.

Table 6

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$
H	68 type MPU	$\overline{CS}$	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6579 discriminate the signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5– 4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to CS="L"and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal is MSB first like as the order of D_7,D_6,D_5,D_4,D_3,D_2,D_1,D_0 and the data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or $\overline{CS}$ terminal becomes "H" in spite of the data less then 8 bits, NJU6579 recognizes wrong data as a instruction data. Therefore 8bits data is required for the input data. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface .

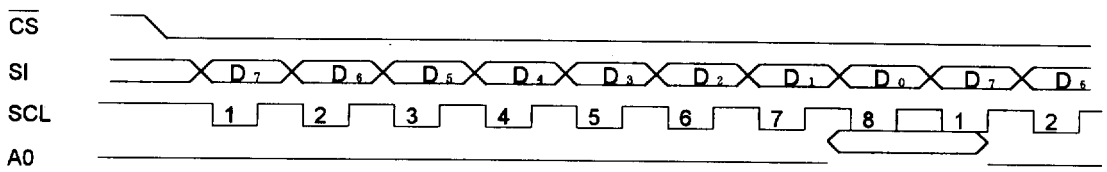


Fig. 5

(5– 5) Access to the Display Data RAM and Internal Register.

The NJU6579 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU read out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at next data read cycle. And when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6579 is available because of the limitation of access time of NJU6579 locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP operation cycle which equivalent to the waiting operation is useful.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

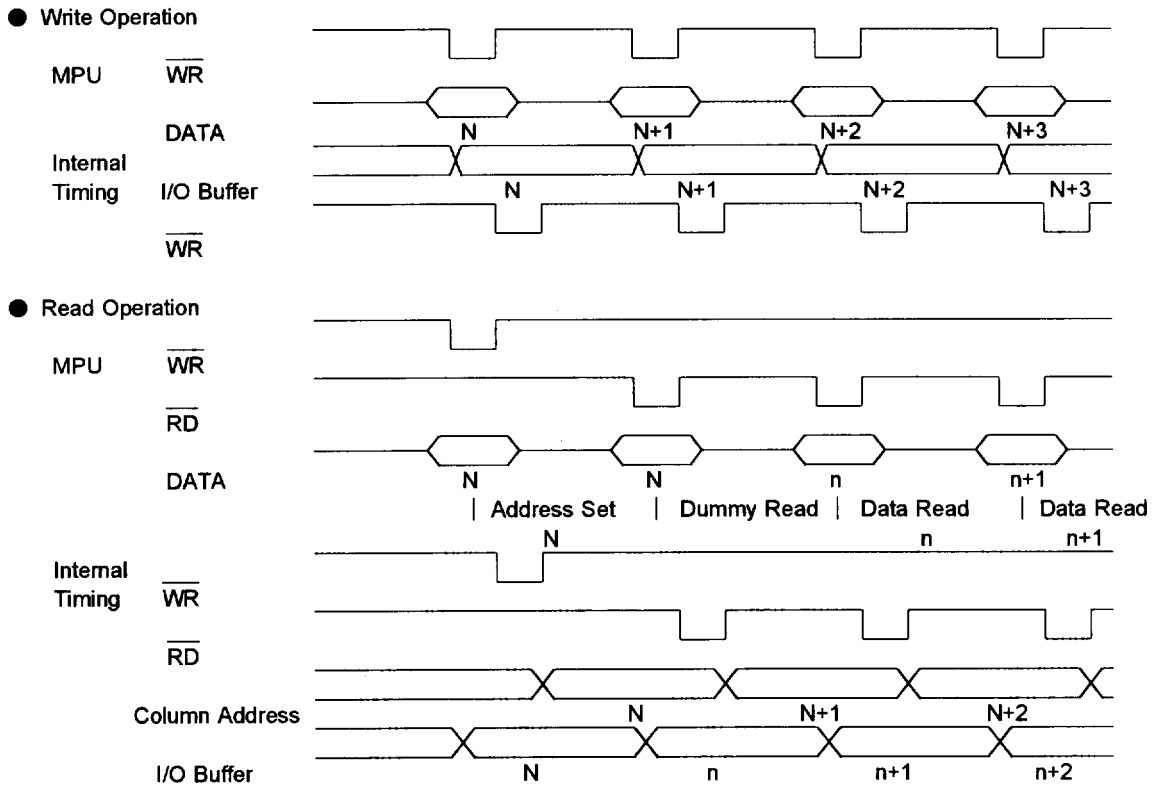


Fig.6

(5-6) Chip Select

CS is Chip Select terminal. The Chip Select is executed by the setting of $\overline{CS}$="L". Only the select mode, the interface with MPU is available. In the non select period, the $D_0 \sim D_7$ are high impedance and A0, RD, WR, SI and SCL input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of CS.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	− 0.3 ～ + 7.0 − 0.3 ～ + 4.5 (used Tripler) − 0.3 ～ + 3.3 (used Quadrupler)	V
Supply Voltage (2)	V_5	V_{DD}−13.5 ～ V_{DD}+0.3	V
Supply Voltage (3)	V_1～V_4	V_5 ～ V_{DD}+0.3	V
Input Voltage	V_{IN}	− 0.3 ～ V_{DD}+0.3	V
Operating Temperature	Topr	− 30 ～ + 80	°C
Storage Temperature	Tstg	− 55 ～ + 125 (Chip) − 55 ～ + 100 (TCP)	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1) (V_{DD}=3V±10%, V_{SS}=0V, Ta=−20～+75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage (1)	Recommend	V_{DD}			2.7	3.0	3.3	V	
	Available				2.4		5.5		5
Operating Voltage (2)	Recommend	V_5			V_{DD}−13.5		V_{DD}−3.5	V	
	Available				V_{DD}−13.5				
	Available	V_1, V_2	V_{LCD}=V_{DD}−V_5		V_{DD}−0.6xV_{LCD}		V_{DD}		
	Available	V_3, V_4			V_5		V_{DD}−0.4xV_{LCD}		
Input Voltage	High Level	V_{IHC}	DO, D1...D7, A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$, $\overline{WR}$, C86, SI, SCL, P/S Terminals		0.8xV_{DD}		V_{DD}	V	
	Low Level	V_{ILC}			V_{SS}		0.2xV_{DD}		
Output Voltage	High Level	V_{OHC}	DO, D1...D7, Terminals	I_O=−0.5mA	0.8xV_{DD}		V_{DD}	V	
	Low Level	V_{OLC}		I_O= 0.5mA	V_{SS}		0.2xV_{DD}		
Input Leakage Current		I_{LI}	All input terminals		−1.0		1.0	uA	
		I_{LO}	All I/O term. (DO...D7)		−3.0		3.0		6
Driver On-resistance		R_{ON1}	Ta=25°C ext. power supply	V_{LCD}=13.5V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD}=10.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	during power save Mode			T.B.D.	T.B.D.	uA	8

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■ ELECTRICAL CHARACTERISTICS (2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Current	I_{DD1}	Display	V_{LCD}=10V		T.B.D.	T.B.D.	uA	8
	I_{DD2}	Accessing fcyc=200kHz			T.B.D.	T.B.D.	uA	9
Input Terminal Capacitance	C_{IN}	A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$, $\overline{WR}$, C86, SI, SCL, P/$\overline{S}$, T1, T2, D_0~D_7 Ta=25°C			10		pF	
Oscillation Frequency	fosc	Rf=1MΩ, V_{DD}=2.7V, Ta=25°C		T.B.D.	16	T.B.D.	kHz	

Voltage Quadrupler	Input Voltage	V_{DD1}	V_{DD}–V_{SS}		2.4		5.5	V	
		V_{DD2}	V_{DD}–V_{SS}, used Quadrupler		2.4		3.3		10
	Output Volt.	V_{OUT}	V_{SS}–V_{LCD}, used Quadrupler		-9.9			V	
	Step-up output on-resistance	R_{STEP}	used Quadrupler, C_1~C_3, C_{OUT}=4.7μF V_{DD}=3.0V		T.B.D.	T.B.D.	T.B.D.	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Quadrupler Circuit "OFF"		V_{DD}–13.5		V_{DD}–5.0	V	11
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"		V_{DD}–13.5		V_{DD}–5.0	V	
	Operating Current	I_{OUT1}	V_{DD}=3.3V, V_{LCD}=10V			T.B.D.	T.B.D.	uA	12
		I_{OUT2}	COM/SEG Term Open, No Access Display check. pattern			T.B.D.	T.B.D.		
		I_{OUT3}				T.B.D.	T.B.D.		
	Voltage Reg.	V_{REG}	V_{DD}=3.0V, Ta=25°C			T.B.D.	T.B.D.	%	13

Note 5) NJU6579 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D_0 to D_7 terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set".

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 10) Supply voltage (V_{DD}) range for internal Voltage Quadrupler operation.

Note 11) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

Note 12) Each operating current of voltage supply circuits block is specified under below table conditions.

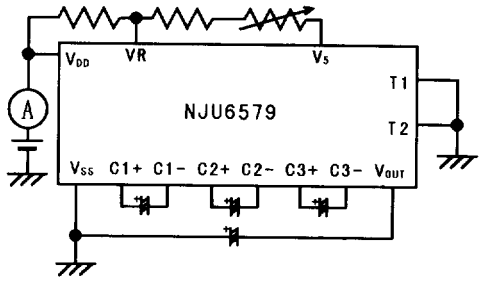
SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T_1	T_2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use (V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use (V_{OUT}, V_5)

* = Don't Care

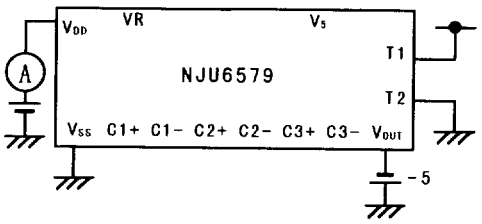
Note 13) Apply to the precision of V_{LCD} voltage on each EVR steps.

■ MEASUREMENT BLOCK DIAGRAM

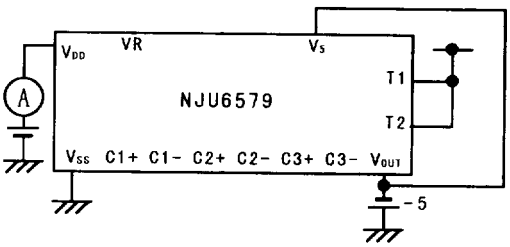
: I_{OUT1}



: I_{OUT2}



: I_{OUT3}



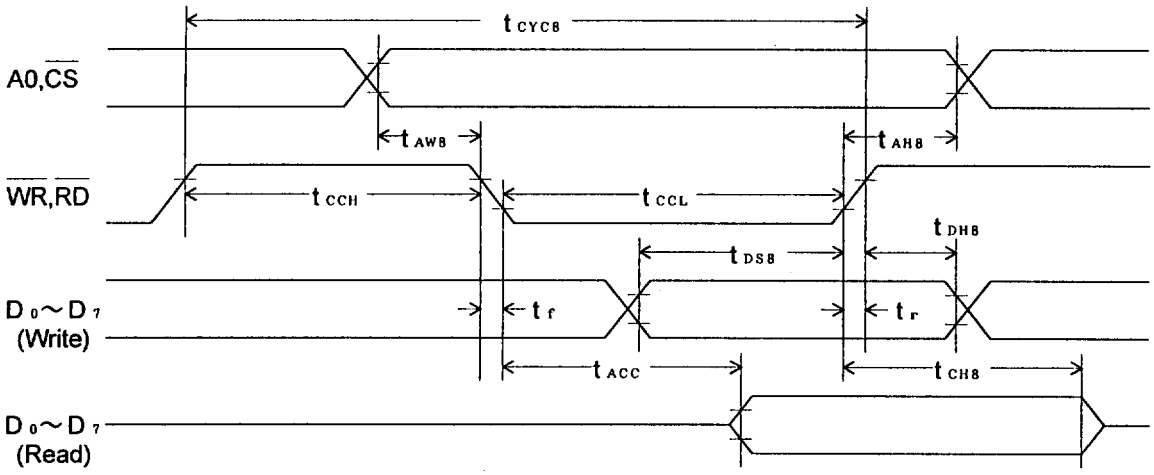
■ ELECTRICAL CHARACTERISTICS (3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	15

Note 14) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 15) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

■ BUS TIMING CHARACTERISTICS

・ Read/Write operation sequence (80 Type MPU)



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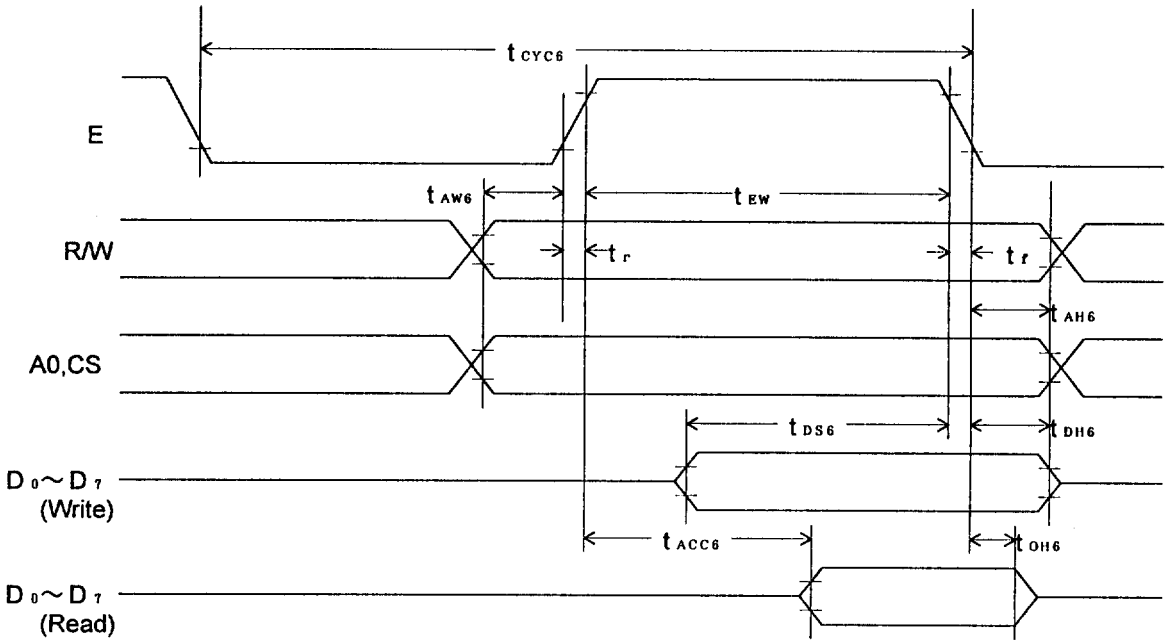
(V_{DD}=3.0V±10%, Ta=-20～75°C)

PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, $\overline{CS}$ Terminals	t_{AH8}	25			ns
Address Set Up Time			t_{AW8}	25			
System Cycle Time		$\overline{WR}$, $\overline{RD}$ Terminals	t_{CYC8}	450			
Control Pulse Width	$\overline{WR}$, "L"		t_{CCL} (W)	50			
	$\overline{RD}$, "L"		t_{CCL} (R)	200			
	"H"		t_{CCH}	220			
Data Set Up Time		D_0～D_7 Terminals	t_{DS8}	120			
Data Hold Time			t_{DH8}	35			
$\overline{RD}$ Access Time			t_{ACC8}		140	CL=100pF	
Output Disable Time			t_{CH8}	0	35		
Rise Time, Fall Time		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, D_0～D_7 Terminals	t_r, t_f		15		

Note 16) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 17) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

・ Read/Write operation sequence (68 Type MPU)

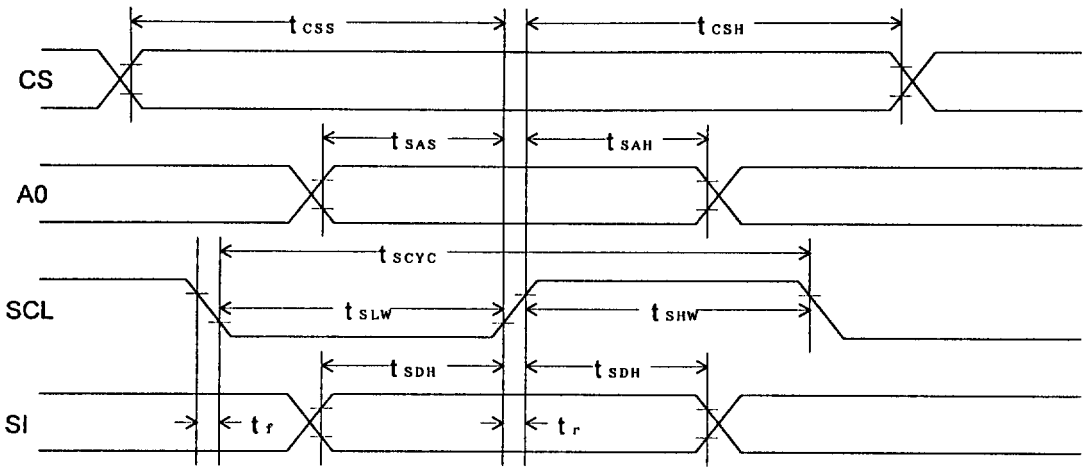


(VDD=3.0V±10%, Ta=-20～75°C)

PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, $\overline{CS}$, R/W Terminals	t_{AH6}	25			ns
Address Set Up Time			t_{AW6}	25			
System Cycle Time			t_{CYC6}	450			
Enable Pulse Width	Read	E Terminal	t_{EW}	200			
	Write			50			
Data Set Up Time		D0～D7 Terminals	t_{DS6}	120			
Data Hold Time			t_{DH6}	40			
Access Time			t_{ACC6}		140	CL=100pF	
Output Disable Time			t_{CH6}	0	45		
Rise Time, Fall Time		A0, $\overline{CS}$, R/W, E, D0～D7 Terminals	t_r, t_f		15		

Note 18) t_{CYC6} indicates the E signal cycle during the $\overline{CS}$ activation period. The System Cycle Time must be required after CS becomes active.
Note 19) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 20) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

・ Write operation sequence (Serial Interface)



(V_{DD}=3.0V±10%, Ta=−20～75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	1000			ns
SCL "H" pulse width		t_{SHW}	300			
SCL "L" pulse width		t_{SLW}	300			
Address Set Up Time	A0 Terminal	t_{SAS}	250			
Address Hold Time		t_{SAH}	400			
Data Set Up Time	SI Terminal	t_{SDS}	250			
Data hold Time		t_{SDH}	100			
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	t_{CSS}	60			
		t_{CSH}	800			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	t_r, t_f		15		

Note 21) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 22) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

■ LCD DRIVING WAVEFORM

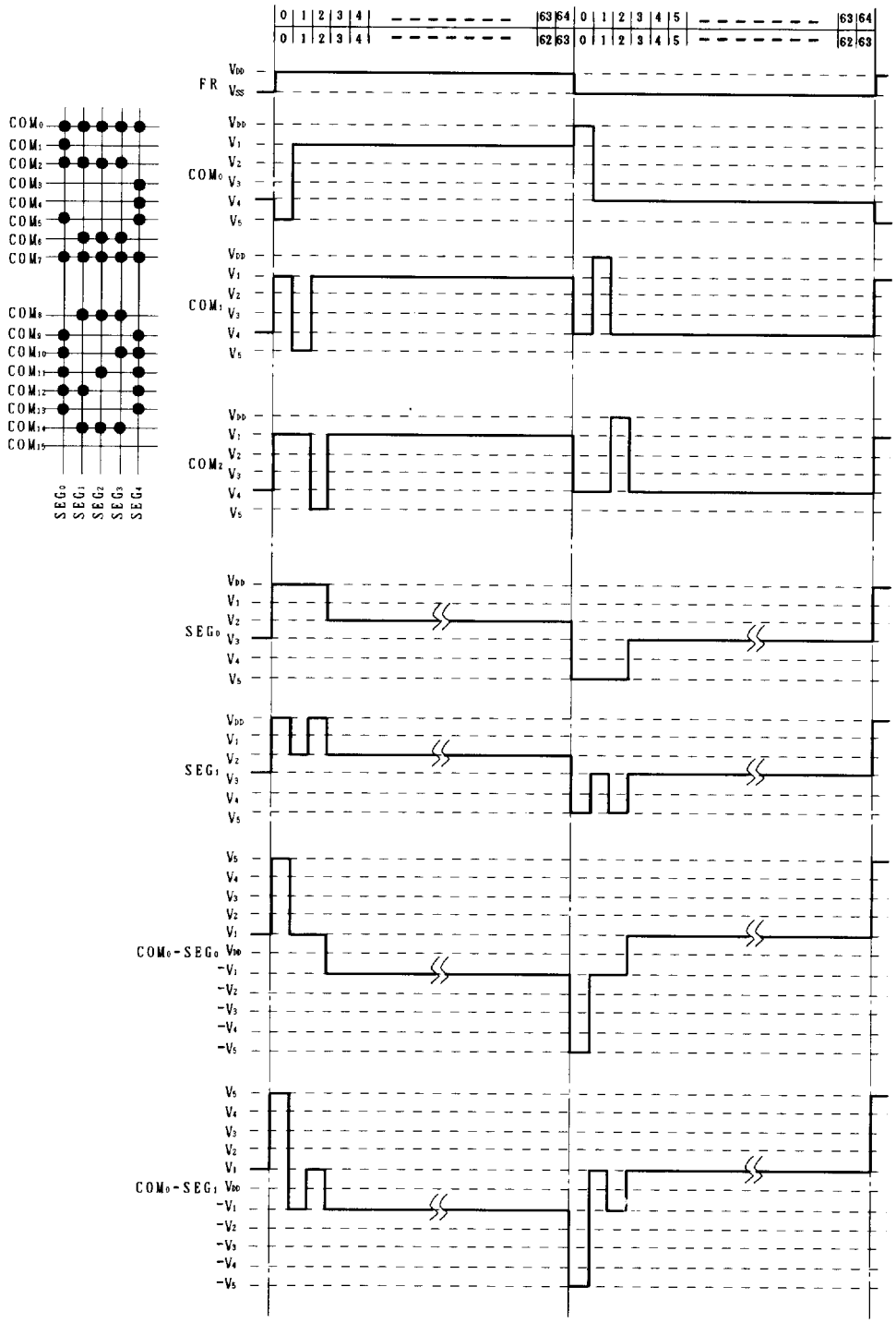


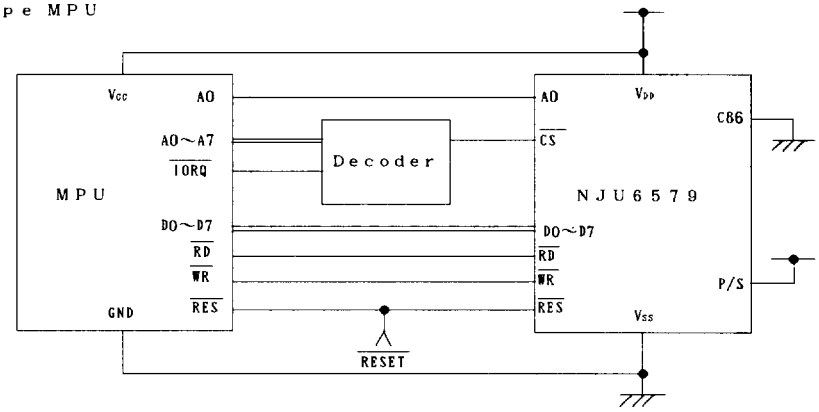
Fig. 7

■ APPLICATION CIRCUIT

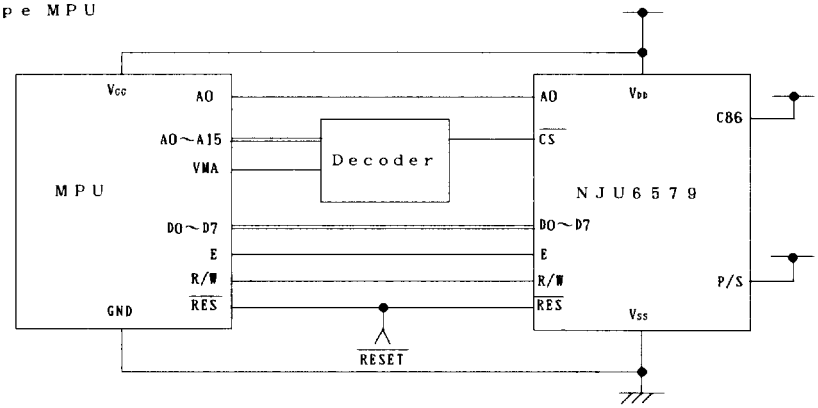
·Microprocessor Interface Example

The NJU6579 can interface with both of 80 type and 68 type MPU by the serial format directly. Therefore minimum wiring for the MPU interface is available.

● 8 0 Type MPU



● 6 8 Type MPU



● S e r i a l I n t e r f a c e