BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6577** is a bit map LCD driver to display graphics or characters.

It contains 4,240 bits display data RAM, microprocessor interface circuits, instruction decoder, 80-segment and 53-common (1 out of 53-driver is prepared for icon display) drivers.

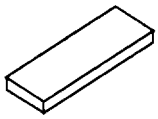
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel mode.

53 x 80 dots graphics or 5-character 3-line by 16 x 16 dot character with icon are displayed by **NJU6577** itself.

The wide operating voltage like as 2.4V t o 5.5V and low operating current are useful to apply small sized battery operated items.

The build-in Electrical Variable Resistance is very precision, furthermore the rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE



NJU6577C

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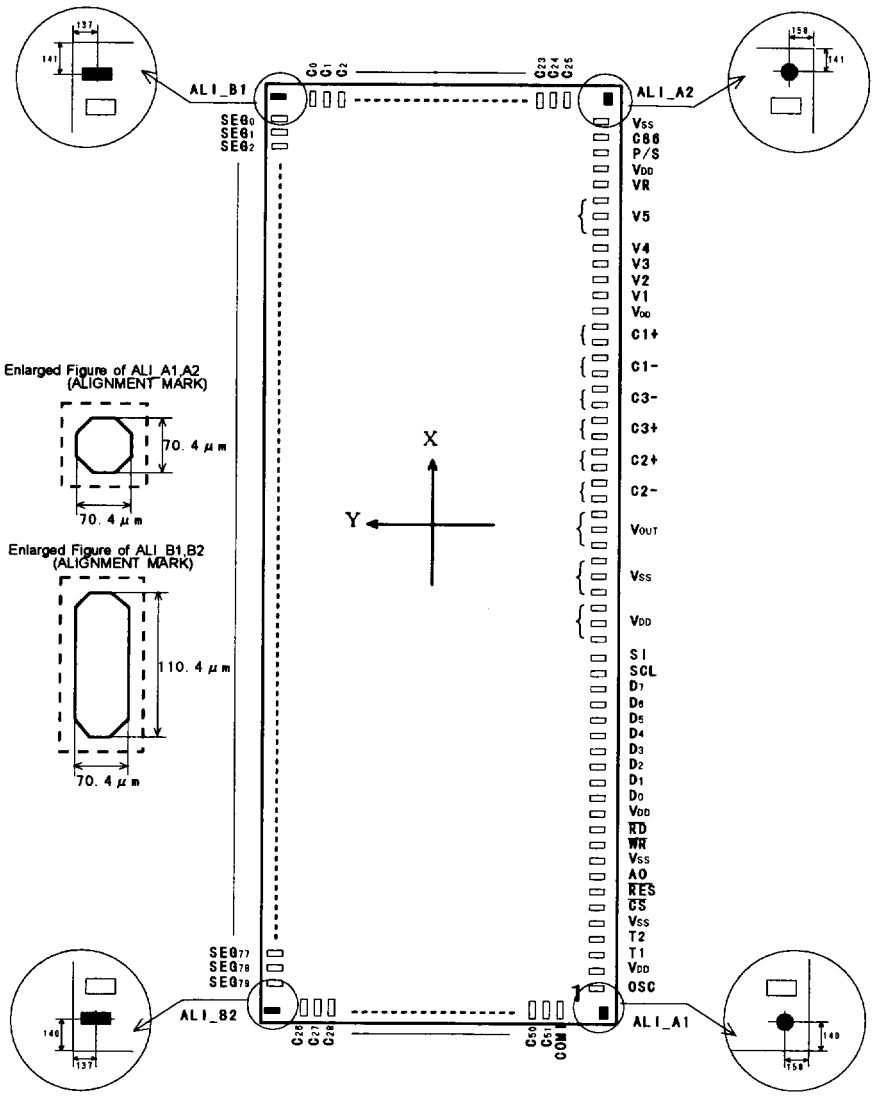
■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 4,240 bits
- 133 LCD Drivers - 53- common and 80-segment
- Direct Interface with both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/52 or 1/53 Duty
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Display Starting Line Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V ~ 5.5V
- LCD Driving Voltage --- 6.0V ~ 13.5V
- Package Outline --- Chip / Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip	Center	X=0um, Y=0um
Chip	Size	X=8.46mm, Y=2.88mm
Chip	Thickness	400um ± 30um
Bump	Size	60umx 110um
Bump	Height	25um TYP.
Bump	Material	Au

■ : Four PADs illustrated with this mark are the alignment marks for COG.

■ PAD COORDINATES

Chip Size 8.46 mm x2.88 mm(Chip Center X=0um,Y=0um)

No.	Terminal	X (μm)	Y= μm
1	OSC	-3903	-1277
2	V_{DD}	-3823	-1277
3	T_1	-3743	-1277
4	T_2	-3663	-1277
5	V_{SS}	-3583	-1277
6	$\overline{CS}$	-3503	-1277
7	$\overline{RES}$	-3423	-1277
8	AO	-3343	-1277
9	V_{SS}	-3263	-1277
10	$\overline{WR}$	-3183	-1277
11	$\overline{RD}$	-3103	-1277
12	V_{DD}	-3023	-1277
13	D_0	-2728	-1277
14	D_1	-2228	-1277
15	D_2	-1728	-1277
16	D_3	-1228	-1277
17	D_4	-728	-1277
18	D_5	-228	-1277
19	D_6	272	-1277
20	D_7	772	-1277
21	SCL	1120	-1277
22	SI	1200	-1277
23	V_{DD}	1280	-1277
24	V_{DD}	1360	-1277
25	V_{DD}	1440	-1277
26	V_{SS}	1520	-1277
27	V_{SS}	1600	-1277
28	V_{SS}	1680	-1277
29	V_{OUT}	1760	-1277
30	V_{OUT}	1840	-1277
31	V_{OUT}	1920	-1277
32	$C2^-$	2000	-1277
33	$C2^-$	2080	-1277
34	$C2^+$	2160	-1277
35	$C2^+$	2240	-1277
36	$C3^+$	2320	-1277
37	$C3^+$	2400	-1277
38	$C3^-$	2480	-1277
39	$C3^-$	2560	-1277
40	$C1^-$	2640	-1277
41	$C1^-$	2720	-1277
42	$C1^+$	2800	-1277
43	$C1^+$	2880	-1277
44	V_{DD}	2960	-1277
45	V_1	3040	-1277
46	V_2	3120	-1277
47	V_3	3200	-1277
48	V_4	3280	-1277
49	V_5	3360	-1277
50	V_5	3440	-1277

No.	Terminal	X (μm)	Y (μm)
51	V_5	3520	-1277
52	VR	3600	-1277
53	V_{DD}	3680	-1277
54	P/S	3760	-1277
55	C_{86}	3840	-1277
56	V_{SS}	3920	-1277
57	C_{25}	4063	-880
58	C_{24}	4063	-800
59	C_{23}	4063	-720
60	C_{22}	4063	-640
61	C_{21}	4063	-560
62	C_{20}	4063	-480
63	C_{19}	4063	-400
64	C_{18}	4063	-320
65	C_{17}	4063	-240
66	C_{16}	4063	-160
67	C_{15}	4063	-80
68	C_{14}	4063	0
69	C_{13}	4063	80
70	C_{12}	4063	160
71	C_{11}	4063	240
72	C_{10}	4063	320
73	C_9	4063	400
74	C_8	4063	480
75	C_7	4063	560
76	C_6	4063	640
77	C_5	4063	720
78	C_4	4063	800
79	C_3	4063	880
80	C_2	4063	960
81	C_1	4063	1040
82	C_0	4063	1120
83	SEG_0	3145	1276
84	SEG_1	3065	1276
85	SEG_2	2985	1276
86	SEG_3	2905	1276
87	SEG_4	2825	1276
88	SEG_5	2745	1276
89	SEG_6	2665	1276
90	SEG_7	2585	1276
91	SEG_8	2505	1276
92	SEG_9	2425	1276
93	SEG_{10}	2345	1276
94	SEG_{11}	2265	1276
95	SEG_{12}	2185	1276
96	SEG_{13}	2105	1276
97	SEG_{14}	2025	1276
98	SEG_{15}	1945	1276
99	SEG_{16}	1865	1276
100	SEG_{17}	1785	1276

No.	Terminal	X (μm)	Y (μm)
101	SEG 18	1705	1276
102	SEG 19	1625	1276
103	SEG 20	1545	1276
104	SEG 21	1465	1276
105	SEG 22	1385	1276
106	SEG 23	1305	1276
107	SEG 24	1225	1276
108	SEG 25	1145	1276
109	SEG 26	1065	1276
110	SEG 27	985	1276
111	SEG 28	905	1276
112	SEG 29	825	1276
113	SEG 30	745	1276
114	SEG 31	665	1276
115	SEG 32	585	1276
116	SEG 33	505	1276
117	SEG 34	425	1276
118	SEG 35	345	1276
119	SEG 36	265	1276
120	SEG 37	185	1276
121	SEG 38	105	1276
122	SEG 39	25	1276
123	SEG 40	-55	1276
124	SEG 41	-135	1276
125	SEG 42	-215	1276
126	SEG 43	-295	1276
127	SEG 44	-375	1276
128	SEG 45	-455	1276
129	SEG 46	-535	1276
130	SEG 47	-615	1276
131	SEG 48	-695	1276
132	SEG 49	-775	1276
133	SEG 50	-855	1276
134	SEG 51	-935	1276
135	SEG 52	-1015	1276
136	SEG 53	-1095	1276
137	SEG 54	-1175	1276
138	SEG 55	-1255	1276
139	SEG 56	-1335	1276
140	SEG 57	-1415	1276
141	SEG 58	-1495	1276
142	SEG 59	-1575	1276
143	SEG 60	-1655	1276
144	SEG 61	-1735	1276
145	SEG 62	-1815	1276
146	SEG 63	-1895	1276
147	SEG 64	-1975	1276
148	SEG 65	-2055	1276
149	SEG 66	-2135	1276
150	SEG 67	-2215	1276

No.	Terminal	X (μm)	Y (μm)
151	SEG 68	-2295	1276
152	SEG 69	-2375	1276
153	SEG 70	-2455	1276
154	SEG 71	-2535	1276
155	SEG 72	-2615	1276
156	SEG 73	-2695	1276
157	SEG 74	-2775	1276
158	SEG 75	-2855	1276
159	SEG 76	-2935	1276
160	SEG 77	-3015	1276
161	SEG 78	-3095	1276
162	SEG 79	-3175	1276
163	C 26	-4064	1121
164	C 27	-4064	1041
165	C 28	-4064	961
166	C 29	-4064	881
167	C 30	-4064	801
168	C 31	-4064	721
169	C 32	-4064	641
170	C 33	-4064	561
171	C 34	-4064	481
172	C 35	-4064	401
173	C 36	-4064	321
174	C 37	-4064	241
175	C 38	-4064	161
176	C 39	-4064	81
177	C 40	-4064	1
178	C 41	-4064	-79
179	C 42	-4064	-159
180	C 43	-4064	-239
181	C 44	-4064	-319
182	C 45	-4064	-399
183	C 46	-4064	-479
184	C 47	-4064	-559
185	C 48	-4064	-639
186	C 49	-4064	-719
187	C 50	-4064	-799
188	C 51	-4064	-879
189	COMI	-4064	-959
ALIGNMENT	ALI_A1	-4090	-1303
ALIGNMENT	ALI_A2	4089	-1303
ALIGNMENT	ALI_B1	4089	1282
ALIGNMENT	ALI_B2	-4090	1282

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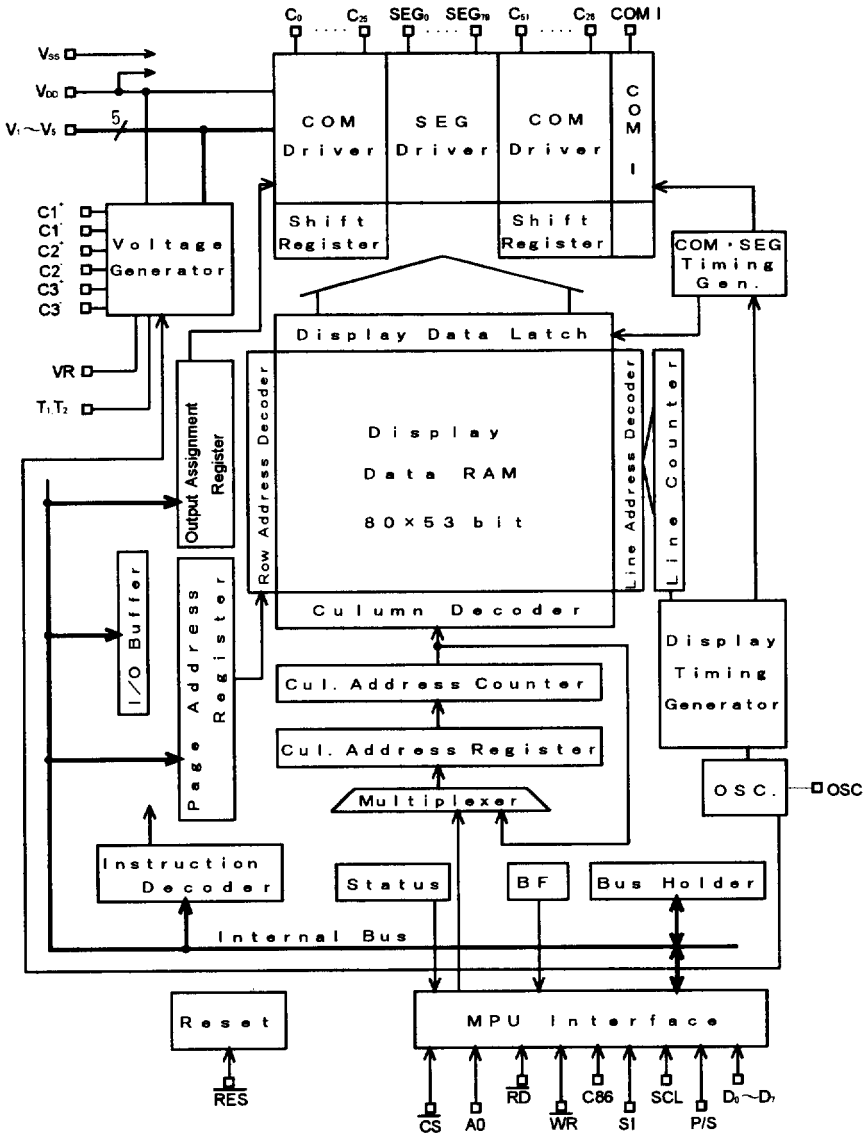
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function
2,12,23, 24,25,44 ,53	V_{DD}	Power	V_{DD} =+3V. (Less then 4.5V should apply when voltage tripler using.) (Less then 3.3V should apply when voltage quadrupler using.)
5,9,26, 27,28,56	V_{SS}	GND	V_{SS} =0V
45 46 47 48 49,50,51	V_1 V_2 V_3 V_4 V_5	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ When internal power supply is on, internal circuits generated and supply following LCD bias voltage to $V_1 \sim V_4$ terminals. The ratio of LCD bias is selected by "LCD bias set" instruction. Term. / Volt.: V_1 = V_5 +7/8V_{LCD}; V_2 = V_5 +6/8V_{LCD}; V_3 = V_5 +2/8V_{LCD}; V_4 = V_5 +1/8V_{LCD} (V_{LCD} =V_{DD} -V_5)
42,43 40,41 34,35 32,33 36,37 38,39	$C1^+$ $C1^-$ $C2^+$ $C2^-$ $C3^+$ $C3^-$	O	Step up capacitor connecting terminals. - In case of quadrupler operation, connect the capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, and $C3^+$ and $C3^-$. - In case of tripler operation, connect the capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, connect $C2^-$ to $C3^-$, and $C3^+$ should be open.(or connect the capacitor between $C1^+$ and $C1^-$, $C3^+$ and $C3^-$, connect $C2^+$ to $C3^+$, and $C2^-$ should be open.) - In case of doubler operation, connect the capacitor between $C1^+$ and $C1^-$, connect $C1^-$ to $C3^-$, and $C2^-$, $C2^+$, $C3^+$ should be open.
29,30,31	V_{OUT}	O	Step up voltage output terminal. Connect the set up capacitor between this terminal and V_{SS}.
52	VR	I	Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance connect between V_{DD} and V5 terminal.
3 4	T_1 T_2	I	LCD bias voltage control terminals. ※ Don't Care T_1 / T_2 / Step up cir. / Voltage Adj. / V/F Cir.: L / ※ / Available / Available / Available H / L / Not Avail. / Available / Available H / H / Not Avail. / Not Avail. / Available
13 ~ 20	$D_0 \sim D_7$	I/O	Tri-state bilateral Data I/O terminal when 8-bit parallel operation.
8	A0	I	Connect to the Address bus of MPU. The data on the D_0 to D_7 is distinguished Display data or Instruction by this signal. A0 / Dist.: H = Display Data; L = Instruction
7	$\overline{RES}$	I	Reset terminal. When the $\overline{RES}$ terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of $\overline{RES}$.
6	$\overline{CS}$	I	Chip select terminal. Data Input/Output are available during $\overline{CS}$ ="L".

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No.	Symbol	I/O	Function
11	$\overline{RD}$ (E)	I	<When interface with 80 type MPU> $\overline{RD}$ signal of 80 type MPU input terminal. Active"L". During this signal "L", the data bus becomes as output terminal. <When interface with 68 type MPU> Enable clock of 68 type MPU input terminal. Active "H".
10	$\overline{WR}$ (R/W)	I	<When interface with 80 type MPU> Connect the 80 type MPU $\overline{WR}$ signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal. <When interface with 68 type MPU> Read/write control signal of 68 type MPU input terminal. R/W: H = Read, L = Write
55	C86	I	Select the MPU interface type. C86: H = 68 Type, L = 80 Type
22	SI	I	Serial data input terminal .
21	SCL	I	Serial data clock signal input terminal. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.
54	P/S	I	Serial or parallel interface select terminal. "H": $\overline{CS}$, A0, D_0~D_7, $\overline{RD}$、$\overline{WR}$, — "L": $\overline{CS}$, A0, SI, Write only, SCL *RAM data and status read operation is impossible when select the serial interface. ・ When select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L". ・ When select the serial interface (P/S="L"), $\overline{RD}$ and $\overline{WR}$ must be fix "H" or "L", and D_0~D_7 becomes to the high impedance state.
1	OSC	I	System clock input terminal for Maker testing. This terminal should be open.

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>57
~
82</td><td>C_{25}
~
C_0</td><td>O</td><td>LCD drive output terminals.
Segment output terminals : SEG_0 to SEG_{79}
Common output terminals :C_0 to C_{51}

・ Segment output terminal
Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM.
<table><tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal</th><th>Reverse</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr><tr><td>L</td><td>V_5</td><td>V_3</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr><tr><td>L</td><td>V_3</td><td>V_5</td></tr></table>
・ Common Output Terminal
Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data.
<table><tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr><tr><td>L</td><td>V_{DD}</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr><tr><td>L</td><td>V_4</td></tr></table></td></tr>
<tr><td></td><td>COMI</td><td>O</td><td>Icon common output terminal.
Icon common output when Icon Display instruction execution.
<table><tr><th></th><th>Icon Display ON</th><th>Icon Display OFF</th></tr><tr><td>State</td><td>COM_{52}</td><td>V_1 or V_4</td></tr></table></td></tr>
</table>

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■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode. the busy flag(BF) is "1", and any instruction except the status read are inhibited .

The busy flag output from D_7 terminal when status read instruction is executed.

If enough cycle time over then t_{cyc} indicated in the bus timing characteristics is kept,no need to checkt he busy flag and it realized high performance for the MPU.

(1-2) Line Counter

The Line Counter is reset at the FR signal changing and counts up by synchronizing common signal cyc le and generate the line address which addressing the read out line of Display Data RAM.

(1-3) Column Address Counter

The column address counter is 8-bit presentable counter which addressing the column address as show n in Fig. 1. This counter increments (+1) up to $(A0)_H$ when the Display Data Read/Write instruction is executed. This counter auto-increment up to $(4F)_H$, but accessing to the display data RAM over than $(4F)_H$ is forbidden.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM correspondence to the Segment Driver.

(1-4) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the dat a by changing the page, the page address set instruction is required. Page address "7"(D_2, D_1, D_0 ="H") is Icon RAM area, the data only for the D_0 is valid.

(1-5) Display Data RAM

Display Data RAM consists of 4,240 bits stores the bit image display data (each bit correspond to the ea ch pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM output 80 bit parallel data addressed by the line counter, and these data are set into the Display Data Latch.

This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize r ewriting.

The relation between column address and segment output can inverse by the Address Inverse Instructio n ADC as shown in Fig. 1.

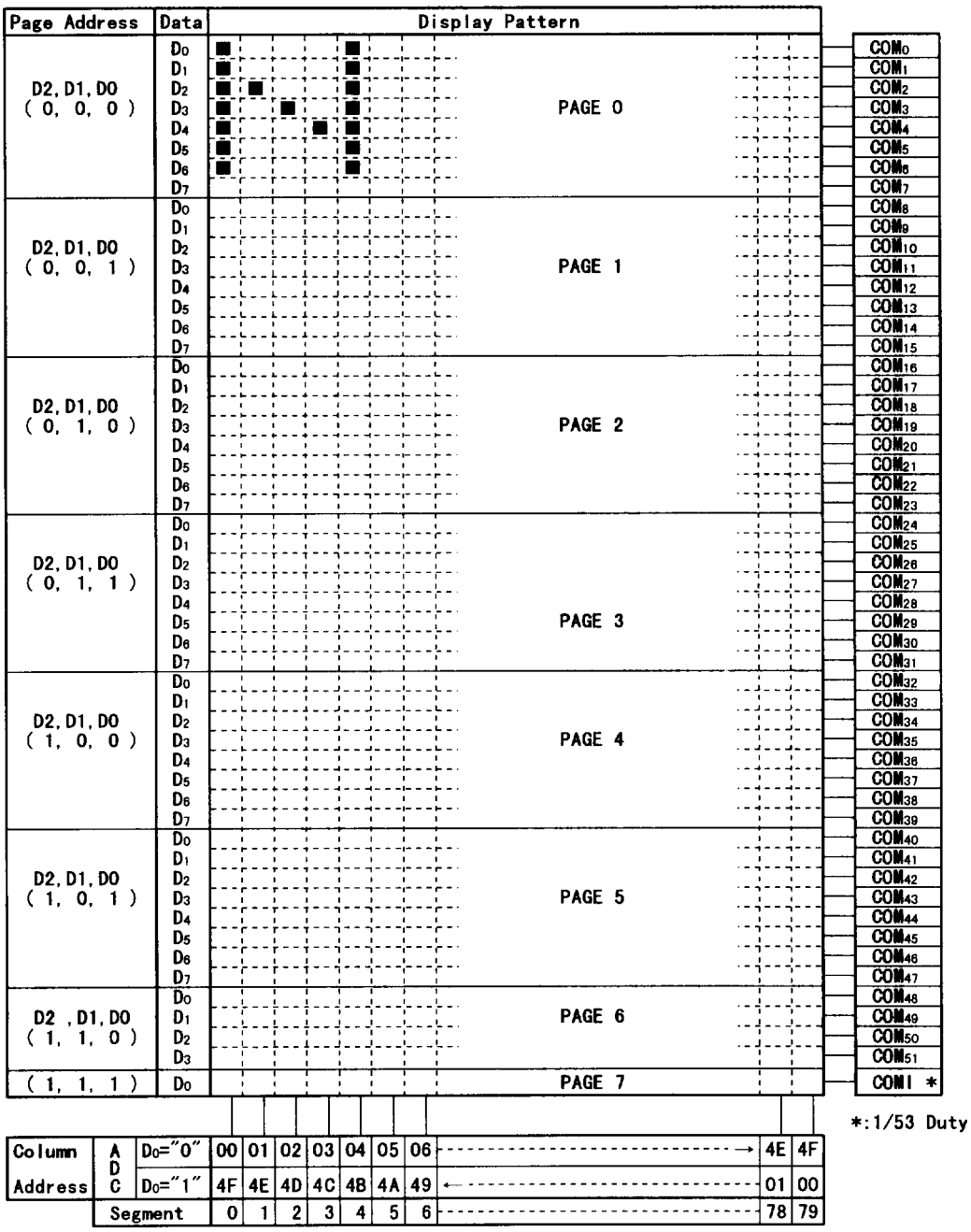

Fig. 1 Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/53 duty set.)

(1-6) Common and Segment Driver Assignment

The scanning order can be assigned by setting A_3 of the Output Assignment Register as shown Table 1.

The location of Segment Drivers are fixed at any time.

Table 1

Register		COM Output Terminals			
A3	PAD No.	82	57	188	163
	Pin name	C_0	C_{25}	C_{51}	C_{26}
0	→	COM_0 ⇢	COM_{25}	COM_{51} ⇠	COM_{26}
1	→	COM_{51} ⇠	COM_{26}	COM_0 ⇢	COM_{25}

The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COMI is fixed to COM_{52} timing regardless the other Common Driver assignment.

(1-7) Reset Circuits

The NJU6577 performs following initialization when the $\overline{RES}$ input is put on the "L" level.

Initialization

① Display Off
② Normal Display(Non-inverse display)
③ Icon Display Reset
④ ADC Select : Normal (ADC Instruction D_0 ="0")
⑤ Read Modify Write Mode Off
⑥ Internal Power supply(Step up) circuits Off
⑦ Clear the serial interface register
⑧ Set the address $(00)_H$ to the Column Address Counter
⑨ Set the page "0" to the Page Address Register
⑩ Select the D_3 of the Output Assignment Register to "0"
⑪ Set the EVR register to $(00)_H$

The $\overline{RES}$ terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface Example". The reset signal require over than 10us $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{RES}$ signal, the normal operation is starting.

In case of the internal power supply(Step up) circuits do not use, the $\overline{RES}$ terminal must be "L" when external power supply turn on. $\overline{RES}$="L" input reset internal register and set above default, but oscillation circuits and output terminals like as D_0 through D_7 are no influence.

No initialization by $\overline{RES}$ when power turns on, will make Hung up condition, therefore please initialize by the $\overline{RES}$ when power turns on. By the reset Instruction performs only ⑧ through ⑪ mentioned in above.

The noise into the $\overline{RES}$ terminal should be cared when of the application design to avoid the error function.

(1-8) LCD Driving

(a) LCD Driving Circuits

NJU6577 incorporates 133 LCD Drivers like as 80 Segment drivers, 52 Common drivers and 1 Icon common driver. 52 Common drivers incorporate the shift register which scanning the common display signal. The combination among the Display data, COM scan signal and FR signal define the LCD driving output voltage. The output wave form is mentioned in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 80-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver. The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits

The clock for Line Counter and latch signal for the Latch Circuits are generated from display clock(CL). The line address is renewed by synchronizing with display clock and 80 bits display data are latched into display latch circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR has a function to generate the two frame alternative driving method waveform for the LCD panel.

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(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

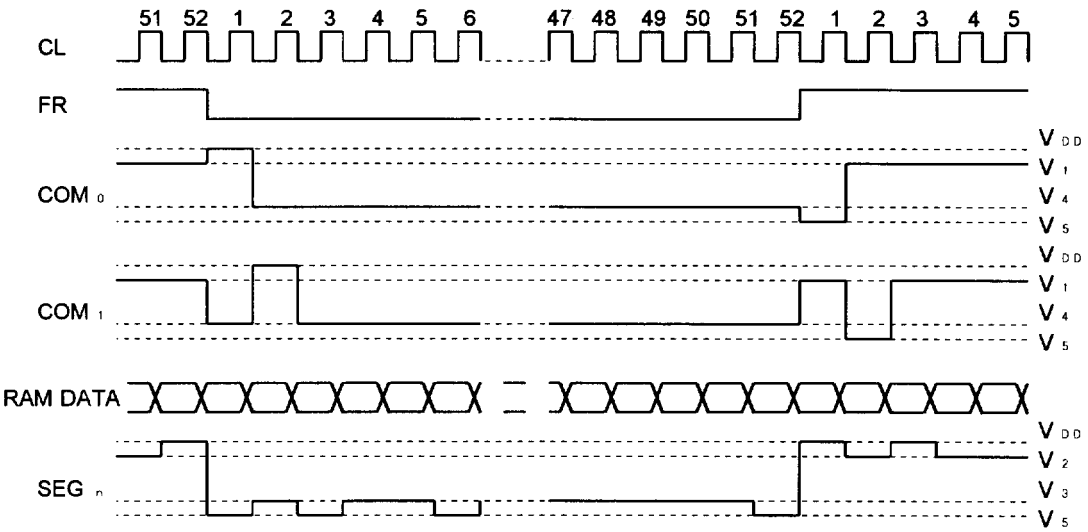


Fig. 2 Waveform of Display Timing

(f) Oscillation Circuits

The Oscillation Circuits which incorporates the oscillating resistance R and capacitor C, is a low power CR oscillator and it is used as display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuits output frequency is divided by 4 which is used as display clock CL.

(g) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Tripler or Doubler) Circuits, Regulation Circuits, and Voltage Follower. Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the large size LCD panel application. If the contrast is no good in those application, please use external power supply supplied more high current.

The suitable values of the capacitors connecting to the V1 to V5 terminals, the step up circuit and the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption in the LCD panel is changeable with the display pattern. Therefore a trial with actual module should be practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, voltage follower circuits are off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD supply from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$ and VR are open. The status of internal power supply can select by T_1 and T_2 terminal. The external power supply can be used together with some of internal power supply function.

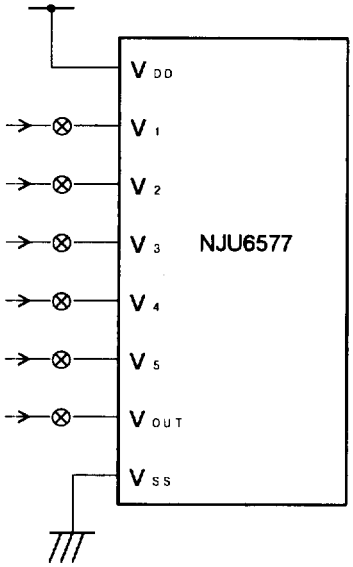
Table 3. (*:Don't Care)

T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term.
L	*	○	○	○	-		
H	L	×	○	○	V_{OUT}	OPEN	
H	H	×	×	○	V_5, V_{OUT}	OPEN	OPEN

When (T_1, T_2)=(H, L), the terminal for step up circuits of $C1^+$,$C1^-$,$C2^+$,$C2^-$,$C3^+$,$C3^-$ are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T_1, T_2)=(H, H), terminals for step up circuits and VR are open, and supply the LCD driving voltage from outside due to the Step up circuits and Voltage adjust circuits are stop its operation.

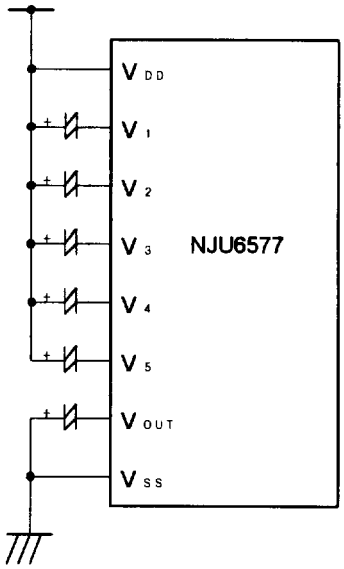
○ Examples for application circuits of the internal Power Supply

(1)None of the internal power supply functions.



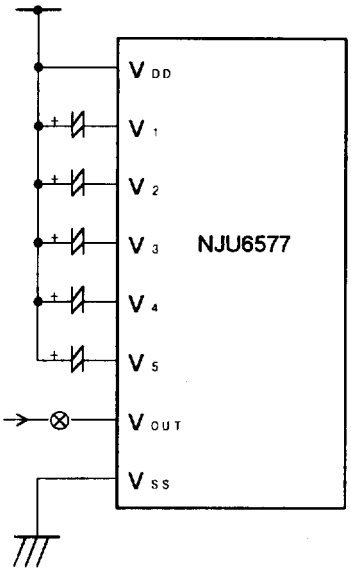
(2) All of the internal power supply functions.
(Step up, Voltage Adj., Buffer(V/F))

(T1, T2) = (L, *) *:Don't care.



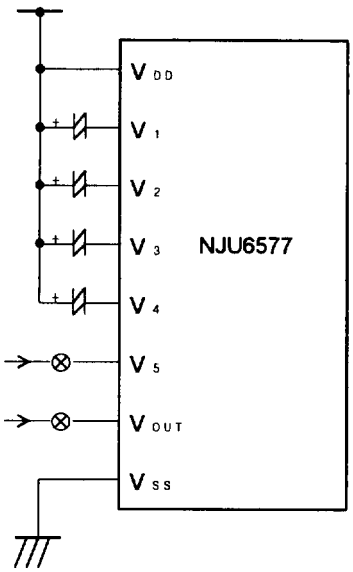
(3)Some of the internal power supply functions.
(Voltage Adjust., Buffer(V/F))

(T1,T2) = (H,L)



(4)Some of the internal power supply functions.
(Buffer(V/F))

(T1,T2) = (H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6577 distinguish the signal on the data bus by combination of A0,$\overline{RD}$ and $\overline{WR}$. Normally, the busy check is not required as the NJU6577 is operating so first because of the decode of the instruction and execution are performs only depend on the internal timing which not depend on the external clock. In case of serial interface, the data input as MSB first serially.

The Table. 4 shows the instruction codes of the NJU6577.

Table 4. Instruction Code

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Add. Register
(3)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								Read the Data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0 1	Inverse the On and Off Display 0:Normal 1:Inverse
(10)	Whole Display On /Normal Display	0	1	0	1	0	1	0	0	1	0	0 1	Whole Display Turns On 0:Normal 1:Whole Disp. On
(11)	Icon Display	0	1	0	1	0	1	0	1	0	1	0 1	Set the Duty Ratio 0:No Icon 1:With Icon
(12)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(15)	Output Assignment Register Set	0	1	0	1	1	0	0	A_3	*	*	*	Set the scanning order of common drivers to the Register
(16)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0 1	0:Int. Power Supply Off 1:Int. Power Supply On
(17)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after after the internal(external) power supply is turned on
(18)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V_5 output level to the EVR register
(19)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power save Mode

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 7 is a Icon display data area which available only for the D_0.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	1	*	A_2	A_1	A_0

(*:Don't Care)

A_2	A_1	A_0	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

(c) Column Address

When MPU access the Display Data RAM, page address set(refer(b) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting.

This counter auto-increment up to $(A0)_H$, but accessing to the display data RAM over than $(4F)_H$ is forbidden.

After writing 1 page data, page address setting is required due to page address doesn't increase automatically.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
Higher Order	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower Order	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				.				.
				.				.
0	1	0	0	1	1	1	1	4F

(d) Status Read

This instruction read out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.
0 :Counterclockwise Output(Inverse) Column Address 79-n ←→ Segment Driver n
1 :Clockwise Output (Normal) Column Address n ←→ Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On"
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initialization period by $\overline{RES}$ signal or reset instruction.
0 : —
1 : Initialization Period

(e) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
1	1	0	WRITE DATA							

(f) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page address. The column address increase "1" automatically when reading, therefore, the MPU can read the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read is required after column address set as explain in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data can not be readout.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
1	0	1	READ DATA							

(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	0	0	D

D 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Data RAM is no changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"
1: Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction executes the all pixel terns on regardless the contents of the Display Data RAM. In this time, the contents of Display Data RAM is no change and is kept. This instruction takes over precedence over the "Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	1	0	D

D 0: Normal Display
1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the power save mode(refer to the (s) Power Save) .

(j) Icon Display

This instruction set the 1/53 duty for the Icon Display. The COMI terminal operate as COM 52 and output the icon display data stored in D 0 of Display Data RAM page 8 (refer to the Fig. 1).

A0	$\overline{RD}$	R/$\overline{W}$	D 7						D 0
0	1	0	1	0	1	0	1	0	1	D

D 0: 1/52 Duty
1: 1/53 Duty

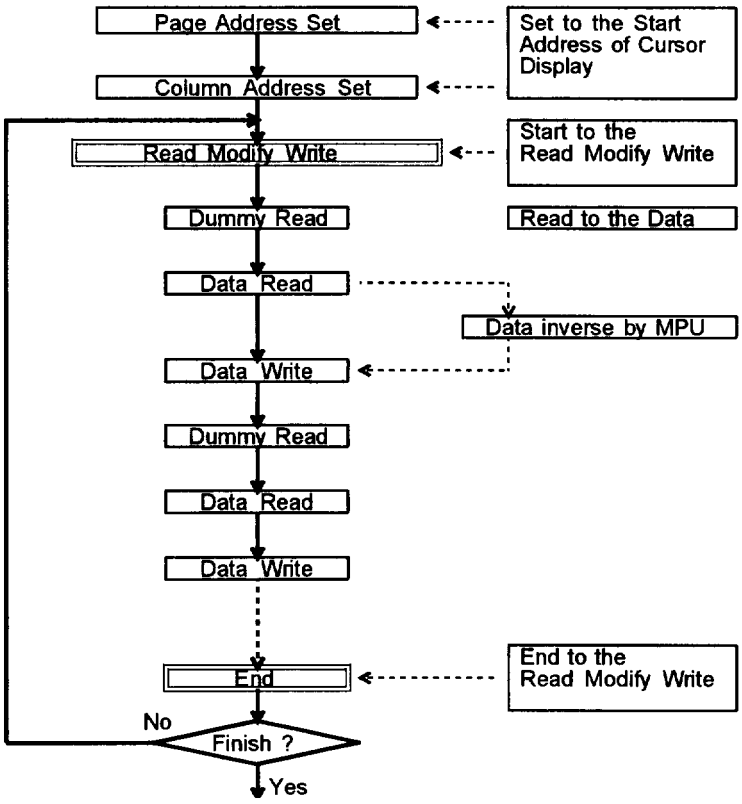
(k) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the Read Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction is executed, but the address is no change when the Display Data Read Instruction is executed. This status is continued during End instruction execution. When the End instruction is entered the column address back to the address where the Read Modify Write instruction entering. By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

A0	$\overline{RD}$	R/$\overline{W}$	D 7						D 0
0	1	0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

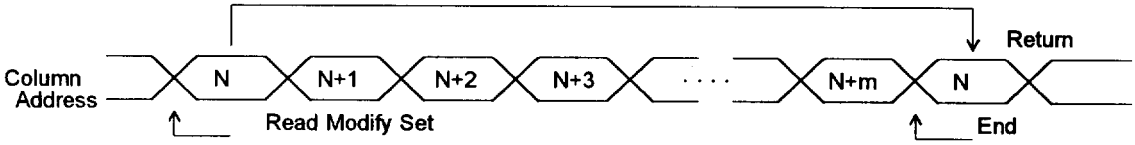
(l) Sequence of inverse display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	1	0	1	1	1	0



(n) Reset

This instruction executes the following initialization.

Initialization

① Set the Address (00)$_H$ to the Column Address Counter.
② Set the page "0" to the Page Address Register.
③ Select the D3 of the Output Assignment Register to "0".
④ Set 0 to the EVR Register to (00)$_H$.

In this time, there are no influence to the Display Data RAM.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal must be required for the initialization when the power terns on. Substitution of Reset Instruction for the reset signal input to the $\overline{RES}$ terminal is not allowed.

(o) Output Assignment Register

This instruction sets the common driver scanning order .

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	0	0	A3	*	*	*

(*:Don't Care)

A3: Set the scanning order .(Refer to 1-6)

(p) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is required.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q) LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 to V4 and output LCD driving waveform through the COM/SEG terminals.

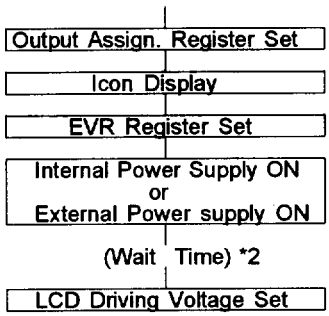
A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	1	0	1	1	0	1

NJU6577 contains operational amplifiers for LCD bias voltage V1 to V4. These amplifiers current are reduced in order to realize low power consumption. Because of this reduction, LCD driving voltage V1 to V4 might be unstable just after the internal power supply is turned on.
LCD Driving Voltage Set instruction is prepared for this unstableness.

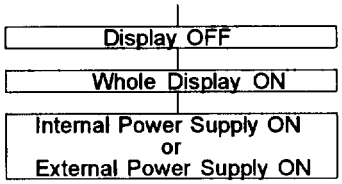
● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is tuned on/of.
When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence mentioned in (s) is required.

Turn ON sequence

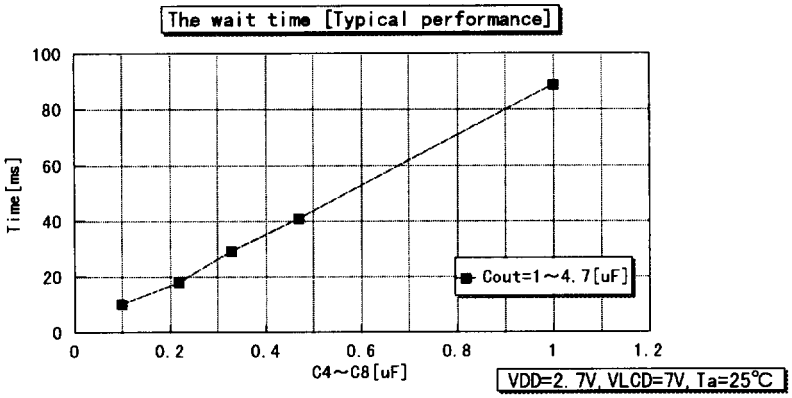


Turn OFF sequence



*1 This instruction is required in both cases of the internal and external power supply.
Until "LCD driving voltage Set" execution, NJU6577 operating current is higher than usual state and all COM/ SEG terminals output V_{DD} level continuously except LCD driving waveform.

*2 The wait time depends on the C_4, C_5, C_6, C_7, C_8 and C_{OUT} capasitors((4) (d)Fig.4), V_{DD} and V_{LCD} voltage.
Therefore a test on actual module should be practiced. Refer to the following graph.



(r) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this instruction execute, the internal Electrical Variable Resistor(EVR) to change the V_5 output voltage, generate one voltage from 16 voltage state. The range of V_5 output level can be adjusted by the external resistance. For more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	0	0	A3	A2	A1	A0

A4	A3	A2	A1	A0	V_{LCD}
0	0	0	0	0	High
		:			:
		:			:
1	1	1	1	1	Low

$V_{LCD} = V_{DD} - V_5$

When EVR doesn't use, set the EVR register to (0,0,0,0,0).

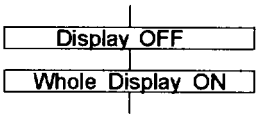
(s) Power Save (Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuit put on the power save mode and the operating current is reduced as same as stand by current.
The internal status in the Power Save Mode is as follows;

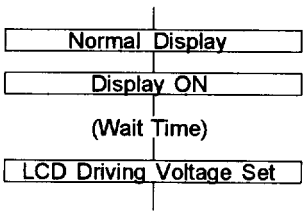
① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
③ Keeping the display data and operating mode as before the power save mode.
④ All of LCD driving bias voltage fixed to the V_{DD} level.

The power save and its release should be performed according to the following sequences.

Power Save Sequence



Power Save Release Sequence



*1 Power save mode requires dual-instruction. After the second instruction" whole Display ON", the power save mode starts.
*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.
*3 Until "LCD driving voltage set" execution, NJU6577 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.
*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.
*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

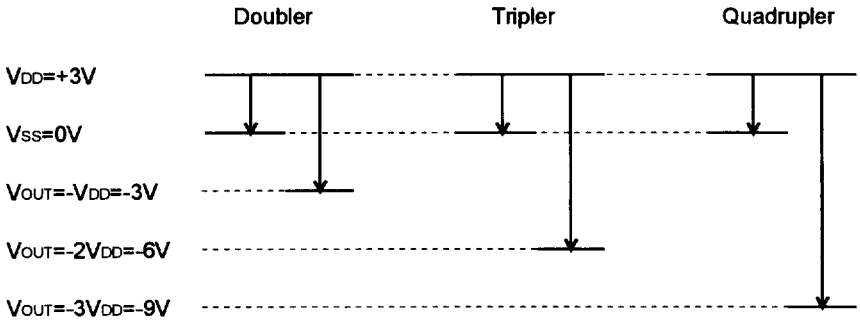
(4) Internal Power Supply

(a) Voltage quadrupler

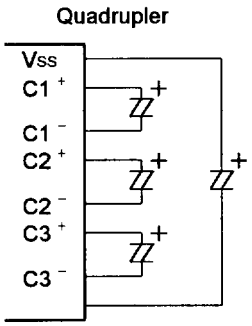
Four times negative voltage(V_{DD} common) of the voltage V_{DD} -V_{SS} is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, $C3^+$ and $C3^-$, V_{SS} and V_{OUT}.

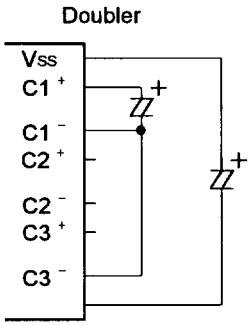
Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage quadrupler operation, the operation voltage

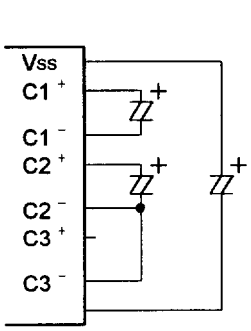
V_{DD} should be less than 3.3V.

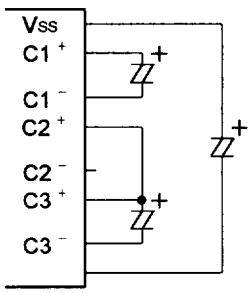


· Examples for connecting the capacitors









(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_S through the voltage adjust circuits. The output voltage of V_S is adjusted by changing the Ra and Rb within the range of $|V_S| < |V_{OUT}|$. The output voltage can calculated by the following formula.

$$V_{LCD} = V_{DD} - V_S = (1+Rb/Ra) \cdot V_{REG} \cdots\cdots ①$$

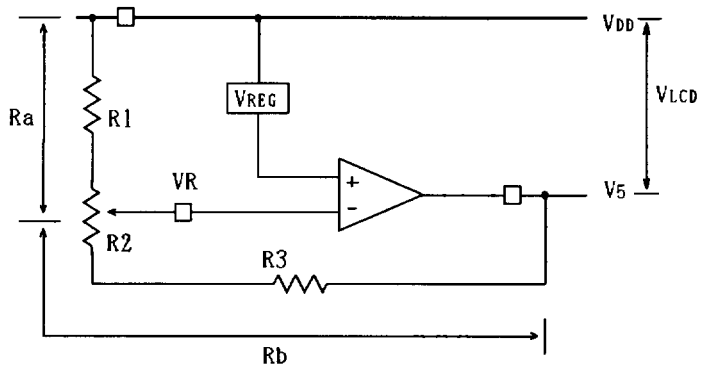


Fig. 3

Where, the V_{REG} is a constant voltage in the NJU6577 like as V_{REG}=2.0V.
To adjust the output voltage from V_S, connect the variable resistance among VR, V_{DD} and V_S as shown in Fig. 3. When fine tuning for V_S is needed, combine with the fixed resistance of R1, R3 and variable resistance of R2 is recommended as shown in Fig. 3.

[Design example for R1, R2 and R3; V_{DD}=3V / reference]

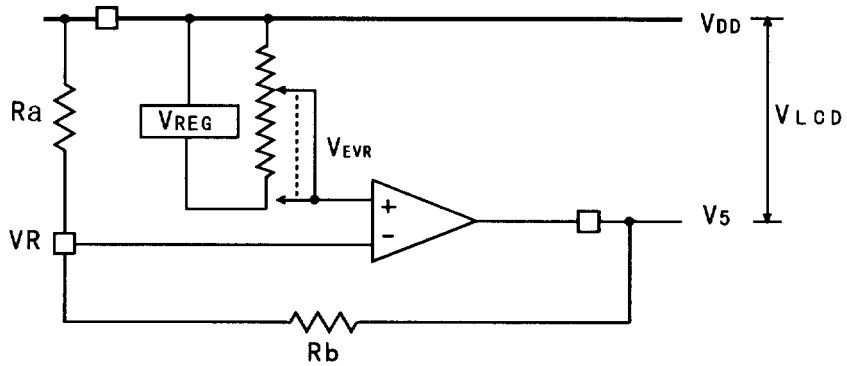
- R1+R2+R3=5M Ω (Determined by the current flown between V_{DD}-V_S)
- Variable voltage range by the R2. -4V ~ -6V (V_{LCD}=V_{DD}-V_S → 7V ~ 9V)
  (Determined by the LCD electrical characteristics)
- R1, R2 and R3 are calculated by above conditions and the formula of ① to mentioned below;
  R1=1.111M Ω
  R2=0.318M Ω
  R3=3.571M Ω

The voltage adjust circuits has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuits serially.
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_5 which controls LCD display contrast can adjust by the instruction. The EVR function is executed to set the 8 bits data into the EVR resistor and determine the one output voltage status out of 32 prefixed voltage status as the following table .

When execute the EVR function, set the T_1 and T_2 except the "H, H" and execute the Internal Power Supply On instruction.



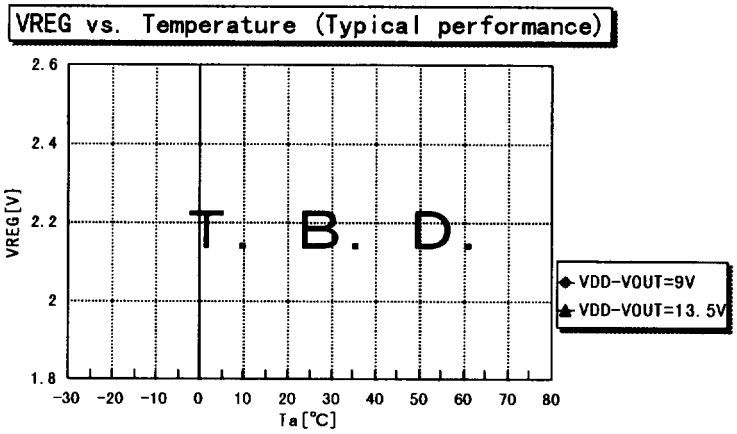
$$V_{LCD} = V_{DD} - V_5 = (1 + Rb/Ra) \cdot V_{EVR} \quad \cdots\cdots \text{②}$$

[: $V_{EVR} = V_{REG} - n \cdot (V_{REG}/164)$]

EVR register		$n \cdot (V_{REG}/164)$	V_{LCD}
$(00)_H$	(0,0,0,0,0)	$0 \cdot (V_{REG}/164)$	High
$(01)_H$	(0,0,0,0,1)	$1 \cdot (V_{REG}/164)$	
$(02)_H$	(0,0,0,1,0)	$2 \cdot (V_{REG}/164)$	
$(03)_H$	(0,0,0,1,1)	$3 \cdot (V_{REG}/164)$	
. . .	. . .	. . .	
$(1E)_H$	(1,1,1,1,0)	$30 \cdot (V_{REG}/164)$	
$(1F)_H$	(1,1,1,1,1)	$31 \cdot (V_{REG}/164)$	Low

When EVR function doesn't use, (D_4 , D_3 , D_2 , D_1 , D_0) of EVR register set to (0, 0, 0, 0, 0) by the $\overline{RES}$ signal or "EVR Register Set" instruction.

*) V_{REG}, depends on the voltage between V_{DD} and V_{OUT}, the operating temperature. Please refer to the following graphs.

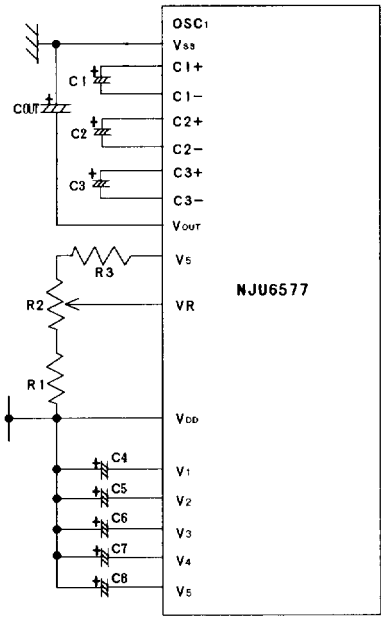


(d) LCD Driving Voltage Generation Circuits

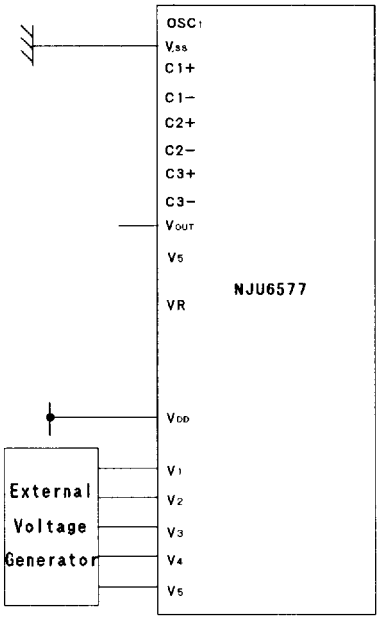
The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V_5 voltage by the bleeder resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 4, Five capacitors are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitors C4, C5, C6, C7 and C8 determine by combine with the actual LCD panel.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

$V_{LCD} = V_{DD}-V5 \fallingdotseq 7 \sim 9V$ Changed

Item	Value
C_{OUT}	4.7～10μF
C1,C2,C3	4.7～10μF
C4 to C8	0.1～0.47μF
R1	1.111MΩ
R2	0.318MΩ
R3	3.571MΩ

Fig. 4

*1 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.

*2 Following connection of VOUT is required when external power supply using.

When $V_{SS} > V_5$ -- $V_{OUT} = V_5$

When $V_{SS} \leqq V_5$ -- $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6577 can interface by using both of 8 bit bilateral data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined the P/S terminal connected to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out is impossible.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	-	-	$D_0 \sim D_7$
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6577 can interface both of 68 or 80 type MPU directly by setting the parallel interface (P/S="H") and "H" or "L" of the C86 terminal as shown in table 6.

Table 6

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$
H	68 type MPU	$\overline{CS}$	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6577 discriminate the signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to CS="L"and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal is MSB first like as the order of D_7,D_6,$\cdots\cdots D_0$, and the data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or $\overline{CS}$ terminal becomes "H" in spite of the data less then 8 bits, NJU6577 recognizes wrong data as a instruction data. Therefore 8bits data is required for the input data. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface .

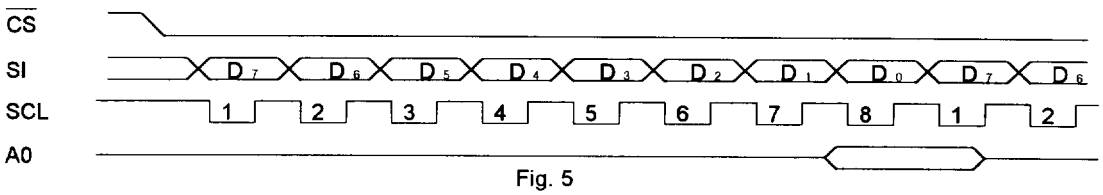


Fig. 5

(5-5) Access to the Display Data RAM and Internal Register.

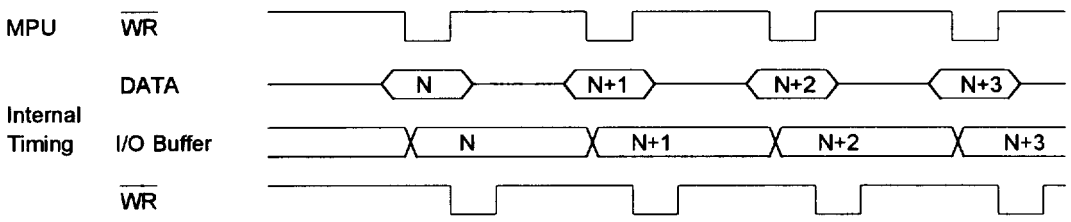
The NJU6577 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU read out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at next data read cycle. And when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6577 is available because of the limitation of access time of NJU6577 locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{OS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP operation cycle which equivalent to the waiting operation is useful.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

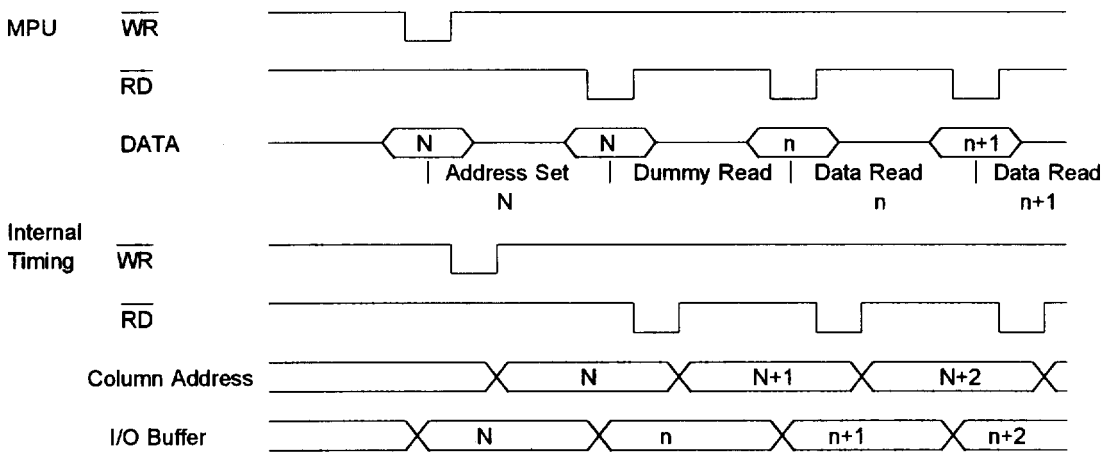


Fig.6

(5-6) Chip Select

CS is Chip Select terminal. The Chip Select is executed by the setting of $\overline{CS}$="L". Only the select mode, the interface with MPU is available. In the non select period, the D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, SI and SCL input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 4.5 (used Tripler) - 0.3 ~ + 3.3 (used Quadrupler)	V
Supply Voltage (2)	V_5	V_{DD} -13.5 ~ V_{DD} +0.3	V
Supply Voltage (3)	V_1~V_4	V_5 ~ V_{DD} +0.3	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD} +0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 125(Chip) - 55 ~ + 100(TCP)	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1) (V_{DD}=3V ± 10%, V_{SS}=0V, Ta=-20 ~ +75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage(1)	Recommend	V_{DD}			2.7	3.0	3.3	V	5
	Available				2.4		5.5		
Operating Voltage(2)	Recommend	V_5			V_{DD} -13.5		V_{DD} -3.5	V	
	Available				V_{DD} -13.5				
	Available	V_1,V_2	V_{LCD} = V_{DD} - V_5		V_{DD} -0.6xV_{LCD}		V_{DD}		
	Available	V_3,V_4			V_5		V_{DD} -0.4xV_{LCD}		
Input Voltage	High Level	V_{IHC}	D0,D1...D7, A0,CS,RES, RD,WR,C86, SI,SCL,P/S Terminals	V_{DD} =2.7V	0.8xV_{DD}		V_{DD}	V	
	Low Level	V_{ILC}			V_{SS}		0.2xV_{DD}		
Output Voltage	High Level	V_{OHC}	D0,D1...D7, Terminals V_{DD} =2.7V	I_O =-0.5mA	0.8xV_{DD}		V_{DD}	V	
	Low Level	V_{OLC}		I_O = 0.5mA	V_{SS}		0.2xV_{DD}		
Input Leakage Current		I_{LI}	All input terminals		-1.0		1.0	uA	
		I_{LO}	All I/O term.(D0...D7)		-3.0		3.0		6
Driver On-resistance		R_{ON1}	Ta=25°C ext. power supply	V_{LCD} =13.5V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD} =8.0V		3.0	4.5		
Stand-by Current		I_{DDQ1}	during sleep Mode			T.B.D.	T.B.D.	uA	8
		I_{DDQ1}	during stand-by Mode			T.B.D.	T.B.D.	uA	

5

■ ELECTRICAL CHARACTERISTICS (2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Current	I_{DD1}	Display	V_{DD}=2.7V, V_{LCD}=8V		T.B.D.	T.B.D.	uA	8
	I_{DD2}	Accessing fcyc=200kHz	V_{DD}=2.7V		T.B.D.	T.B.D.	uA	9
Input Terminal Capacitance	C_{IN}	A0,$\overline{CS}$,$\overline{RES}$,$\overline{RD}$,$\overline{WR}$,C86,SI, SCL,P/$\overline{S}$,T1,T2,D_0~D_7 Ta=25 °C			10		pF	
Oscillation Frequency	fosc	Ta=25 °C	V_{DD}=3.0V	T.B.D.	16	T.B.D.	kHz	

Voltage Tripler	Input Voltage	V_{DD1}	V_{DD}-V_{SS}	2.4		5.5	V	
		V_{DD2}	V_{DD}-V_{SS}, used Quadrupler	2.4		3.3		10
	Output Volt.	V_{OUT}	V_{SS}-V_{LCD} ,used Quadrupler	-9.9			V	
	ON -Resistance	R_{STEP}	V_{DD}=3V, C=4.7uF used Quadrupler		930	1200	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Tripler Circuit "OFF"	V_{DD}-13.5		V_{DD}-5.0	V	11
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"	V_{DD}-13.5		V_{DD}-5.0	V	
	Operating Current	I_{OUT1}	V_{DD}=3.3V, V_{LCD}=8V	T.B.D.	T.B.D.	T.B.D.	uA	12
		I_{OUT2}	COM/SEG Term Open, No Access	T.B.D.	T.B.D.	T.B.D.		
		I_{OUT3}	Display check. pattern	T.B.D.	T.B.D.	T.B.D.		
	Voltage Reg.	V_{REG}	V_{DD}=3.0V, Ta=25 °C			3.0	%	13

Note 5) NJU6577 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D_0 to D_7 terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1,V_2,V_3,V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set"

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 10) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

Note 12) Each operating current of voltage supply circuits block is specified under below table conditions. (V_{DD}=3.3V ; V_{LCD}=8V ; COM/SEG Terminals Open ; No Access ; display checkered pattern)

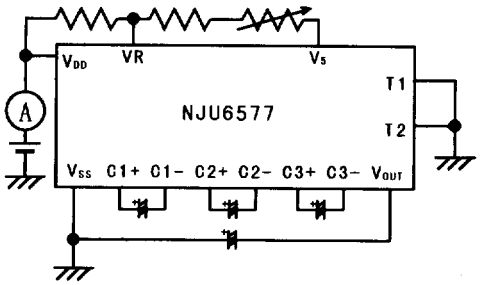
SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T_1	T_2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT},V_5)

* = Don't Care

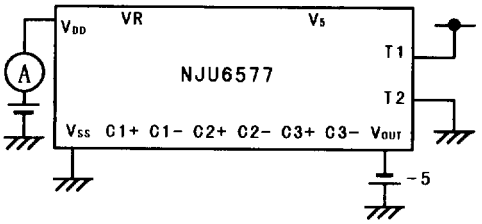
Note 13) Apply to the precision of the voltage between V_{DD} and V_5 with EVR function.

■ MEASUREMENT BLOCK DIAGRAM

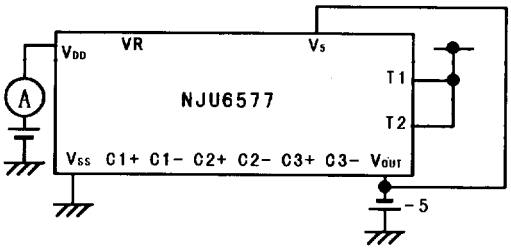
: I_{OUT1}



: I_{OUT2}



: I_{OUT3}



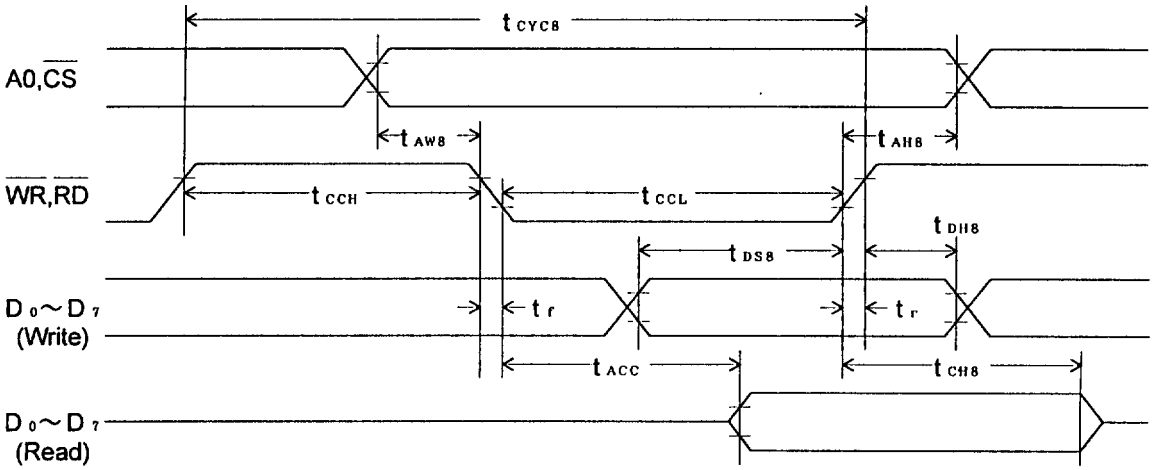
■ ELECTRICAL CHARACTERISTICS (3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	15

Note 14) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 15) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

■ BUS TIMING CHARACTERISTICS

・ Read/Write operation sequence (80 Type MPU)



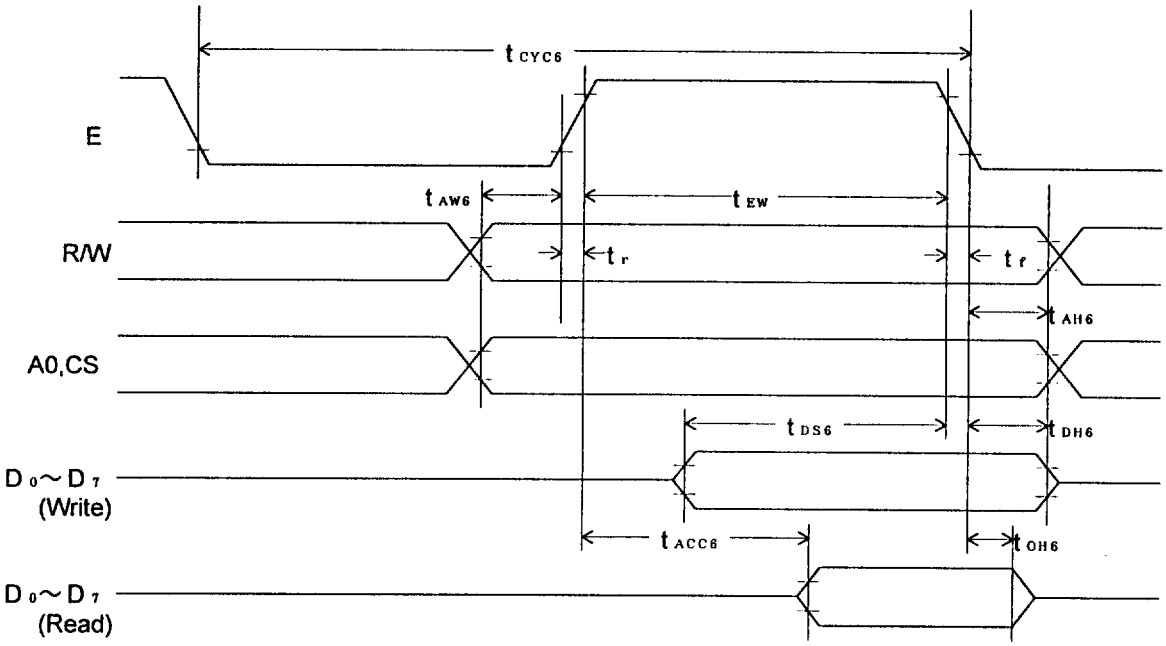
5

(V_{DD}=3.0V±10%, Ta=-20～75°C)

PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, CS Terminals	t_{AH8}	25			ns
Address Set Up Time			t_{AW8}	25			
System Cycle Time		WR, RD Terminals	t_{CYC8}	450			
Control Pulse Width	WR, "L"		t_{CCL}(W)	50			
	RD, "L"		t_{CCL}(R)	200			
	"H"		t_{CCH}	220			
Data Set Up Time		D0～D7 Terminals	t_{DS8}	120			
Data Hold Time			t_{DH8}	35			
RD Access Time			t_{ACC8}		140	CL=100pF	
Output Disable Time			t_{CH8}	0	35		
Rise Time, Fall Time		CS, WR, RD, A0, D0～D7 Terminals	t_r, t_f		15		

Note 16) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 17) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

・ Read/Write operation sequence (68 Type MPU)

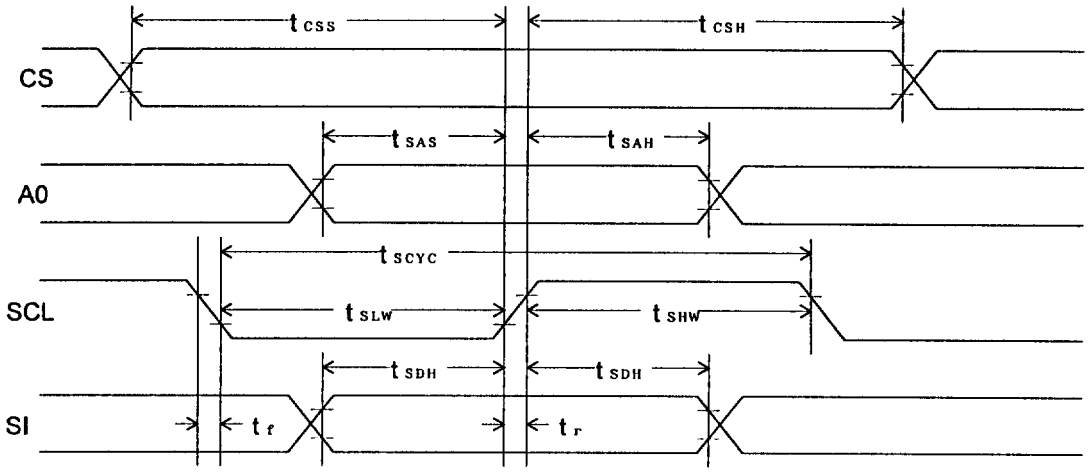


(VDD=3.0V±10%, Ta=-20～75°C)

PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, CS, R/W Terminals	tAH6	25			ns
Address Set Up Time			tAW6	25			
System Cycle Time			tCYC6	450			
Enable Pulse Width	Read	E Terminal	tEW	200			
	Write			50			
Data Set Up Time		D0～D7 Terminals	tDS6	120			
Data Hold Time			tDH6	40			
Access Time			tACC6		140	CL=100pF	
Output Disable Time			tCH6	0	45		
Rise Time, Fall Time		A0, CS, R/W, E, D0～D7 Terminals	tr, tf		15		

Note 18) tCYCE indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.
Note 19) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 20) Each timing is specified based on 0.2xVDD and 0.8xVDD.

· Write operation sequence (Serial Interface)



(VDD=3.0V±10%, Ta=−20～75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC	1000			ns
SCL "H" pulse width		tSHW	300			
SCL "L" pulse width		tSLW	300			
Address Set Up Time	A0 Terminal	tSAS	250			
Address Hold Time		tSAH	400			
Data Set Up Time	SI Terminal	tSDS	250			
Data hold Time		tSDH	100			
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	tCSS	60			
		tCSH	800			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	tr, tf		15		

Note 21) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 22) Each timing is specified based on 0.2xVDD and 0.8xVDD.

■ LCD DRIVING WAVEFORM

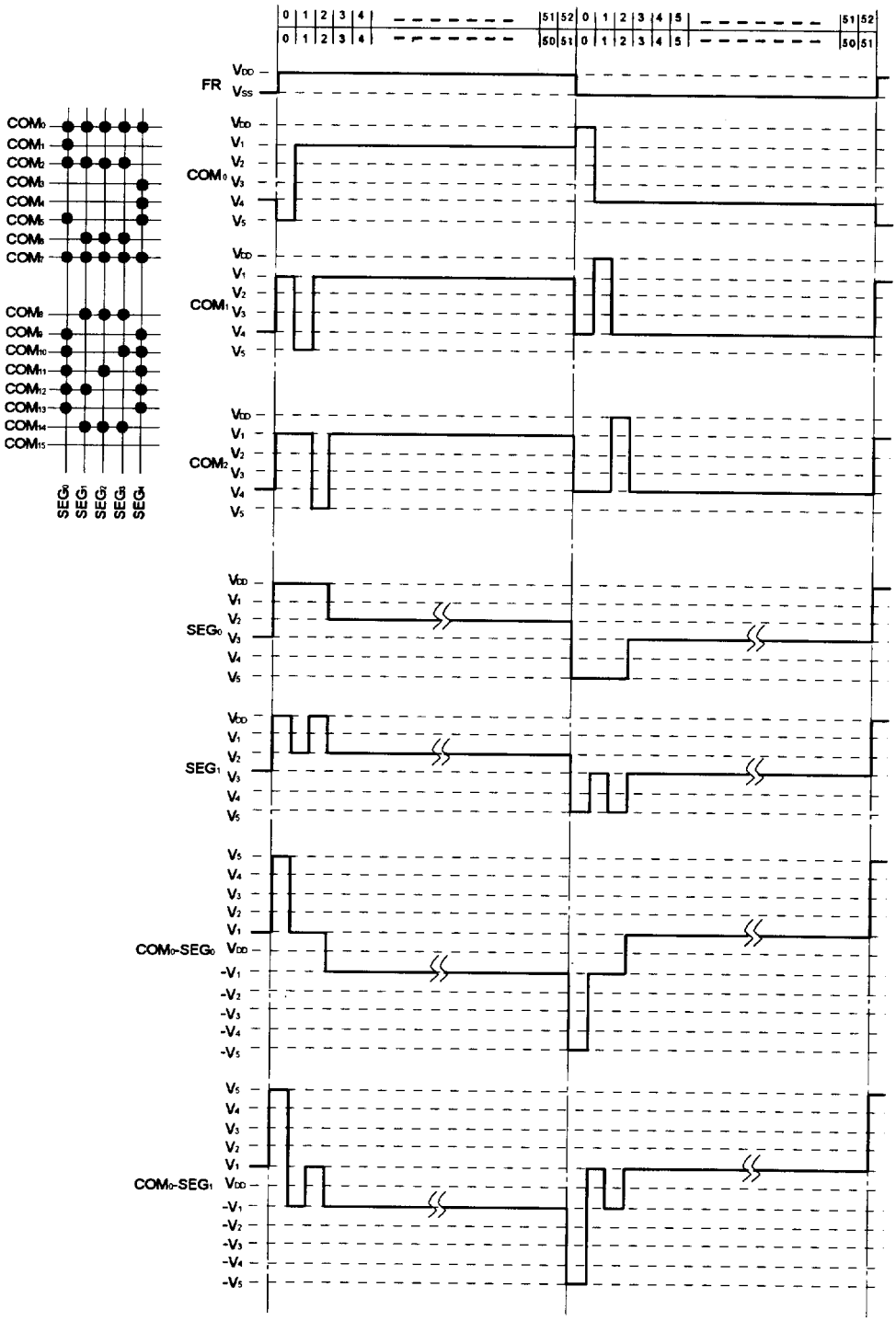


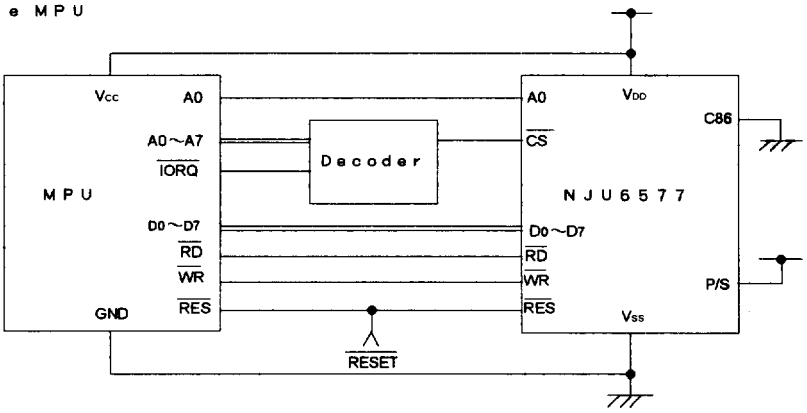
Fig.7

■ APPLICATION CIRCUIT

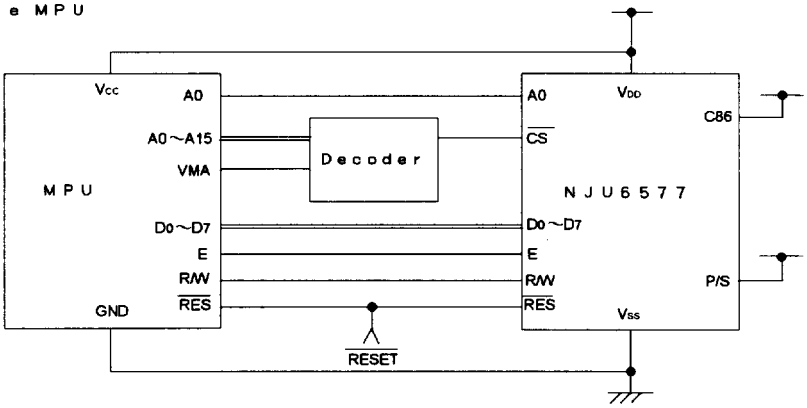
·Microprocessor Interface Example

The NJU6577 can interface with both of 80 type and 68 type MPU by the serial format directly.
Therefore minimum wiring for the MPU interface is available.

●80 Type MPU



●68 Type MPU



●Serial Interface