PRELIMINARY

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6575 is a bit map LCD driver to display graphics or characters.

It contains 4,422 bits display data RAM, microprocessor interface circuits, instruction decoder, 134-segment and 33-common (1 out of 33-driver is prepared for icon display) drivers.

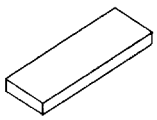
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel mode.

33 x 134 dots graphics or 8-character 2-line by 16 x 16 dot character with icon are displayed by NJU6575 itself.

The wide operating voltage like as 2.4V t o 5.5V and low operating current are useful to apply small sized battery operated items.

The rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE

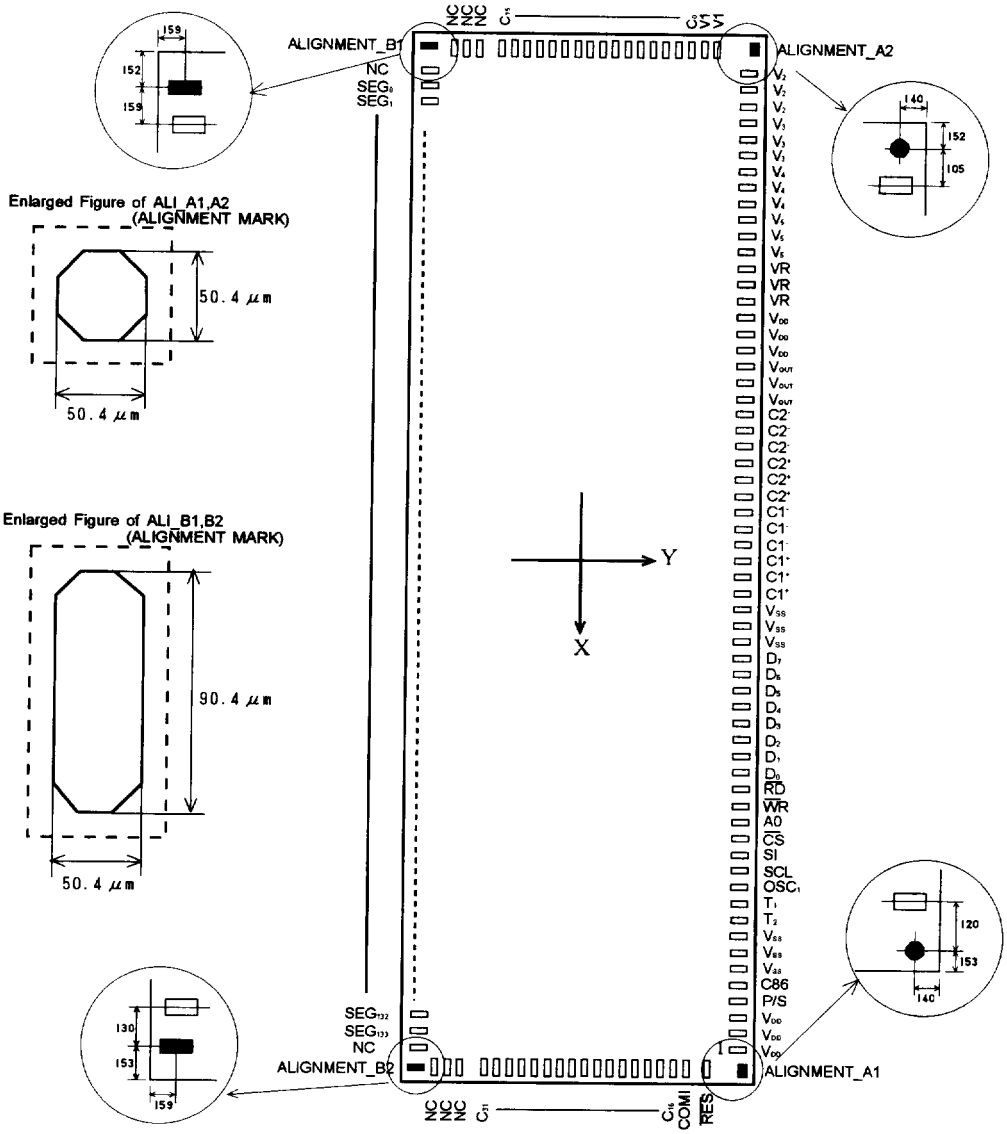


NJU6575C

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 4,422 bits
- 167 LCD Drivers - 33- common and 134-segment
- Direct Interface with both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/32 or 1/33 Duty
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V ~ 5.5V
- LCD Driving Voltage --- 6.0V ~ 13.5V
- Package Outline --- Chip / Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip	Center	X=0um, Y=0um
Chip	Size	X=11.49mm, Y=2.44mm
Chip	Thickness	400um ± 30um
Bump	Size	50um x 110um
Bump	Height	25um TYP.
Bump	Material	Au

■ : Four PADs illustrated with this mark are the alignment marks for COG.

■ PAD COORDINATES

Chip Size 11.49mm x 2.44mm(Chip Center X=0um,Y=0um)

NO.	Termi.	X= μm	Y= μm
1	V_{DD}	5472	1054
2	V_{DD}	5392	1054
3	V_{DD}	5312	1054
4	P/S	5232	1054
5	C86	5152	1054
6	V_{SS}	5072	1054
7	V_{SS}	4992	1054
8	V_{SS}	4912	1054
9	T_2	4832	1054
10	T_1	4752	1054
11	OSC_1	4672	1054
12	SCL	4592	1054
13	SI	4192	1054
14	$\overline{CS}$	3792	1054
15	A0	3392	1054
16	$\overline{WR}$	2992	1054
17	$\overline{RD}$	2592	1054
18	D_0	2192	1054
19	D_1	1792	1054
20	D_2	1392	1054
21	D_3	992	1054
22	D_4	592	1054
23	D_5	192	1054
24	D_6	-208	1054
25	D_7	-608	1054
26	V_{SS}	-928	1054
27	V_{SS}	-1008	1054
28	V_{SS}	-1088	1054
29	C1	-1328	1054
30	C1	-1408	1054
31	C1	-1488	1054
32	C1	-1728	1054
33	C1	-1808	1054
34	C1	-1888	1054
35	C2	-2128	1054
36	C2	-2208	1054
37	C2	-2288	1054
38	C2	-2528	1054
39	C2	-2608	1054
40	C2	-2688	1054
41	V_{OUT}	-2928	1054
42	V_{OUT}	-3008	1054
43	V_{OUT}	-3088	1054
44	V_{DD}	-3328	1054
45	V_{DD}	-3408	1054
46	V_{DD}	-3488	1054
47	VR	-3728	1054
48	VR	-3808	1054
49	VR	-3888	1054
50	V_6	-4128	1054

No.	Termi.	X= μm	Y= μm
51	V_5	-4208	1054
52	V_5	-4288	1054
53	V_4	-4528	1054
54	V_4	-4608	1054
55	V_4	-4688	1054
56	V_3	-4928	1054
57	V_3	-5008	1054
58	V_3	-5088	1054
59	V_2	-5328	1054
60	V_2	-5408	1054
61	V_2	-5488	1054
62	V_1	-5584	862
63	V_1	-5584	782
64	C_0	-5584	702
65	C_1	-5584	622
66	C_2	-5584	542
67	C_3	-5584	462
68	C_4	-5584	382
69	C_5	-5584	302
70	C_6	-5584	222
71	C_7	-5584	142
72	C_8	-5584	62
73	C_9	-5584	-18
74	C_{10}	-5584	-98
75	C_{11}	-5584	-178
76	C_{12}	-5584	-258
77	C_{13}	-5584	-338
78	C_{14}	-5584	-418
79	C_{15}	-5584	-498
80	NC	-5584	-634
81	NC	-5584	-770
82	NC	-5584	-906
83	NC	-5434	-1055
84	SEG_0	-5306	-1055
85	SEG_1	-5226	-1055
86	SEG_2	-5146	-1055
87	SEG_3	-5066	-1055
88	SEG_4	-4986	-1055
89	SEG_5	-4906	-1055
90	SEG_6	-4826	-1055
91	SEG_7	-4746	-1055
92	SEG_8	-4666	-1055
93	SEG_9	-4586	-1055
94	SEG_{10}	-4506	-1055
95	SEG_{11}	-4426	-1055
96	SEG_{12}	-4346	-1055
97	SEG_{13}	-4266	-1055
98	SEG_{14}	-4186	-1055
99	SEG_{15}	-4106	-1055
100	SEG_{16}	-4026	-1055

No.	Termi.	X= μm	Y= μm
101	SEG_{17}	-3946	-1055
102	SEG_{18}	-3866	-1055
103	SEG_{19}	-3786	-1055
104	SEG_{20}	-3706	-1055
105	SEG_{21}	-3626	-1055
106	SEG_{22}	-3546	-1055
107	SEG_{23}	-3466	-1055
108	SEG_{24}	-3386	-1055
109	SEG_{25}	-3306	-1055
110	SEG_{26}	-3226	-1055
111	SEG_{27}	-3146	-1055
112	SEG_{28}	-3066	-1055
113	SEG_{29}	-2986	-1055
114	SEG_{30}	-2906	-1055
115	SEG_{31}	-2826	-1055
116	SEG_{32}	-2746	-1055
117	SEG_{33}	-2666	-1055
118	SEG_{34}	-2586	-1055
119	SEG_{35}	-2506	-1055
120	SEG_{36}	-2426	-1055
121	SEG_{37}	-2346	-1055
122	SEG_{38}	-2266	-1055
123	SEG_{39}	-2186	-1055
124	SEG_{40}	-2106	-1055
125	SEG_{41}	-2026	-1055
126	SEG_{42}	-1946	-1055
127	SEG_{43}	-1866	-1055
128	SEG_{44}	-1786	-1055
129	SEG_{45}	-1706	-1055
130	SEG_{46}	-1626	-1055
131	SEG_{47}	-1546	-1055
132	SEG_{48}	-1466	-1055
133	SEG_{49}	-1386	-1055
134	SEG_{50}	-1306	-1055
135	SEG_{51}	-1226	-1055
136	SEG_{52}	-1146	-1055
137	SEG_{53}	-1066	-1055
138	SEG_{54}	-986	-1055
139	SEG_{55}	-906	-1055
140	SEG_{56}	-826	-1055
141	SEG_{57}	-746	-1055
142	SEG_{58}	-666	-1055
143	SEG_{59}	-586	-1055
144	SEG_{60}	-506	-1055
145	SEG_{61}	-426	-1055
146	SEG_{62}	-346	-1055
147	SEG_{63}	-266	-1055
148	SEG_{64}	-186	-1055
149	SEG_{65}	-106	-1055
150	SEG_{66}	-26	-1055

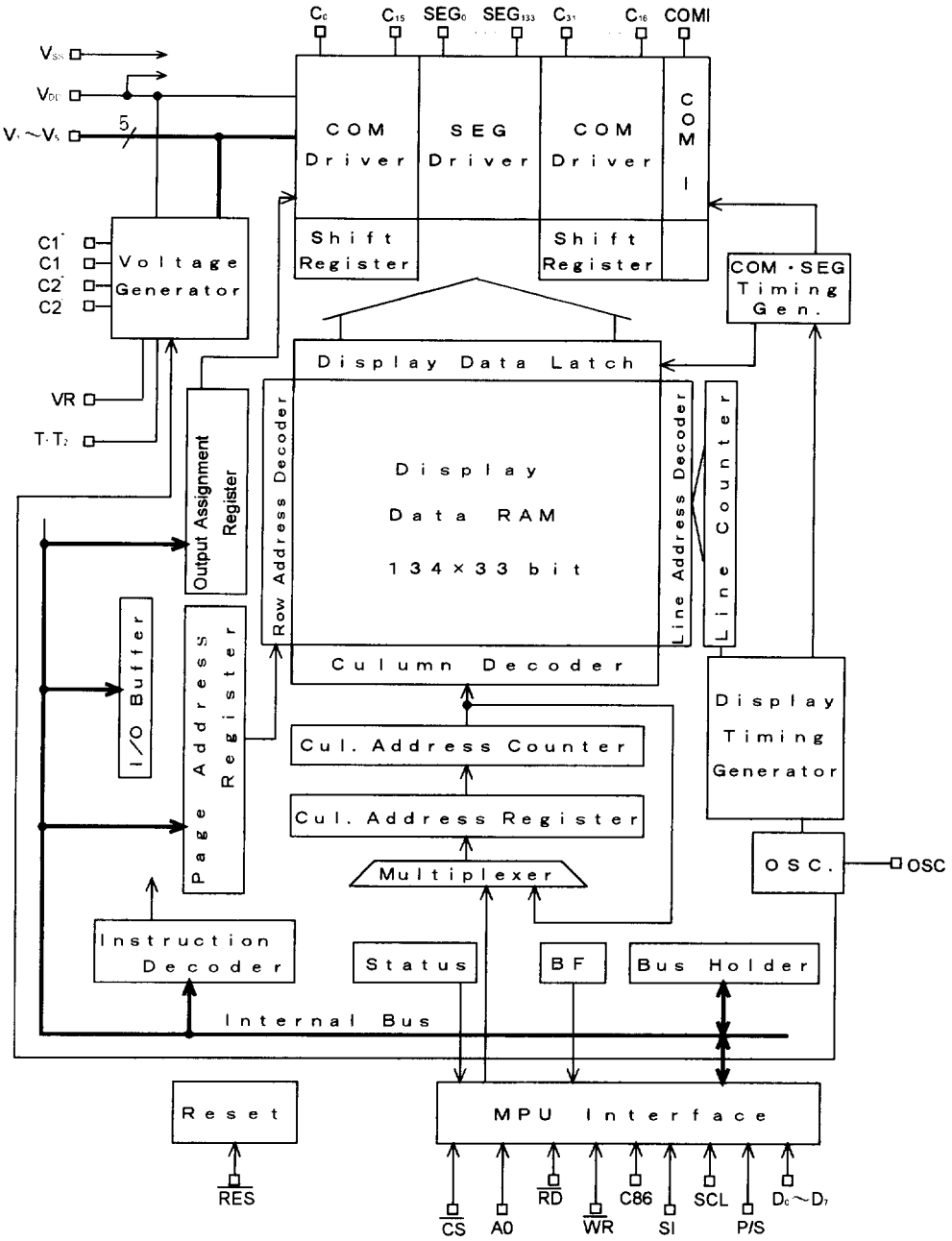
5

No.	Terminal	X= μm	Y= μm
151	SEG_{67}	54	-1055
152	SEG_{68}	134	-1055
153	SEG_{69}	214	-1055
154	SEG_{70}	294	-1055
155	SEG_{71}	374	-1055
156	SEG_{72}	454	-1055
157	SEG_{73}	534	-1055
158	SEG_{74}	614	-1055
159	SEG_{75}	694	-1055
160	SEG_{76}	774	-1055
161	SEG_{77}	854	-1055
162	SEG_{78}	934	-1055
163	SEG_{79}	1014	-1055
164	SEG_{80}	1094	-1055
165	SEG_{81}	1174	-1055
166	SEG_{82}	1254	-1055
167	SEG_{83}	1334	-1055
168	SEG_{84}	1414	-1055
169	SEG_{85}	1494	-1055
170	SEG_{86}	1574	-1055
171	SEG_{87}	1654	-1055
172	SEG_{88}	1734	-1055
173	SEG_{89}	1814	-1055
174	SEG_{90}	1894	-1055
175	SEG_{91}	1974	-1055
176	SEG_{92}	2054	-1055
177	SEG_{93}	2134	-1055
178	SEG_{94}	2214	-1055
179	SEG_{95}	2294	-1055
180	SEG_{96}	2374	-1055
181	SEG_{97}	2454	-1055
182	SEG_{98}	2534	-1055
183	SEG_{99}	2614	-1055
184	SEG_{100}	2694	-1055
185	SEG_{101}	2774	-1055
186	SEG_{102}	2854	-1055
187	SEG_{103}	2934	-1055
188	SEG_{104}	3014	-1055
189	SEG_{105}	3094	-1055
190	SEG_{106}	3174	-1055
191	SEG_{107}	3254	-1055
192	SEG_{108}	3334	-1055
193	SEG_{109}	3414	-1055
194	SEG_{110}	3494	-1055
195	SEG_{111}	3574	-1055
196	SEG_{112}	3654	-1055
197	SEG_{113}	3734	-1055
198	SEG_{114}	3814	-1055
199	SEG_{115}	3894	-1055

No.	Terminal	X= μm	Y= μm
200	SEG_{116}	3974	-1055
201	SEG_{117}	4054	-1055
202	SEG_{118}	4134	-1055
203	SEG_{119}	4214	-1055
204	SEG_{120}	4294	-1055
205	SEG_{121}	4374	-1055
206	SEG_{122}	4454	-1055
207	SEG_{123}	4534	-1055
208	SEG_{124}	4614	-1055
209	SEG_{125}	4694	-1055
210	SEG_{126}	4774	-1055
211	SEG_{127}	4854	-1055
212	SEG_{128}	4934	-1055
213	SEG_{129}	5014	-1055
214	SEG_{130}	5094	-1055
215	SEG_{131}	5174	-1055
216	SEG_{132}	5254	-1055
217	SEG_{133}	5334	-1055
218	NC	5462	-1055
219	NC	5583	-913
220	NC	5583	-777
221	NC	5583	-641
222	C_{31}	5583	-505
223	C_{30}	5583	-425
224	C_{29}	5583	-345
225	C_{28}	5583	-265
226	C_{27}	5583	-185
227	C_{26}	5583	-105
228	C_{25}	5583	-25
229	C_{24}	5583	56
230	C_{23}	5583	136
231	C_{22}	5583	216
232	C_{21}	5583	296
233	C_{20}	5583	376
234	C_{19}	5583	456
235	C_{18}	5583	536
236	C_{17}	5583	616
237	C_{16}	5583	696
238	COMI	5583	776
239	$\overline{RES}$	5583	856
ALIGNMENT	A1	5592	1080
ALIGNMENT	A2	-5593	1080
ALIGNMENT	B1	-5593	-1061
ALIGNMENT	B2	5592	-1061

5

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function
1,2,3, 44,45,46	V_{DD}	Power	V_{DD} =+5V. (Less than 4.5V should apply when voltage tripler using.)
6,7,8 26,27,28	V_{SS}	GND	V_{SS} =0V
62,63 59,60,61 56,57,58 53,54,55 50,51,52	V_1 V_2 V_3 V_4 V_5	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ When internal power supply is on, internal circuits generated and supply following LCD bias voltage to $V_1 \sim V_4$ terminals. Term. | V_1 | V_2 | V_3 | V_4 Volt. | $V_5+4/5V_{LCD}$ | $V_5+3/5V_{LCD}$ | $V_5+2/5V_{LCD}$ | $V_5+1/5V_{LCD}$ ($V_{LCD}=V_{DD}-V_5$)
29,30,31 32,33,34 35,36,37 38,39,40	$C1^+$ $C1^-$ $C2^+$ $C2^-$	O	Step up capacitor connecting terminals. In case of tripler operation, connect the capacitor between $C1^+$ and $C1^-$, $C2^+$ and C2 . In case of doubler operation, connect the capacitor between $C2^+$ and $C2^-$, connect $C2^+$ to $C1^+$, and $C1^-$ should be open.
41,42,43	V_{OUT}	O	Step up voltage output terminal. Connect the set up capacitor between this terminal and V_{SS}.
47,48,49	VR	I	Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance connect between V_{DD} and V5 terminal.
10 9	T_1 T_2	I	LCD bias voltage control terminals. ※ Don't Care T_1 | T_2 | Step up cir. | Voltage Adj. | V/F Cir. L | ※ | Available | Available | Available H | L | Not Avail. | Available | Available H | H | Not Avail. | Not Avail. | Available
18 ~ 25	$D_0 \sim D_7$	I/O	Tri-state bilateral Data I/O terminal when 8-bit parallel operation.
15	A0	I	Connect to the Address bus of MPU. The data on the D_0 to D_7 is distinguished Display data or Instruction by this signal. A0 | H | L Dist. | Display Data | Instruction
239	$\overline{RES}$	I	Reset terminal. When the $\overline{RES}$ terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of $\overline{RES}$.
14	$\overline{CS}$	I	Chip select terminal. Data Input/Output are available during $\overline{CS}$ ="L".
17	$\overline{RD}$ (E)	I	<When interface with 80 type MPU> $\overline{RD}$ signal of 80 type MPU input terminal. Active"L". During this signal "L", the data bus becomes as output terminal. <When interface with 68 type MPU> Enable clock of 68 type MPU input terminal. Active "H".

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No.	Symbol	I/O	Function
16	$\overline{WR}$ (R/$\overline{W}$)	I	<When interface with 80 type MPU> · Connect the 80 type MPU $\overline{WR}$ signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal. <When interface with 68 type MPU> Read/write control signal of 68 type MPU input terminal. R/$\overline{W}$: H = Read, L = Write
5	C86	I	Select the MPU interface type. C86: H = 68 Type, L = 80 Type
13	SI	I	Serial data input terminal .
12	SCL	I	Serial data clock signal input terminal. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.
4	P/S	I	Serial or parallel interface select terminal. P/S="H": Chip Select $\overline{CS}$, Data/Command A0, Data D_0 ~ D_7, Read/Write $\overline{RD}$、$\overline{WR}$, Serial CLK — P/S="L": Chip Select $\overline{CS}$, Data/Command A0, Data SI, Read/Write Write only, Serial CLK SCL *RAM data and status read operation is impossible when select the serial interface. · When select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L". · When select the serial interface (P/S="L"), $\overline{RD}$ and $\overline{WR}$ must be fix "H" or "L", and D_0 ~ D_7 becomes to the high impedance state.
11	OSC 1	I	System clock input terminal for Maker testing. This terminal should be open.

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<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>64 ~ 79</td><td>C_0 ~ C_{15}</td><td>O</td><td>LCD drive output terminals.
Segment output terminals : SEG_0 to SEG_{133}
Common output terminals :C_0 to C_{32}

・ Segment output terminal
Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM.
<table><tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal</th><th>Reverse</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr><tr><td>L</td><td>V_5</td><td>V_3</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr><tr><td>L</td><td>V_3</td><td>V_5</td></tr></table>
・ Common Output Terminal
Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data.
<table><tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr><tr><td>L</td><td>V_{DD}</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr><tr><td>L</td><td>V_4</td></tr></table></td></tr>
<tr><td>84 ~ 217</td><td>SEG_0 ~ SEG_{133}</td><td></td><td></td></tr>
<tr><td>222 ~ 237</td><td>C_{31} ~ C_{16}</td><td></td><td></td></tr>
<tr><td>238</td><td>COMI</td><td>O</td><td>Icon common output terminal.
Icon common output when Icon Display instruction execution.
<table><tr><th></th><th>Icon Display ON</th><th>Icon Display OFF</th></tr><tr><td>State</td><td>COM_{32}</td><td>V_1 or V_4</td></tr></table></td></tr>
</table>

(Terminals 80,81,82,83,218,219,220,221 are NC)

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■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode. the busy flag(BF) is "1", and any instruction except the status read are inhibited .

The busy flag output from D_7 terminal when status read instruction is executed.

If enough cycle time over then t_{cyc} indicated in the bus timing characteristics is kept, no need to check the busy flag and it realized high performance for the MPU.

(1-2) Line Counter

The Line Counter is reset at the FR signal changing and counts up by synchronizing common signal cycle and generate the line address which addressing the read out line of Display Data RAM.

(1-3) Column Address Counter

The column address counter is 8-bit presentable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to $(A0)_H$ when the Display Data Read/Write instruction is executed. The count up is stop at $(A0)_H$, do not count up non existing address of over than $(A0)_H$ by the count lock function. This count lock is released by new column address set.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM correspondence to the Segment Driver.

(1-4) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the data by changing the page, the page address set instruction is required. Page address "4"(D_2 ="H" and D_1 =D_0 ="L") is Icon RAM area, the data only for the D_0 is valid.

(1-5) Display Data RAM

Display Data RAM consists of 4,422 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM output 134 bit parallel data addressed by the line counter, and these data are set into the Display Data Latch.

This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize rewriting.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.

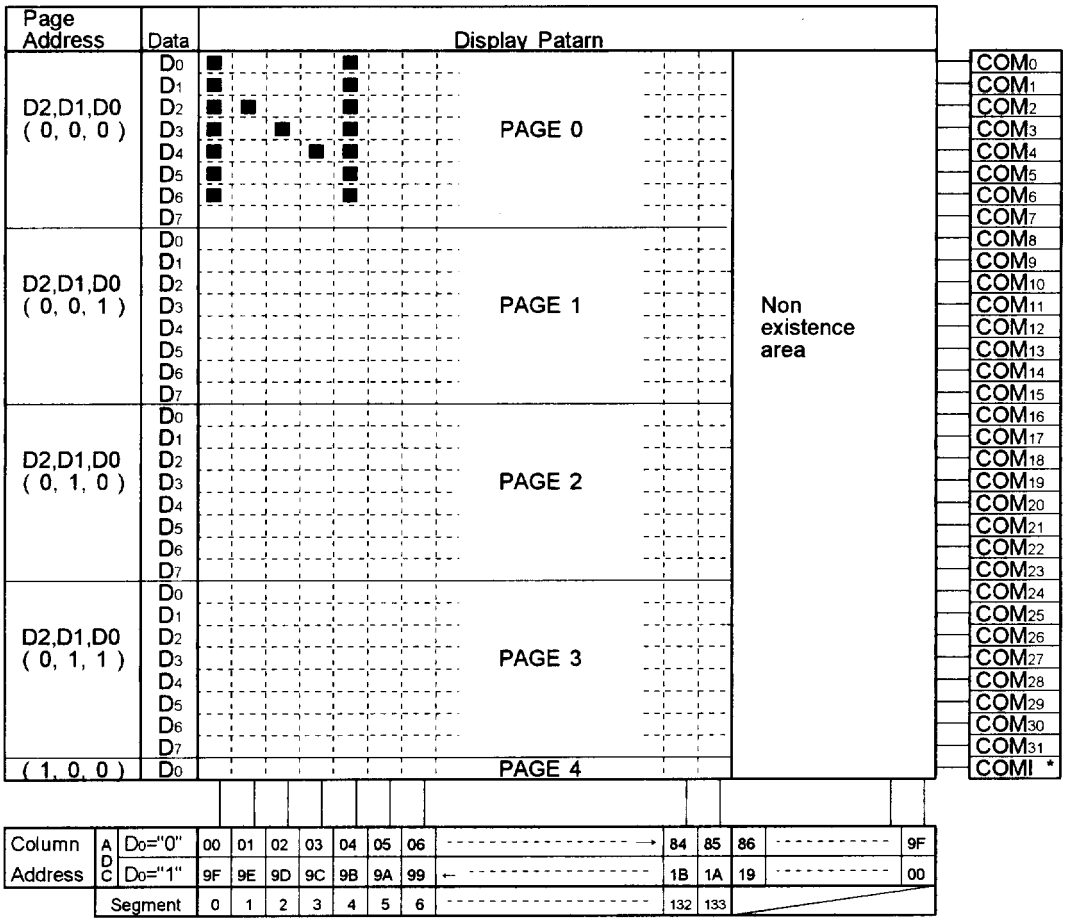


Fig.1 Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/33 duty set.)

* When readout the Display Data RAM address 86H to 9FH in normal ADC or 00H to 19H in inverse ADC the data FFH is output as those address data.

(1-6) Common and Segment Driver Assignment

The scanning order can be assigned by setting A_3 of the Output Assignment Register as shown Table 1.

The location of Segment Drivers are fixed at any time.

Table 1

Register	PAD No.	COM Output Terminals			
		64	79	222	237
A3	Pin name	C_0	C_{15}	C_{31}	C_{16}
0	→	COM_{15} ←	COM_0	COM_{16} →	COM_{31}
1	→	COM_{16} →	COM_{31}	COM_{15} ←	COM_0

The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COMI is fixed to COM_{32} timing regardless the other Common Driver assignment.

(1-7) Reset Circuits

The NJU6575 performs following initialization when the $\overline{RES}$ input is put on the "L" level.

Initialization

① Display Off
② Normal Display(Non-inverse display)
③ Icon Display Reset
④ ADC Select : Normal (ADC Instruction D_0 ="0")
⑤ Read Modify Write Mode Off
⑥ Internal Power supply(Step up) circuits Off
⑦ Clear the serial interface register
⑧ Set the address $(00)_H$ to the Column Address Counter
⑨ Set the page "0" to the Page Address Register
⑩ Select the D_3 of the Output Assignment Register to "0"
⑪ Set the EVR register to $(00)_H$

The $\overline{RES}$ terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface Example". The reset signal require over than 10us $\overline{RES}$= "L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{RES}$ signal, the normal operation is starting.

In case of the internal power supply(Step up) circuits do not use, the $\overline{RES}$ terminal must be "L" when external power supply turn on. RES="L" input reset internal register and set above default, but oscillation circuits and output terminals like as D_0 through D_7 are no influence.

No initialization by $\overline{RES}$ when power turns on, will make Hung up condition, therefore please initialize by the $\overline{RES}$ when power turns on. By the reset Instruction performs only ⑧ through ⑪ mentioned in above.

The noise into the $\overline{RES}$ terminal should be cared when of the application design to avoid the error function.

(1-8) LCD Driving

(a) LCD Driving Circuits

NJU6575 incorporates 167 LCD Drivers like as 134 Segment drivers, 32 Common drivers and 1 Icon common driver. 32 Common drivers incorporate the shift register which scanning the common display signal. The combination among the Display data, COM scan signal and FR signal define the LCD driving output voltage. The output wave form is mentioned in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 134-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver. The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits

The clock for Line Counter and latch signal for the Latch Circuits are generated from display clock(CL). The line address is renewed by synchronizing with display clock and 134 bits display data are latched into display latch circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR has a function to generate the two frame alternative driving method waveform for the LCD panel.

5

(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

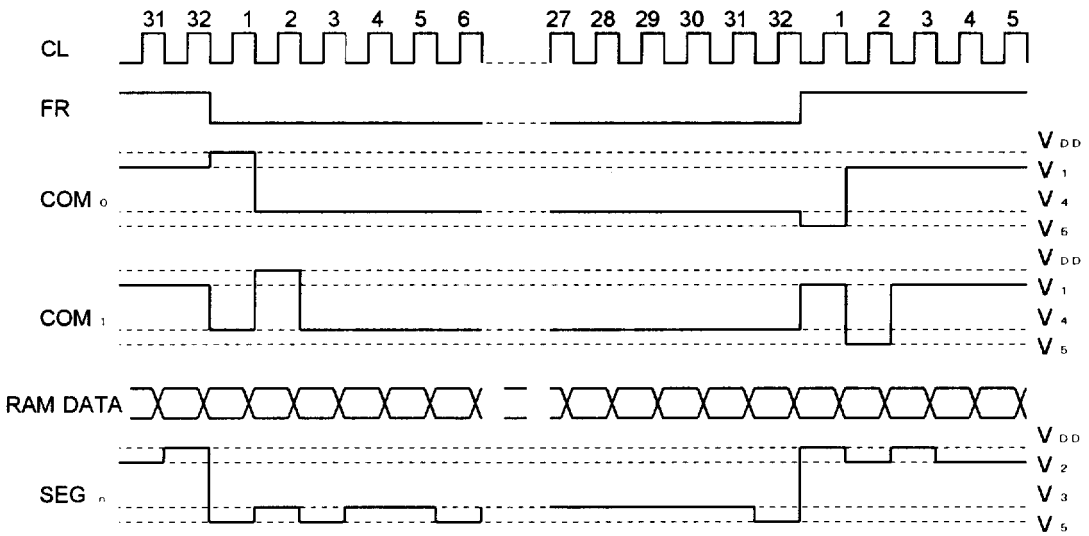


Fig. 2 Waveform of Display Timing

(f) Oscillation Circuits

The Oscillation Circuits which incorporates the oscillating resistance R and capacitor C, is a low power CR oscillator and it is used as display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuits output frequency is divided by 8 which is used as display clock CL.

(g) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Tripler or Doubler) Circuits, Regulation Circuits, and Voltage Follower. Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the large size LCD panel application. If the contrast is no good in those application, please use external power supply supplied more high current.

The suitable values of the capacitors connecting to the V1 to V5 terminals, the step up circuit and the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption in the LCD panel is changeable with the display patarn. Therefore a trial with actual module should be practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, voltage follower circuits are off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD supply from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$,and VR are open. The status of internal power supply can select by T_1 and T_2 terminal. The external power supply can be used together with some of internal power supply function.

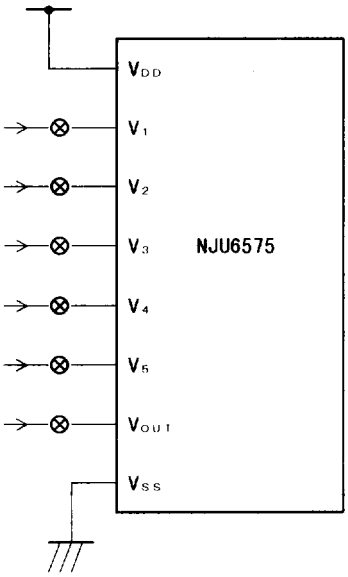
Table 3. (*:Don't Care)

T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term.
L	*	O	O	O	-		
H	L	×	O	O	V_{OUT}	OPEN	
H	H	×	×	O	V_5, V_{OUT}	OPEN	OPEN

When (T_1, T_2)=(H, L), the terminal for step up circuits of $C1^+$,$C1^-$ $C2^+$,$C2^-$ are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T_1, T_2)=(H, H), terminals for step up circuits and VR are open, and supply the LCD driving voltage from outside due to the Step up circuits and Voltage adjust circuits are stop its operation.

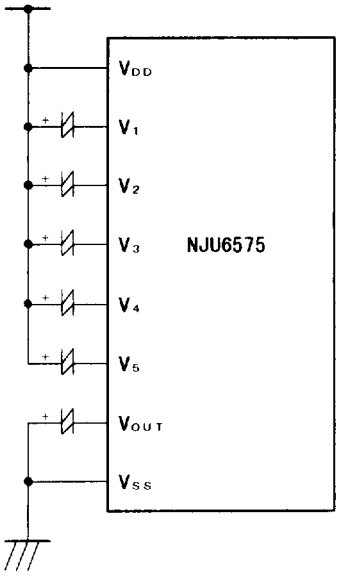
○ Examples for application circuits of the internal Power Supply

(1)None of the internal power supply functions.



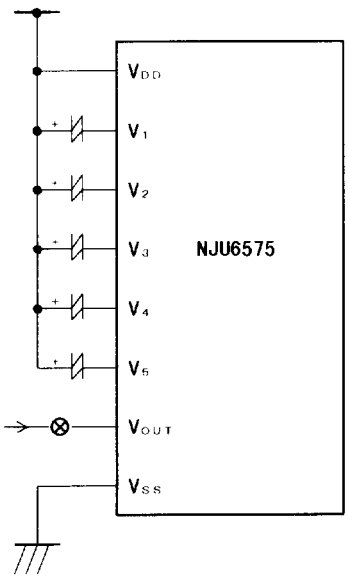
(2) All of the internal power supply functions.
(Step up, Voltage Adj., Buffer(V/F))

(T1, T2) = (L, *) *: Don't care.



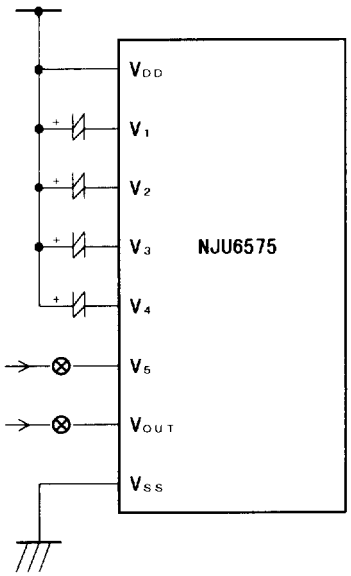
(3)Some of the internal power supply functions.
(Voltage Adjust., Buffer(V/F))

(T1,T2) = (H,L)



(4)Some of the internal power supply functions.
(Buffer(V/F))

(T1,T2) = (H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6575 distinguish the signal on the data bus by combination of A0,$\overline{RD}$ and $\overline{WR}$. Normally, the busy check is not required as the NJU6575 is operating so first because of the decode of the instruction and execution are performs only depend on the internal timing which not depend on the external clock. In case of serial interface, the data input as MSB first serially.

The Table. 4 shows the instruction codes of the NJU6575.

Table 4. Instruction Code

Instruction		Code A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Add. Register
(3)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								Read the Data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0 1	Inverse the On and Off Display 0:Normal 1:Inverse
(10)	Whole Display On /Normal Display	0	1	0	1	0	1	0	0	1	0	0 1	Whole Display Turns On 0:Normal 1:Whole Disp. On
(11)	Icon Display	0	1	0	1	0	1	0	1	0	1	0 1	Set the Duty Ratio 0:No Icon 1:With Icon
(12)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(15)	Output Assignment Register Set	0	1	0	1	1	0	0	A_3	*	*	*	Set the scanning order of common drivers to the Register
(16)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0 1	0:Int. Power Supply Off 1:Int. Power Supply On
(17)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal(external) power supply is turned on
(18)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V_5 output level to the EVR register
(19)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power save Mode

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7							D_0
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 4 is a Icon display data area which available only for the D_0.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7							D_0
0	1	0	1	0	1	1	*	A_2	A_1	A_0

(*:Don't Care)

A_2	A_1	A_0	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

5

(c) Column Address

When MPU access the Display Data RAM, page address set(refer(b) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting.

After writing 1page data ,page address setting is required due to page address doesn't increase automatically.

The increment of the column address is stopped by the address of $(A0)_H$ automatically, or the page address is no change even if the column address increase to $(A0)_H$ and stop. In this time the page address is no change.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
Higher Order	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower Order	0	1	0	0	0	0	0	A3	A2	A1	A0

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				.				.
				.				.
1	0	1	0	0	0	0	0	A0

(d) Status Read

This instruction read out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.
0 :Counterclockwise Output(Inverse) Column Address 133-n ←→ Segment Driver n
1 :Clockwise Output (Normal) Column Address n ←→ Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On"
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initialization period by $\overline{RES}$ signal or reset instruction.
0 : —
1 : Initialization Period

(e) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$	D_7 ——— D_0
1	1	0	WRITE DATA

(f) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page address. The column address increase "1" automatically when reading, therefore, the MPU can read the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read is required after column address set as explain in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data can not be readout.

A0	$\overline{RD}$	R/$\overline{W}$	D_7 ——— D_0
1	0	1	READ DATA

(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	0	0	D

D 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Data RAM is no changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"
1: Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction executes the all pixel terns on regardless the contents of the Display Data RAM. In this time, the contents of Display Data RAM is no change and is kept. This instruction takes over precedence over the "Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	1	0	D

D 0: Normal Display
1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the power save mode(refer to the (s) Power Save) .

(j) Icon Display

This instruction set the 1/33 duty for the Icon Display. The COMI terminal operate as COM_{32} and output the icon display data stored in D_0 of Display Data RAM page 4 (refer to the Fig. 1).

A0	$\overline{RD}$	R/$\overline{WR}$	D_7						D_0
0	1	0	1	0	1	0	1	0	1	D

D 0: 1/32 Duty
1: 1/33 Duty

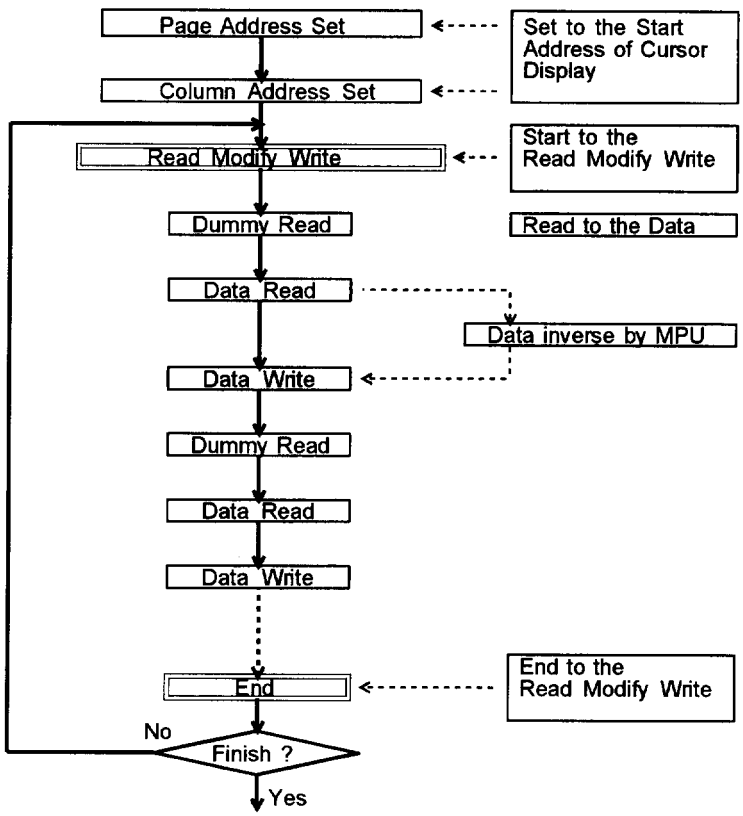
(k) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the Read Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction is executed, but the address is no change when the Display Data Read Instruction is executed. This status is continued during End instruction execution. When the End instruction is entered the column address back to the address where the Read Modify Write instruction entering. By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

A0	$\overline{RD}$	R/$\overline{WR}$	D_7						D_0
0	1	0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

(l) Sequence of inverse display



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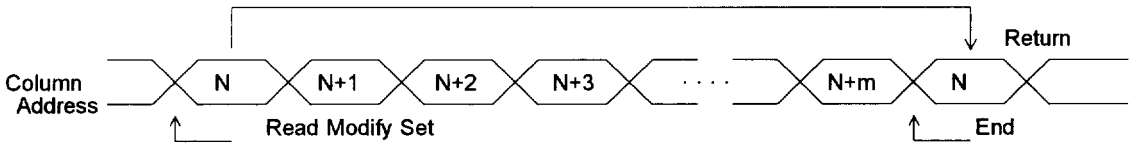
(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	1	0	1	1	0



(n) Reset

This instruction executes the following initialization.

Initialization

① Set the Address (00)$_H$ to the Column Address Counter.
② Set the page "0" to the Page Address Register.
③ Select the D3 of the Output Assignment Register to "0".
④ Set 0 to the EVR Register to (00)$_H$.

In this time, there are no influence to the Display Data RAM.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal must be required for the initialization when the power terns on. Substitution of Reset Instruction for the reset signal input to the $\overline{RES}$ terminal is not allowed.

(o) Output Assignment Register

This instruction sets the common driver scanning order .

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	0	0	A3	*	*	*

(*:Don't Care)

A3: Set the scanning order .(Refer to 1-6)

(p) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is required.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q)LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 to V4 and output LCD driving waveform through the COM/SEG terminals.

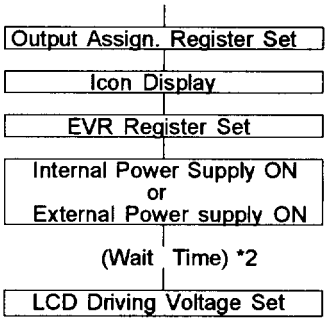
A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	1	0	1	1	0	1

NJU6575 contains operational amplifiers for LCD bias voltage V1 to V4. These amplifiers current are reduced in order to realize low power consumption. Because of this reduction, LCD driving voltage V1 to V4 might be unstable just after the internal power supply is turned on.
LCD Driving Voltage Set instruction is prepared for this unstableness.

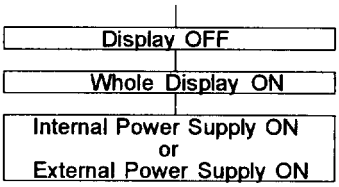
● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is tuned on/of.
When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence mentioned in (s) is required.

Turn ON sequence

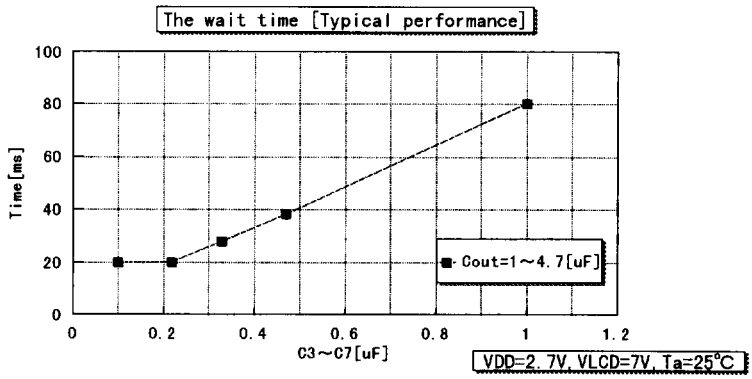


Turn OFF sequence



*1 This instruction is required in both cases of the internal and external power supply.
Until "LCD driving voltage Set" execution, NJU6575 operating current is higher than usual state and all COM/ SEG terminals output V_{DD} level continuously except LCD driving waveform.

*2 The wait time depends on the C_3 to C_7, C_{OUT} capasitors((4) (d)Fig.4), V_{DD} and V_{LCD} voltage.
Therefore a test on actual module should be practiced. Refer to the following graph.



(r) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this instruction execute, the internal Electrical Variable Resistor(EVR) to change the V_5 output voltage, generate one voltage from 16 voltage state. The range of V_5 output level can be adjusted by the external resistance. For more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	0	0	A3	A2	A1	A0

A3	A2	A1	A0	V_{LCD}
0	0	0	0	Low
		:		:
		:		:
1	1	1	1	High

$V_{LCD} = V_{DD} - V_5$

When EVR doesn't use, set the EVR register to (0,0,0,0).

(s) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits put on the power save mode and the operating current is reduced as same as stand by current.
The internal status in the Power Save Mode is as follows;

① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
③ Keeping the display data and operating mode as before the power save mode.
④ All of LCD driving bias voltage fixed to the V_{DD} level.

5

The power save and its release should be performed according to the following sequences.

Power Save Sequence

Display OFF

Whole Display ON

Power Save Release Sequence

Normal Display

Display ON

(Wait Time)

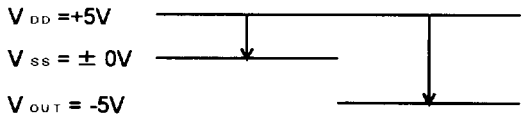
LCD Driving Voltage Set

*1 Power save mode requires dual-instruction. After the second instruction" whole Display ON", the power save mode starts.
*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.
*3 Until "LCD driving voltage set" execution, NJU6575 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.
*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.
*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

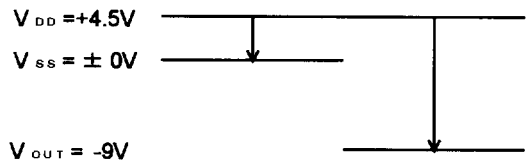
(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage(V_{DD} common) of the voltage V_{DD}-V_{SS} is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT}. In case of the voltage doubler operation, connect the two capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{OUT}, then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 4.5V.



Voltage Relation in Doubler



Voltage relation in Tripler

(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage can calculated by the following formula.

$V_5 = V_{DD} - (1+Rb/Ra) \cdot V_{REG}$ ····· ①

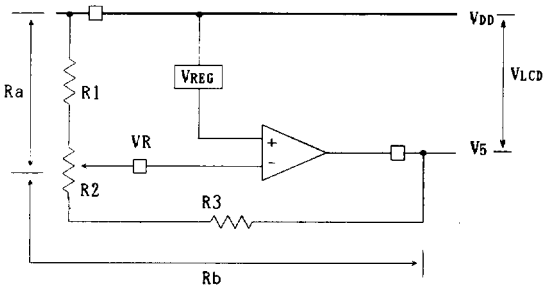


Fig. 3

Where, the V_{REG} is a constant voltage in the NJU6575 like as $V_{REG} \fallingdotseq 2.2V$.

To adjust the output voltage from V_5, connect the variable resistance among VR, V_{DD} and V_5 as shown in Fig. 3. When fine tuning for V_5 is needed, combine with the fixed resistance of R1, R3 and variable resistance of R2 is recommended as shown in Fig. 4.

Design example for R1, R2 and R3(reference)

- R1+R2+R3=5M Ω (Determined by the current flown between V_{DD}-V_5)
- Variable voltage range by the R2. -2.5V ~ -4.5V (V_{DD}-V_5→ 7V ~ 9V)
  (Determined by the LCD electrical characteristics)

R1, R2 and R3 are calculated by above conditions and the formula of ① to mentioned below;

R1=1.222M Ω
R2=0.349M Ω
R3=3.428M Ω

The voltage adjust circuits has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuits serially.

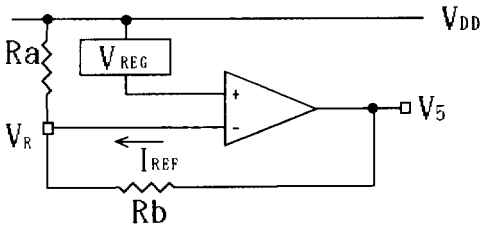
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_5 which controls LCD display contrast can adjust by the instruction. The EVR function is executed to set the 4 bits data into the EVR resistor and determine the one output voltage status out of 16 prefixed voltage status.

When execute the EVR function, set the T_1 and T_2 except the "H, H" and execute the Internal Power Supply On instruction.

[External parts constants setting example when EVR function using / reference]



(1) Determine the V_5 voltage range controlled by EVR.

LCD Driving Voltage V_{DD}-V_5 7V ~ 9V

The range of V_5 2V

(2) Determine the Rb.

Rb = [The range of V_5] / I_{REF} (16status $I_{REF} \fallingdotseq 2.15\ \mu A$ constant current)

Rb = 2V/2.15 μ A = 0.93M Ω *Ta=25 °C ,V_{DD}-V_{OUT} =9V

(3) Adjust the Ra

$$Ra = \frac{V_{REG}}{([\text{LCD Driving Voltage}]\text{-}V_{REG})/Rb}$$

$$Ra = \frac{2.2\ V}{(7V\text{-}2.2V)/0.93M\ \Omega} = 0.43M\ \Omega$$

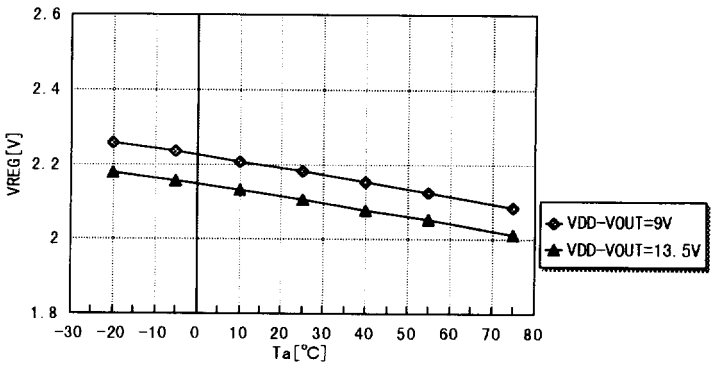
(4) Adjust the Ra

Adjust the Ra to good contrast of LCD display after the (D_3 ,D_2 ,D_1 ,D_0) of EVR register set to (1, 0, 0, 0) or (0, 1, 1, 1). When the EVR using, Ra use a variable resistance and contrast adjustment mentioned in (4) for each chip is required due to the I_{REF} is simple constant current source.

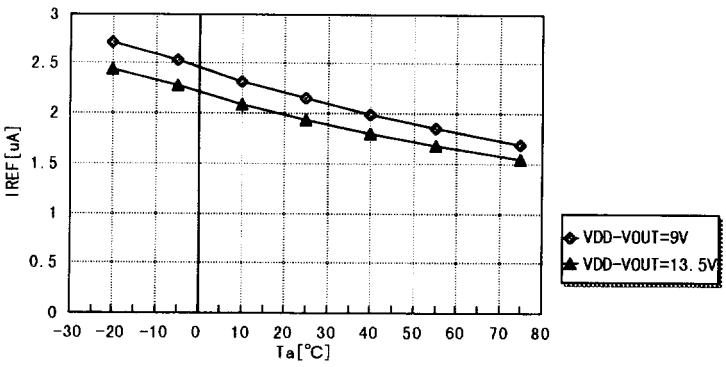
When the EVR function does not use, the (D_3 ,D_2 ,D_1 ,D_0) of EVR register set to (0, 0, 0, 0) by the RES signal or the EVR Register Set instruction.

*) V_{REG}, I_{REF} depends on the voltage between V_{DD} and V_{OUT}, the operating temperature. Please refer to the following graphs.

VREG vs. Temperature (Typical performance)



IREF vs. Temperature (Typical performance)



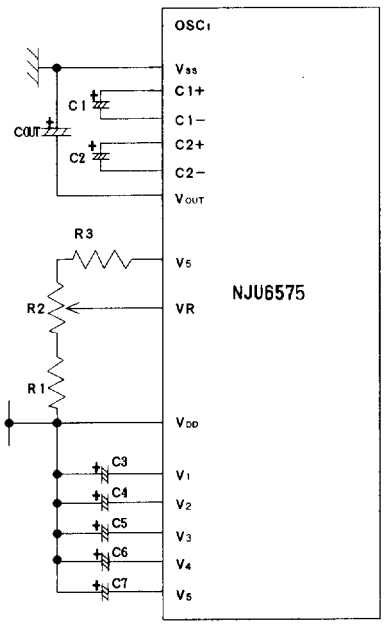
5

(d) LCD Driving Voltage Generation Circuits

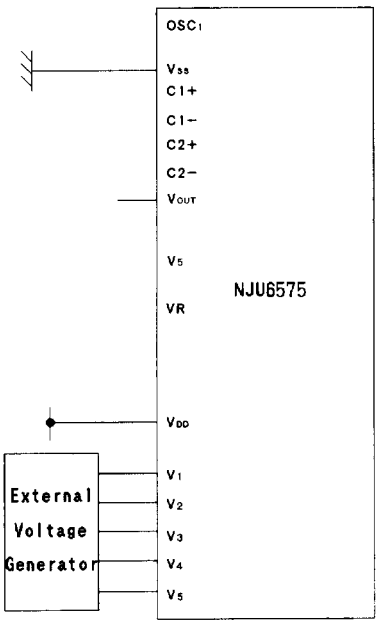
The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V_6 voltage by the bleeder resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 4, five capacitors are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitors C3, C4, C5, C6 and C7 determine by combine with the actual LCD panel.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

VLCD = VDD-V5 ≒ 7 ~ 9 Changed

Item	Value
C_{OUT}	4.7 ~ 10 μF
C1,C2	4.7 ~ 10 μF
C3 to C7	0.1 ~ 0.47 μF
R1	1.222MΩ
R2	0.349MΩ
R3	3.428MΩ

Fig. 4

*1 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.

*2 Following connection of VOUT is required when external power supply using.

When $V_{SS} > V_6$ – $V_{OUT} = V_6$

When $V_{SS} \leqq V_6$ – $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6575 can interface by using both of 8 bit bilateral data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined the P/S terminal connected to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out is impossible.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	-	-	$D_0 \sim D_7$
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6575 can interface both of 68 or 80 type MPU directly by setting the parallel interface (P/S="H") and "H" or "L" of the C86 terminal as shown in table 6.

Table 6

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$
H	68 type MPU	$\overline{CS}$	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6575 discriminate the signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to CS="L"and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal is MSB first like as the order of D_7 to D_0. and the data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or $\overline{CS}$ terminal becomes "H" in spite of the data less then 8 bits, NJU6575 recognizes wrong data as a instruction data. Therefore 8bits data is required for the input data. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface .

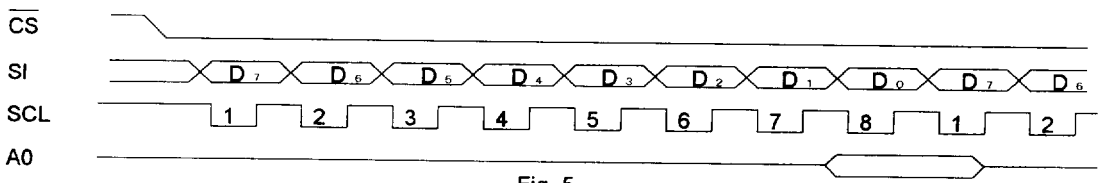


Fig. 5

(5-5) Access to the Display Data RAM and Internal Register.

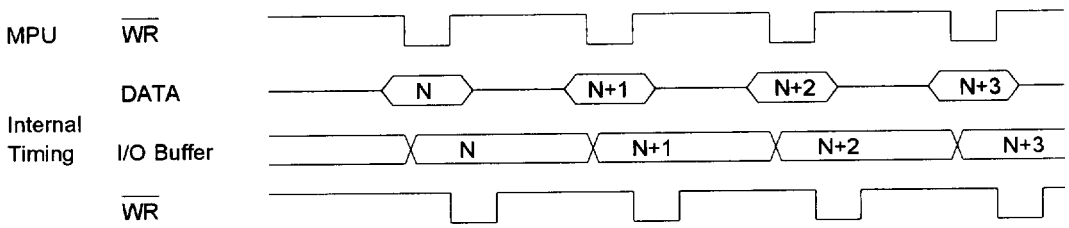
The NJU6575 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU read out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at next data read cycle. And when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6575 is available because of the limitation of access time of NJU6575 locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP operation cycle which equivalent to the waiting operation is useful.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

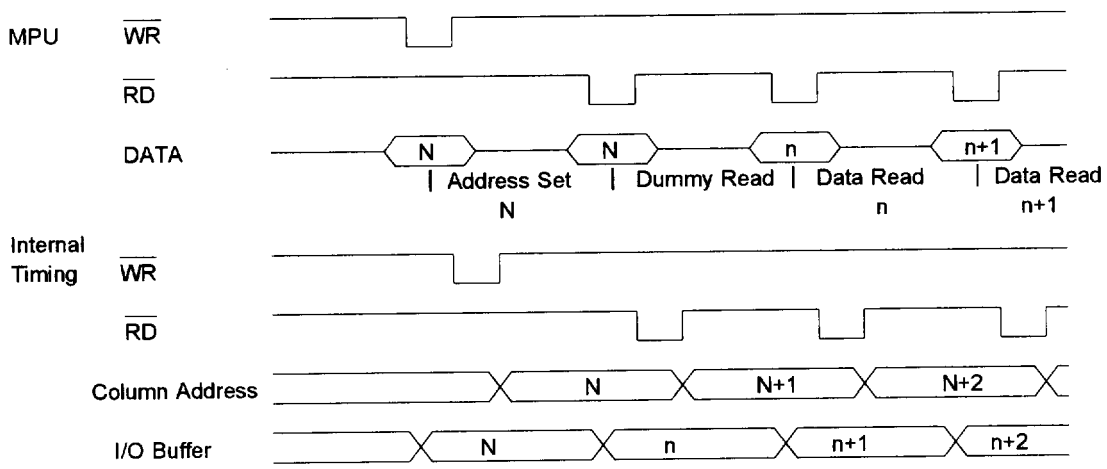


Fig.6

(5-6) Chip Select

$\overline{CS}$ is Chip Select terminal. The Chip Select is executed by the setting of $\overline{CS}$="L". Only the select mode, the interface with MPU is available. In the non select period, the D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, SI and SCL input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 4.5 (used Tripler)	V
Supply Voltage (2)	V_5	V_{DD}-13.5 ~ V_{DD}+0.3	V
Supply Voltage (3)	V_1~V_4	V_5 ~ V_{DD}+0.3	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 125 (Chip) - 55 ~ + 100 (TCP)	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1) (V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~+75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage (1)	Recommend	V_{DD}			4.5	5.0	5.5	V	5
	Available				2.4		5.5		
Operating Voltage (2)	Recommend	V_5			V_{DD}-13.5		V_{DD}-3.5	V	
	Available				V_{DD}-13.5				
	Available	V_1, V_2	V_{LCD}=V_{DD}-V_5		V_{DD}-0.6xV_{LCD}		V_{DD}		
	Available	V_3, V_4			V_5		V_{DD}-0.4xV_{LCD}		
Input Voltage	1	V_{IHC1}	D0, D1...D7, A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$, $\overline{WR}$, C86, SI, SCL, P/S Terminals		0.7xV_{DD}		V_{DD}	V	
		V_{IHC2}		V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
	2	V_{ILC1}			V_{SS}		0.3xV_{DD}		
		V_{ILC2}		V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		
Output Voltage	1	V_{OHC11}	D0, D1...D7, Terminals	I_{OH}= -1mA	0.8xV_{DD}		V_{DD}	V	
		V_{OHC12}		I_{OH}=-0.5mA V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
	2	V_{OLC11}	D0, D1...D7, Terminals	I_{OL}= 1mA	V_{SS}		0.2xV_{DD}		
		V_{OLC12}		I_{OL}= 0.5mA V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		
Input Leakage Current		I_{LI}	All input terminals		-1.0		1.0	uA	
		I_{LO}	All I/O term. (D0...D7)		-3.0		3.0		6
Driver On-resistance		R_{ON1}	Ta=25°C	V_{LCD}=13.5V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD}=8.0V		3.0	4.5		

5

■ ELECTRICAL CHARACTERISTICS (2)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Stand-by Current		I_{DDQ}	during Power save Mode			0.05	5.0	uA	8
Operating Current		I_{DD12}	Display			28	45		
		I_{DD14}	V_{LCD}=8V	V_{DD}=2.7V		16	25		
		I_{DD21}	Accessing fcyc=200kHz			350	500	uA	9
		I_{DD22}		V_{DD}=2.7V		170	240		
Input Terminal Capacitance		C_{IN}	A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$, $\overline{WR}$, C86, SI, SCL, P/S, T1, T2, D0, D1...D7 Ta=25°C			10		pF	
Oscillation Frequency		fosc	Ta=25°C	V_{DD}=5.0V	15	18	21	kHz	
				V_{DD}=2.7V	11	16	21		
Voltage Tripler	Input Voltage	V_{DD1}	V_{DD}-V_{SS}		2.4		5.5	V	
		V_{DD2}	V_{DD}-V_{SS} used Tripler		2.4		4.5		10
	Output Volt.	V_{OUT}	V_{SS}-V_{LCD}, used Tripler		-9.0			V	
	On -resistance	R_{TRI}	V_{DD}=3V; C=4.7uF used Tripler			600	1000	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Tripler Circuit "OFF"		V_{DD}-13.5		V_{DD}-5.0	V	11
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"		V_{DD}-13.5		V_{DD}-5.0	V	
	Operating Current	I_{OUT1}	V_{DD}=4.5V, V_{LCD}=8V			53	T.B.D.	uA	12
		I_{OUT2}	COM/SEG Term Open, No Access Display check. pattern			12	T.B.D.		
		I_{OUT3}				10	T.B.D.		
	Voltage Reg.	V_{REG}	V_{DD}-V_{out}=9V; Ta=25°C		T.B.D.	2.2	T.B.D.	V	13
	Reference Current	I_{REF}	V_{DD}-V_{out}=9V; Ta=25°C		1.50	2.15	2.80	uA	

Note 5) NJU6575 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D_0 to D_7 terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set".

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 10) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

■ ELECTRICAL CHARACTERISTICS (2)

Note 12) Each operating current of voltage supply circuits block is specified under below table conditions.

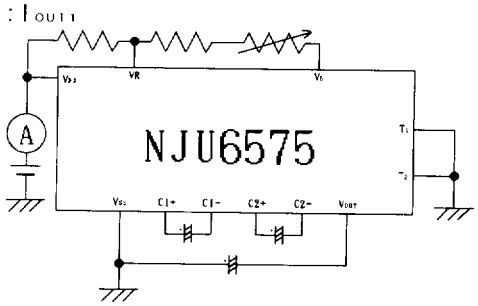
SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T_1	T_2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use (V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use (V_{OUT}, V_5)

* = Don't Care

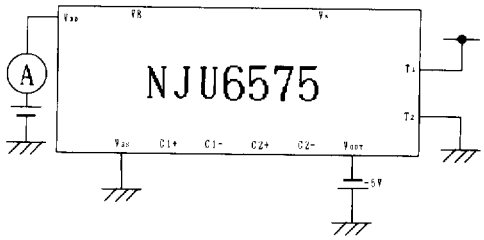
Note 13) Apply to the precision of Voltage on each EVR steps.

MEASUREMENT BLOCK DIAGRAM

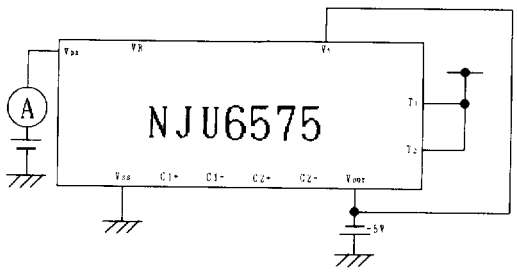
: I_{OUT1}



: I_{OUT2}



: I_{OUT3}



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■ ELECTRICAL CHARACTERISTICS (3)

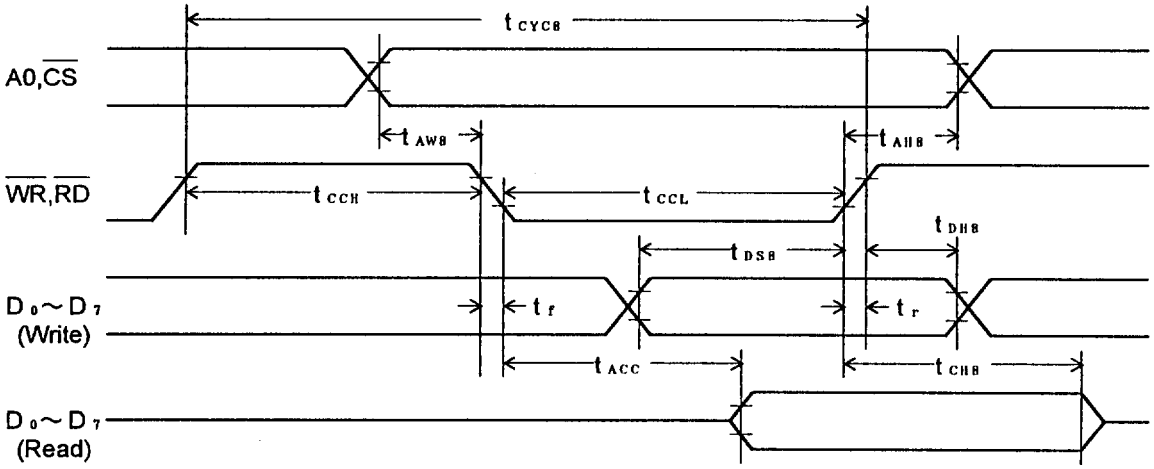
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	15

Note 14) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 15) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

5

■ BUS TIMING CHARACTERISTICS

• Read/Write operation sequence (80 Type MPU)



(V_{DD}=5.0V±10%, Ta=-20~75°C)

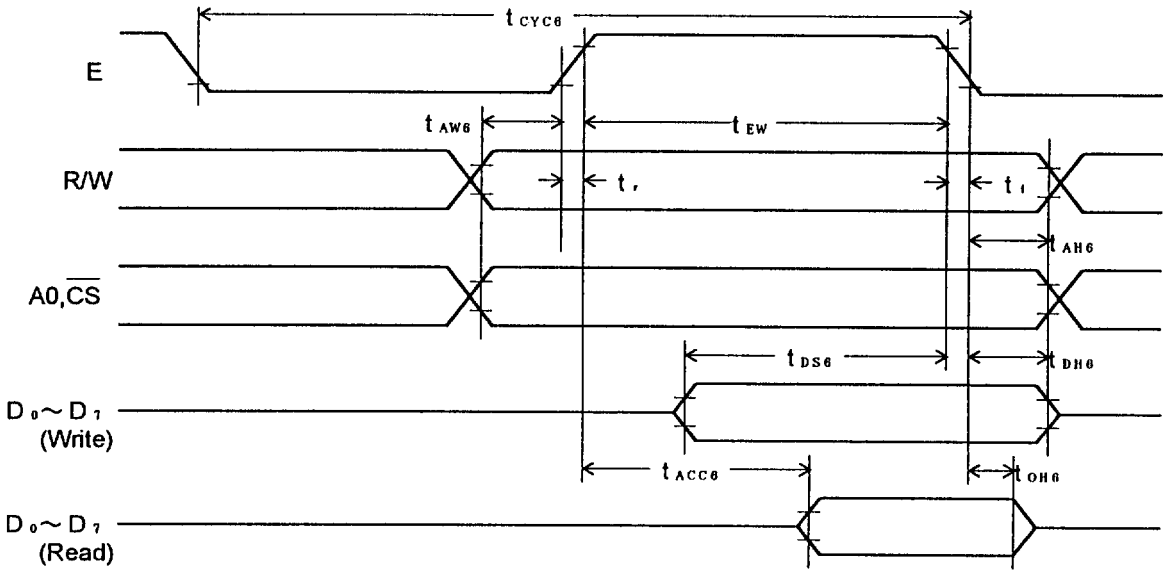
PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		AO, CS Terminals	t_{AH8}	10			ns
Address Set Up Time			t_{AW8}	10			
System Cycle Time		WR, RD Terminals	t_{CYC8}	180			
Control Pulse Width	WR, "L"		t_{CCL} (W)	25			
	RD, "L"		t_{CCL} (R)	80			
	"H"		t_{CCH}	70			
Data Set Up Time		D0~D7 Terminals	t_{DS8}	60			
Data Hold Time			t_{DH8}	10			
RD Access Time			t_{ACC8}		70	CL=100pF	
Output Disable Time			t_{OH8}	0	30		
Rise Time, Fall Time		CS, WR, RD, AO, D0~D7 Terminals	t_r, t_f		15		

(V_{DD}=2.7V~4.5V, Ta=-20~75°C)

PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		AO, CS Terminals	t_{AH8}	25			ns
Address Set Up Time			t_{AW8}	25			
System Cycle Time		WR, RD Terminals	t_{CYC8}	450			
Control Pulse Width	WR, "L"		t_{CCL} (W)	50			
	RD, "L"		t_{CCL} (R)	200			
	"H"		t_{CCH}	220			
Data Set Up Time		D0~D7 Terminals	t_{DS8}	120			
Data Hold Time			t_{DH8}	35			
RD Access Time			t_{ACC8}		140	CL=100pF	
Output Disable Time			t_{OH8}	0	35		
Rise Time, Fall Time		CS, WR, RD, AO, D0~D7 Terminals	t_r, t_f		15		

Note 16) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 17) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

・ Read/Write operation sequence (68 Type MPU)



(V_{DD}=5.0V±10%, Ta=−20～75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS, R/W Terminals	t_{AH6}	10			ns
Address Set Up Time		t_{AW6}	10			
System Cycle Time		t_{CYC6}	180			
Enable Pulse Width	Read	t_{EW}	100			
	Write		25			
Data Set Up Time	D0～D7 Terminals	t_{DS6}	60			
Data Hold Time		t_{DH6}	20			
Access Time		t_{ACC6}		70	CL=100pF	
Output Disable Time		t_{OH6}	0	25		
Rise Time, Fall Time	A0, CS, R/W, E, D0～D7 Terminals	t_r, t_f		15		

(V_{DD}=2.7V～4.5V, Ta=−20～75°C)

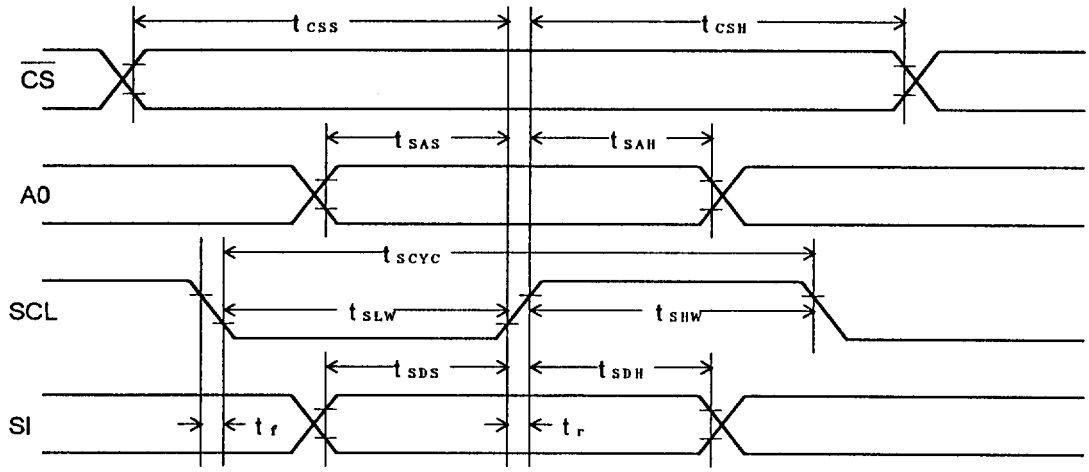
PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, CS, R/W Terminals	t_{AH6}	25			ns
Address Set Up Time		t_{AW6}	25			
System Cycle Time		t_{CYC6}	450			
Enable Pulse Width	Read	t_{EW}	200			
	Write		50			
Data Set Up Time	D0～D7 Terminals	t_{DS6}	120			
Data Hold Time		t_{DH6}	40			
Access Time		t_{ACC6}		140	CL=100pF	
Output Disable Time		t_{OH6}	0	45		
Rise Time, Fall Time	A0, CS, R/W, E, D0～D7 Terminals	t_r, t_f		15		

Note 18) t_{CYC6} indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.

Note 19) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.

Note 20) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

· Write operation sequence (Serial Interface)



(V_{DD}=5.0V±10%, Ta=-20~75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	500			ns
SCL "H" pulse width		t_{SHW}	150			
SCL "L" pulse width		t_{SLW}	150			
Address Set Up Time	A0 Terminal	t_{SAS}	120			
Address Hold Time		t_{SAH}	200			
Data Set Up Time	SI Terminal	t_{SDS}	120			
Data hold Time		t_{SDH}	50			
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	t_{CSS}	30			
		t_{CSH}	400			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	t_r, t_f		15		

(V_{DD}=2.7V~4.5V, Ta=-20~75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	1000			ns
SCL "H" pulse width		t_{SHW}	300			
SCL "L" pulse width		t_{SLW}	300			
Address Set Up Time	A0 Terminal	t_{SAS}	250			
Address Hold Time		t_{SAH}	400			
Data Set Up Time	SI Terminal	t_{SDS}	250			
Data hold Time		t_{SDH}	100			
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	t_{CSS}	60			
		t_{CSH}	800			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	t_r, t_f		15		

Note 21) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 22) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

■ LCD DRIVING WAVEFORM

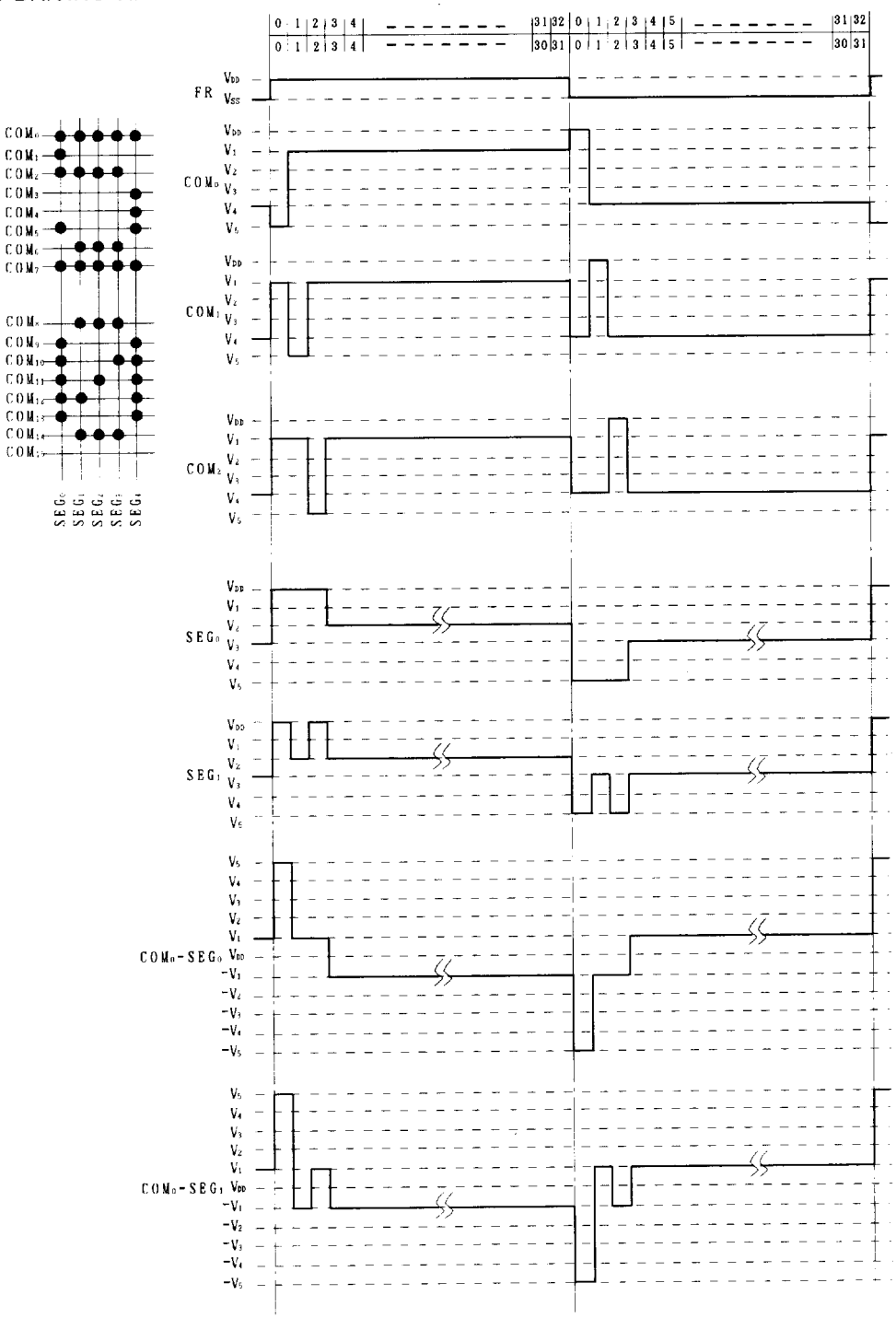


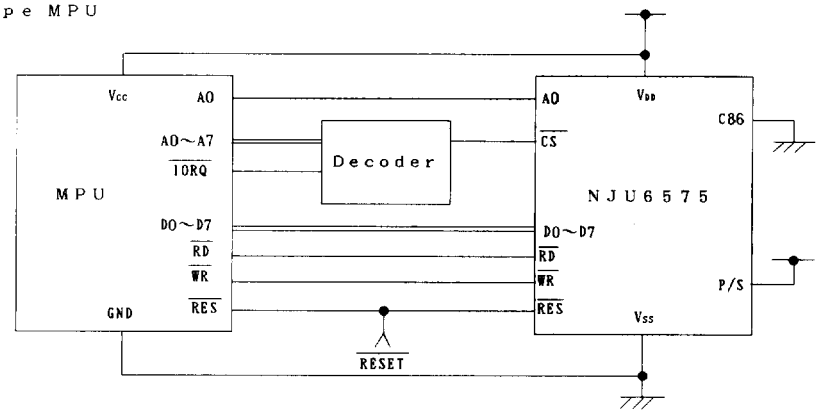
Fig. 7

■ APPLICATION CIRCUIT

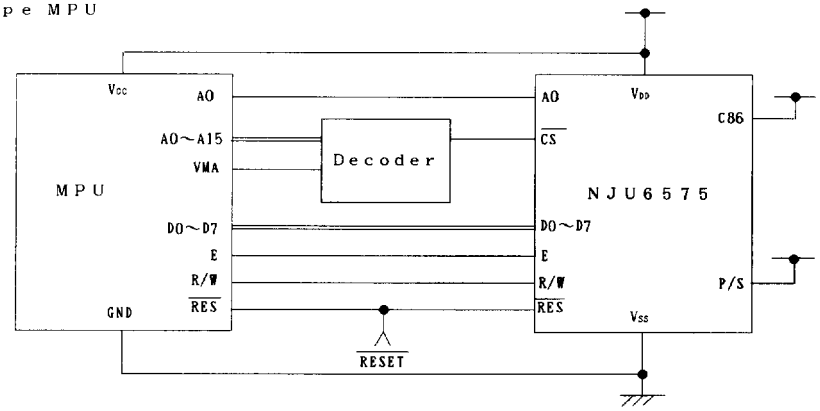
·Microprocessor Interface Example

The NJU6575 can interface with both of 80 type and 68 type MPU by the serial format directly.
Therefore minimum wiring for the MPU interface is available.

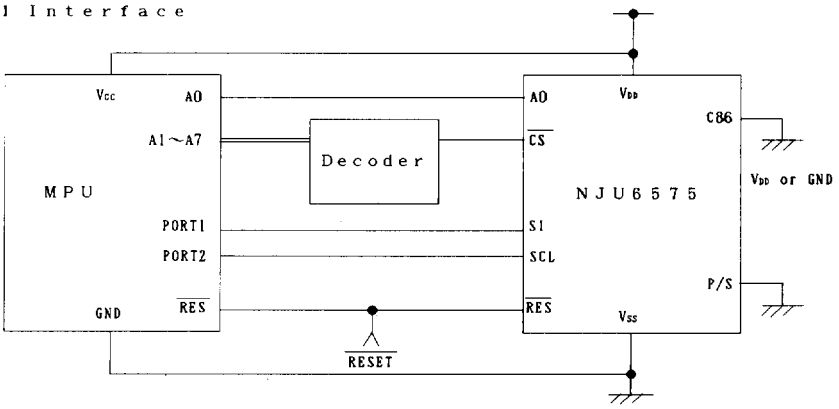
●80 Type MPU



●68 Type MPU



●Serial Interface



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