BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6561 is a bit map LCD driver to display graphics or characters.

It contains 3,920 bits display data RAM, microprocessor interface circuits, instruction decoder, 80-segment and 49-common (1 out of 49-driver is prepared for icon display) drivers.

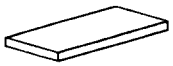
The bit image display data is transferred to the display data RAM by serial interface circuit.

49 x 80 dot graphics or 5-character 3-line by 16 x 16 dot character with icon are displayed by NJU6561 itself.

The wide operating voltage like as 2.4V to 5.5V and low operating current are useful to apply small sized battery operated items.

The rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE

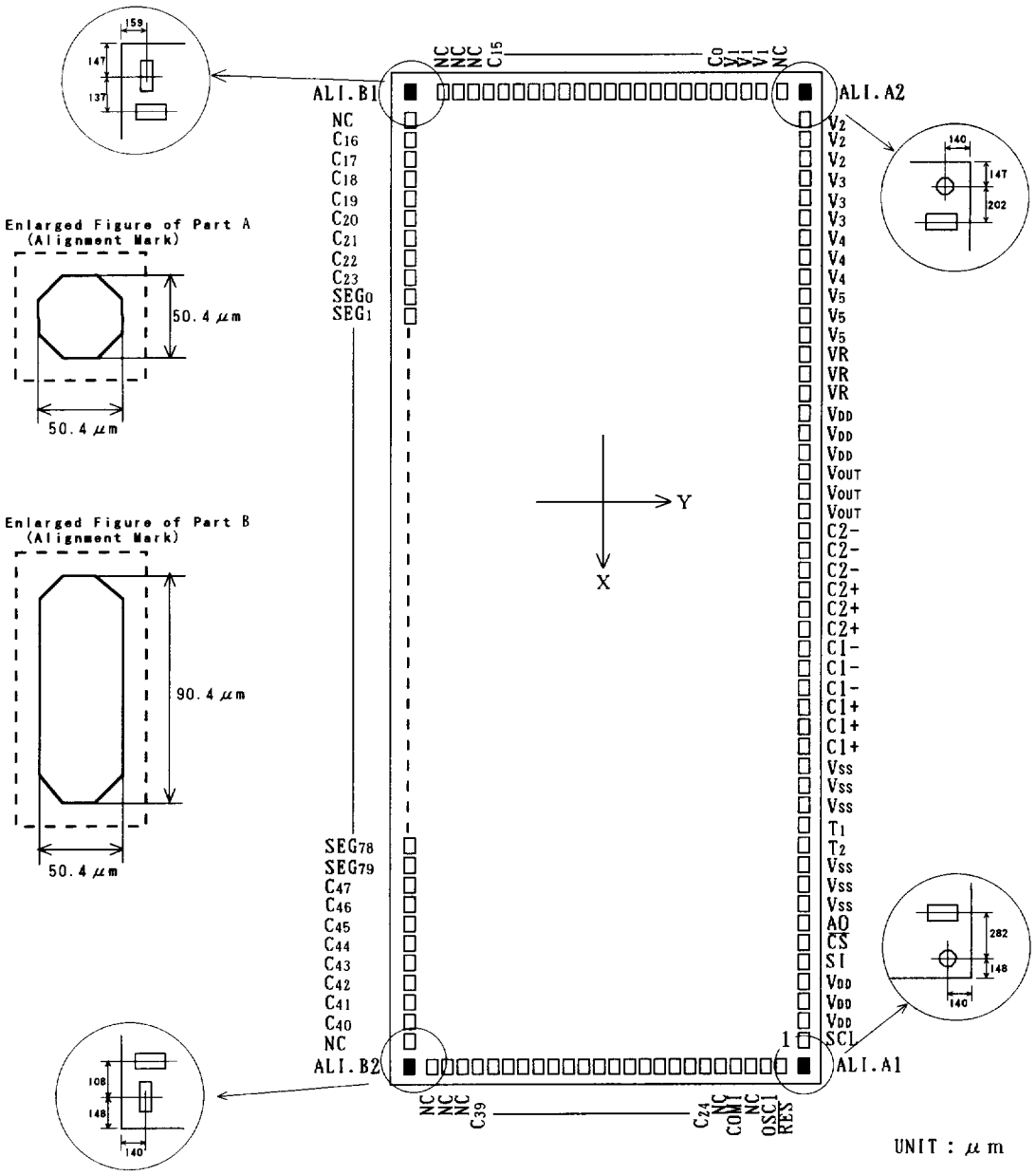


NJU6561C

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 3,920 bits
- 129 LCD Drivers - 49-common and 80-segment
- Serial Interface
- Programmable Duty Ratio ; 1/48 or 1/49 Duty
- Useful Instruction Set
  Display Data Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, All On/Off, Icon Display, Read Modify Write, Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage — 2.4V ~5. 5V
- LCD Driving Voltage — 6.0V ~ 13.5V
- Package Outline — Chip / Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip	Center	X=0um, Y=0um
Chip	Size	X=8.46mm, Y=2.82mm
Chip	Thickness	400um ± 30um
Bump	Size	50um x 110um
Bump	height	25umTYP.
Bump	Material	Au

■ : Four PADs illustrated with this mark are the alignment marks for COG.

■ PAD COORDINATES

Chip Size 8.46mm x 2.82mm(Chip Center X=0um,Y=0um)

PAD No.	Terminal	X=(μm)	Y=(μm)	PAD No.	Terminal	X=(μm)	Y=(μm)	PAD No.	Terminal	X=(μm)	Y=(μm)
1	SCL	3800	1244	51	V_1	-4064	830	101	SEG_{20}	-1546	-1245
2	V_{DD}	3480	1244	52	V_1	-4064	750	102	SEG_{21}	-1466	-1245
3	V_{DD}	3400	1244	53	C_0	-4064	670	103	SEG_{22}	-1386	-1245
4	V_{DD}	3320	1244	54	C_1	-4064	590	104	SEG_{23}	-1306	-1245
5	SI	3000	1244	55	C_2	-4064	510	105	SEG_{24}	-1226	-1245
6	CS	2600	1244	56	C_3	-4064	430	106	SEG_{25}	-1146	-1245
7	A0	2200	1244	57	C_4	-4064	350	107	SEG_{26}	-1066	-1245
8	V_{SS}	1880	1244	58	C_5	-4064	270	108	SEG_{27}	-986	-1245
9	V_{SS}	1800	1244	59	C_6	-4064	190	109	SEG_{28}	-906	-1245
10	V_{SS}	1720	1244	60	C_7	-4064	110	110	SEG_{29}	-826	-1245
11	T_2	1400	1244	61	C_8	-4064	30	111	SEG_{30}	-746	-1245
12	T_1	1000	1244	62	C_9	-4064	-51	112	SEG_{31}	-666	-1245
13	V_{SS}	680	1244	63	C_{10}	-4064	-131	113	SEG_{32}	-586	-1245
14	V_{SS}	600	1244	64	C_{11}	-4064	-211	114	SEG_{33}	-506	-1245
15	V_{SS}	520	1244	65	C_{12}	-4064	-291	115	SEG_{34}	-426	-1245
16	C1+	280	1244	66	C_{13}	-4064	-371	116	SEG_{35}	-346	-1245
17	C1+	200	1244	67	C_{14}	-4064	-451	117	SEG_{36}	-266	-1245
18	C1+	120	1244	68	C_{15}	-4064	-531	118	SEG_{37}	-186	-1245
19	C1−	-121	1244	69	NC	-4064	-691	119	SEG_{38}	-106	-1245
20	C1−	-201	1244	70	NC	-4064	-851	120	SEG_{39}	-26	-1245
21	C1−	-281	1244	71	NC	-4064	-1011	121	SEG_{40}	54	-1245
22	C2+	-521	1244	72	NC	-3946	-1245	122	SEG_{41}	134	-1245
23	C2+	-601	1244	73	C_{16}	-3786	-1245	123	SEG_{42}	214	-1245
24	C2+	-681	1244	74	C_{17}	-3706	-1245	124	SEG_{43}	294	-1245
25	C2−	-921	1244	75	C_{18}	-3626	-1245	125	SEG_{44}	374	-1245
26	C2−	-1001	1244	76	C_{19}	-3546	-1245	126	SEG_{45}	454	-1245
27	C2−	-1081	1244	77	C_{20}	-3466	-1245	127	SEG_{46}	534	-1245
28	V_{OUT}	-1321	1244	78	C_{21}	-3386	-1245	128	SEG_{47}	614	-1245
29	V_{OUT}	-1401	1244	79	C_{22}	-3306	-1245	129	SEG_{48}	694	-1245
30	V_{OUT}	-1481	1244	80	C_{23}	-3226	-1245	130	SEG_{49}	774	-1245
31	V_{DD}	-1721	1244	81	SEG_0	-3146	-1245	131	SEG_{50}	854	-1245
32	V_{DD}	-1801	1244	82	SEG_1	-3066	-1245	132	SEG_{51}	934	-1245
33	V_{DD}	-1881	1244	83	SEG_2	-2986	-1245	133	SEG_{52}	1014	-1245
34	VR	-2121	1244	84	SEG_3	-2906	-1245	134	SEG_{53}	1094	-1245
35	VR	-2201	1244	85	SEG_4	-2826	-1245	135	SEG_{54}	1174	-1245
36	VR	-2281	1244	86	SEG_5	-2746	-1245	136	SEG_{55}	1254	-1245
37	V_5	-2521	1244	87	SEG_6	-2666	-1245	137	SEG_{56}	1334	-1245
38	V_5	-2601	1244	88	SEG_7	-2586	-1245	138	SEG_{57}	1414	-1245
39	V_5	-2681	1244	89	SEG_8	-2506	-1245	139	SEG_{58}	1494	-1245
40	V_4	-2921	1244	90	SEG_9	-2426	-1245	140	SEG_{59}	1574	-1245
41	V_4	-3001	1244	91	SEG_{10}	-2346	-1245	141	SEG_{60}	1654	-1245
42	V_4	-3081	1244	92	SEG_{11}	-2266	-1245	142	SEG_{61}	1734	-1245
43	V_3	-3321	1244	93	SEG_{12}	-2186	-1245	143	SEG_{62}	1814	-1245
44	V_3	-3401	1244	94	SEG_{13}	-2106	-1245	144	SEG_{63}	1894	-1245
45	V_3	-3481	1244	95	SEG_{14}	-2026	-1245	145	SEG_{64}	1974	-1245
46	V_2	-3721	1244	96	SEG_{15}	-1946	-1245	146	SEG_{65}	2054	-1245
47	V_2	-3801	1244	97	SEG_{16}	-1866	-1245	147	SEG_{66}	2134	-1245
48	V_2	-3881	1244	98	SEG_{17}	-1786	-1245	148	SEG_{67}	2214	-1245
49	NC	-4064	1070	99	SEG_{18}	-1706	-1245	149	SEG_{68}	2294	-1245
50	V_1	-4064	910	100	SEG_{19}	-1626	-1245	150	SEG_{69}	2374	-1245

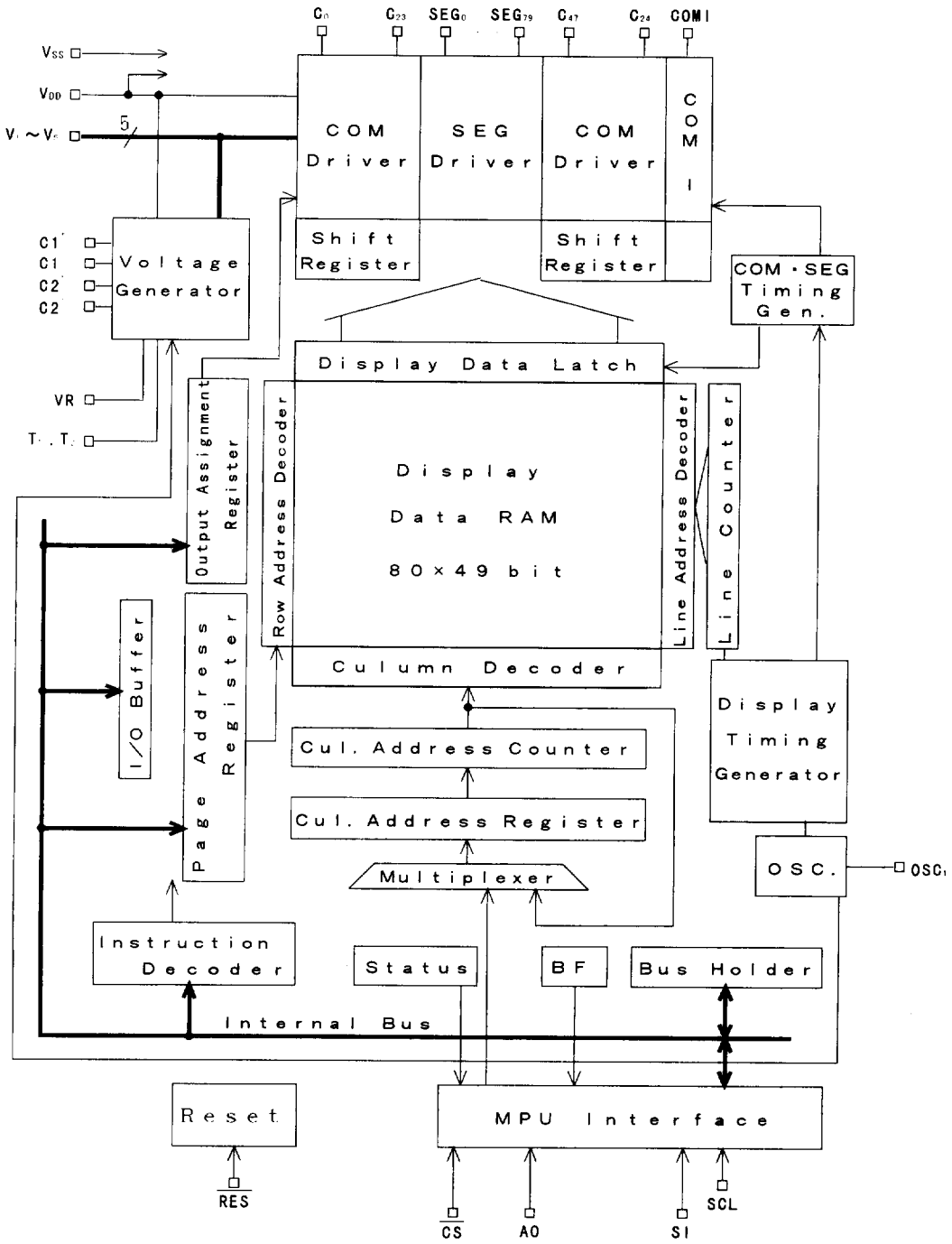
5

PAD No.	Terminal	X=(μm)	Y=(μm)
151	SEG 70	2454	-1245
152	SEG 71	2534	-1245
153	SEG 72	2614	-1245
154	SEG 73	2694	-1245
155	SEG 74	2774	-1245
156	SEG 75	2854	-1245
157	SEG 76	2934	-1245
158	SEG 77	3014	-1245
159	SEG 78	3094	-1245
160	SEG 79	3174	-1245
161	C 47	3254	-1245
162	C 46	3334	-1245
163	C 45	3414	-1245
164	C 44	3494	-1245
165	C 43	3574	-1245
166	C 42	3654	-1245
167	C 41	3734	-1245
168	C 40	3814	-1245
169	NC	3974	-1245
170	NC	4063	-1017
171	NC	4063	-857
172	NC	4063	-697
173	C 39	4063	-537
174	C 38	4063	-457

PAD No.	Terminal	X=(μm)	Y=(μm)
175	C 37	4063	-377
176	C 36	4063	-297
177	C 35	4063	-217
178	C 34	4063	-137
179	C 33	4063	-57
180	C 32	4063	23
181	C 31	4063	103
182	C 30	4063	183
183	C 29	4063	263
184	C 28	4063	343
185	C 27	4063	423
186	C 26	4063	503
187	C 25	4063	583
188	C 24	4063	663
189	NC	4063	743
190	COMI	4063	823
191	NC	4063	903
192	OSC 1	4063	983
193	$\overline{RES}$	4063	1063
ALIGNMENT	ALIGNMENT A1	4082	1270
ALIGNMENT	ALIGNMENT A2	-4083	1270
ALIGNMENT	ALIGNMENT B1	-4083	-1251
ALIGNMENT	ALIGNMENT B2	4082	-1251

5

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function
2,3,4, 31,32,33	V_{DD}	Power	V_{DD} =+5V.(Less than 4.5V should be apply When voltage tripler using.)
8,9,10, 13,14,15	V_{SS}	GND	V_{SS} =0V
50,51,52 46,47,48 43,44,45 40,41,42 37,38,39	V_1 V_2 V_3 V_4 V_5	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ When internal power supply is on, internal circuits generated and supply following LCD bias voltage to $V_1 \sim V_4$ terminals. Term. / Volt.: V_1 = V_5 +4/5V_{LCD}; V_2 = V_5 +3/5V_{LCD}; V_3 = V_5 +2/5V_{LCD}; V_4 = V_5 +1/5V_{LCD} (V_{LCD} =V_{DD} -V_5)
16,17,18 19,20,21 22,23,24 25,26,27	C1 + C1 - C2 + C2 -	O	Step up capacitor connecting terminals. In case of tripler operation, connect the capacitor between C1 + and C1 -, C2 + and C2 -. In case of doubler operation, connect the capacitor between C2 - and C2 -, connect C2 + to C1 +, and C1 - should be open.
28,29,30	V_{OUT}	O	Step up voltage output terminal. Connect the capacitor between this terminal and V_{SS}.
34,35,36	VR	I	Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance connect between V_{DD} and V_5 terminal.
12 11	T_1 T_2	I	LCD bias voltage control terminals. ※ Don't Care T_1 / T_2 / Step up cir. / Voltage Adj. / V/F Cir.: L / ※ / Available / Available / Available H / L / Not Avail. / Available / Available H / H / Not Avail. / Not Avail. / Available
7	A0	I	Connect to the Address bus of MPU. The data is distinguished Display Data or Instruction by this signal. A0 / Dist.: H = Display Data; L = Instruction
193	$\overline{RES}$	I	Reset terminal. When the $\overline{RES}$ terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of $\overline{RES}$.
6	$\overline{CS}$	I	Chip select terminal. Data input is available by during "L" state of $\overline{CS}$.
5	SI	I	Serial data input terminal.
1	SCL	I	Serial data clock signal input terminal. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.
192	OSC_1	I	System clock input terminal for Maker testing. This terminal should be open.

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>53 ~ 68</td><td>C_0 ~ C_{15}</td><td rowspan="4">O</td><td rowspan="4">LCD drive output terminals.

・ Segment output terminal (SEG_0 to SEG_{79})
Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM.

<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal</th><th>Reverse</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
</table>

・ Common Output Terminal (C_0 to C_{47})
Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data.

<table>
<tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
</table>
</td></tr>
<tr><td>73 ~ 80</td><td>C_{16} ~ C_{23}</td></tr>
<tr><td>81 ~ 160</td><td>SEG_0 ~ SEG_{79}</td></tr>
<tr><td>188 ~ 173</td><td>C_{24} ~ C_{39}</td></tr>
<tr><td>168 ~ 161</td><td>C_{40} ~ C_{47}</td></tr>
<tr><td>190</td><td>COMI</td><td>O</td><td>Icon common output terminal.
Icon common output when Icon Display instruction execution.

<table>
<tr><th></th><th>Icon Display ON</th><th>Icon Display OFF</th></tr>
<tr><td>State</td><td>C_{48}</td><td>V_1 or V_4</td></tr>
</table>
</td></tr>
</table>

(Terminals 49,69,70,71,72,169,170,171,172,189,191 are NC)

5

■ Functional Description

(1) Description for each blocks

(1-1) Line Counter

The Line Counter is reset at the FR signal changing and counts up by synchronizing common signal cycle and generate the line address which addressing the read out line of Display Data RAM.

(1-2) Column Address Counter

The column address counter is 8-bit presettable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to $(AO)_H$ when the Display Date Write instruction is executed. This counter auto-increments (+1) up to $(A0)_H$ but accessing to the display data RAM over than $(4F)_H$ is forbidden.

Furthermore, this counter is independent with the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM correspondence to the Segment Driver.

(1-3) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the data by changing the page, the page address set instruction is required. Page address "6"(D_2=D_1="H" and D_0="L") is Icon RAM area, the data only for the D_0 is valid.

(1-4) Display Data RAM

Display Data RAM consists of 3,920 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

When Normal Display : On="1" , Off="0"
When Inverse Display : On="0" , Off="1"

The Display Data RAM output 80 bit parallel data addressed by the line counter, and these data are set into the Display Data Latch.

This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize rewriting.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.

(1-5) Common and Segment Driver Assignment

The scanning order can be assigned by setting A_3 of the Output Assignment Register as shown Table 1.

The location of Segment Drivers are fixed at any time.

Table 1

Register		COM Output Terminals			
A3	PAD No.	53	80	161	188
	Pin name	C_0	C_{23}	C_{47}	C_{24}
0	---------->	COM23 <----------	COM0	COM24 ---------->	COM47
1	---------->	COM24 ---------->	COM47	COM23 <----------	COM0

The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COMI is fixed to COM_{48} timing regardless the other Common Driver assignment.

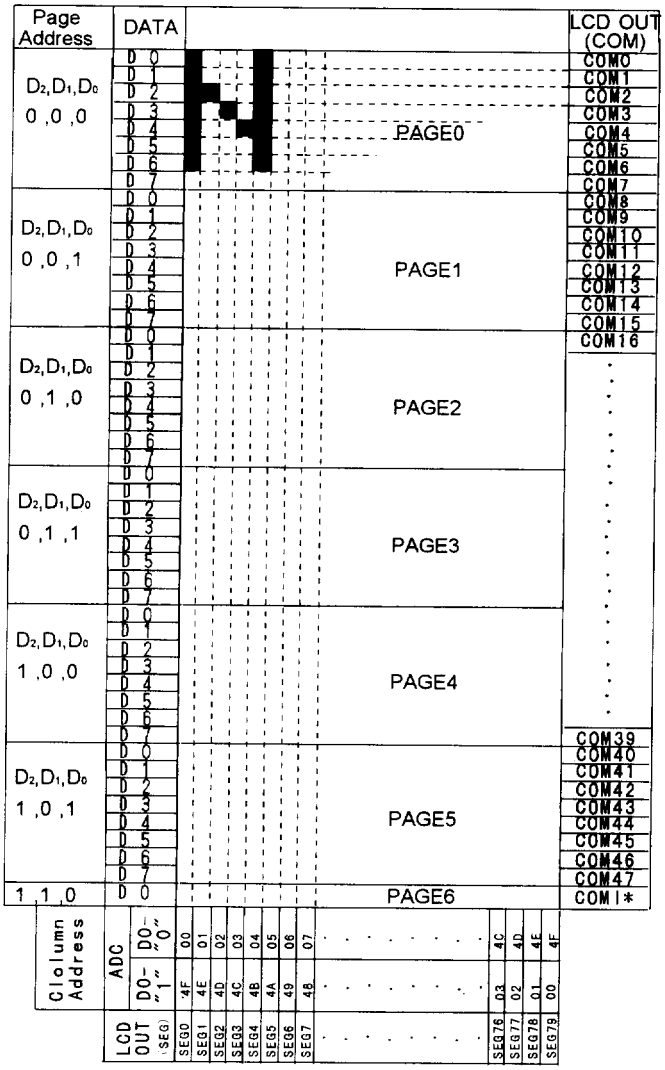


Fig.1 Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/49 duty set,)

(1-6) Reset Circuits

The NJU6561 performs following initialization when the $\overline{RES}$ input is put on the "L" level.

Initialization

① Display Off
② Normal Display(Non-inverse display)
③ Icon Display Reset
④ ADC Select : Normal (ADC Instruction D_0 ="0")
⑤ Read Modify Write Mode Off
⑥ Internal Power supply(Step up) circuits Off
⑦ Clear the serial interface register
⑧ Set the address $(00)_H$ to the Column Address Counter
⑨ Set the page "0" to the Page Address Register
⑩ Select the D_3 of the Output Assignment Register to "0"
⑪ Set the EVR register to $(00)_H$

The $\overline{RES}$ terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface Example". The reset signal require over than 10us $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{RES}$ signal, the normal operation is starting.
In case of the internal power supply(Step up) circuits do not use, the $\overline{RES}$ terminal must be "L" when external power supply turn on. $\overline{RES}$="L" input reset internal register and set above default, but oscillation circuits are no influence.
No initialization by $\overline{RES}$ when power turns on, will make Hung up condition, therefore please initialize by the $\overline{RES}$ when power turns on. By the reset Instruction performs only ⑧ through ⑪ mentioned in above.
The noise into the $\overline{RES}$ terminal should be cared when of the application design to avoid the error function.

5

(1-7) LCD Driving

(a) LCD Driving Circuits

NJU6561 incorporate 129 LCD Drivers like as 80 Segment drivers, 48 Common drivers and 1 Icon common driver. 48 Common drivers incorporate the shift register which scanning the common display signal. The combination among the Display data, COM scan signal and FR signal define the LCD driving output voltage. The output wave form is mentioned in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 80-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver. The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits

The clock for Line Counter and latch signal for the Latch Circuits are generated from display clock(CL). The line address is renewed by synchronizing with display clock and 80 bits display data are latched into display latch circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR has a function to generate the two frame alternative driving method waveform for the LCD panel.

(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

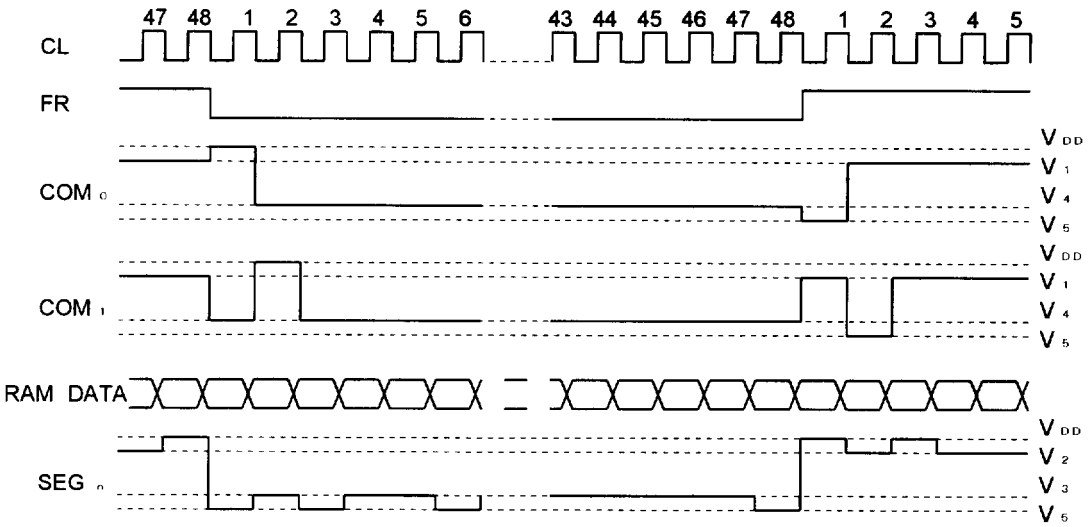


Fig. 2 Waveform of Display Timing

(f) Oscillation Circuits

The Oscillation Circuits which incorporates the oscillating resistance R and capacitance C, is a low power CR oscillator and it is used as display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuits output frequency is divided by 8 which is used as display clock CL.

(g) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Tripler or Doubler) Circuits, Regulation Circuits, and Voltage Follower. Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the large size LCD panel application. If the contrast is no good in those application, please use external power supply supplied more high current.

The suitable values of the capacitors connecting to the V1 to V5 terminals, the step up circuit and the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption in the LCD panel is changeable with the display patarn. Therefore a trial with actual module should be practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, voltage follower circuits are off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD supply from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$,and VR are open, and V_{OUT} connect to the V_5 terminal The status of internal power supply can select by T_1 and T_2 terminal. The external power supply can be used together with some of internal power supply function.

Table 3. (*:Don't Care)

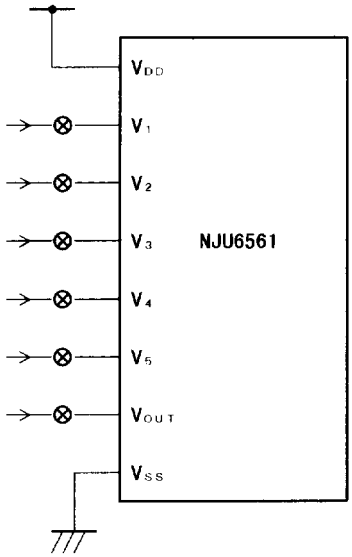
T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term
L	*	O	O	O	-		
H	L	×	O	O	V_{OUT}	OPEN	
H	H	×	×	O	V_5,V_{OUT}	OPEN	OPEN

When (T_1, T_2)=(H, L), the terminal for step up circuit of $C1^+$,$C1^-$ $C2^+$,$C2^-$ are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T_1, T_2)=(H, H), terminals for step up circuit and VR are open, Connect the V_5 terminal and

V_{OUT}, and supply the LCD driving voltage from outside due to the Step up circuit and Voltage adjust circuits are stop its operation.

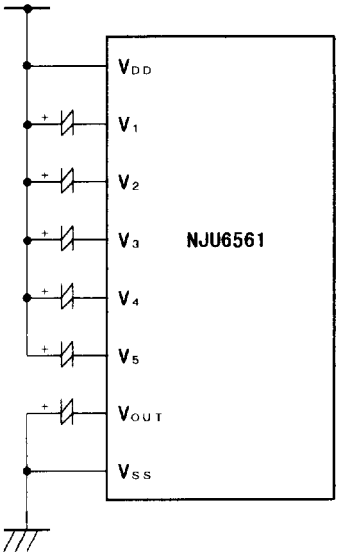
○ Examples for application circuits of the internal Power Supply

(1)None of the internal power supply functions.



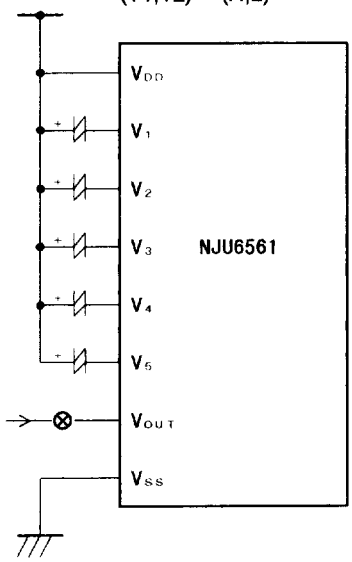
(2) All of the internal power supply functions.
(Step up, Voltage Adj., Buffer(V/F))

(T1, T2) = (L, *) *: Don't care.



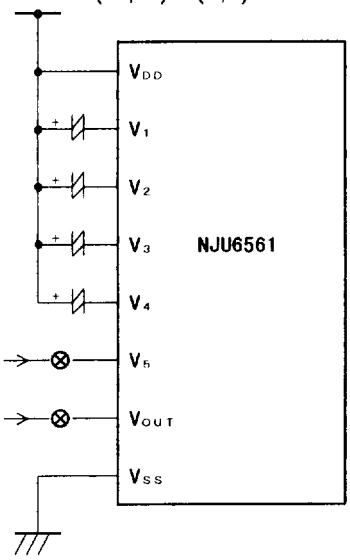
(3)Some of the internal power supply functions.
(Voltage Adjust., Buffer(V/F))

(T1,T2) = (H,L)



(4)Some of the internal power supply functions.
(Buffer(V/F))

(T1,T2) = (H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6561 distinguishes the signal on the 8-bit serial input data (D_7 to D_0) by combination of A0.
The NJU6561 is operating so first because of the decode of the instruction and execution are performs only depend on the internal timing which not depend on the external clock.
The data input as MSB first serially.
The Table. 4 shows the instruction codes of the NJU6561.

Table 4. Instruction Code

Instruction		Code A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description
(1)	Display ON/OFF	0	1	0	1	0	1	1	1	0 1	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Add. Register
(3)	Column Address Set High Order 3bit	0	0	0	0	1	High order Column. Add.				Set the Higher order 4 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bit	0	0	0	0	0	Lower order Column. Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Write Display Data	1	Write Data								Write the data into the Display Data RAM
(6)	ADC Select	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(7)	Normal or Inverse of On/Off Set	0	1	0	1	0	0	1	1	0 1	Inverse the On and Off Display 0:Normal 1:Inverse
(8)	Whole Display On	0	1	0	1	0	0	1	0	0 1	Whole Display Turns On 0:Normal 1:Whole Disp. On
(9)	Icon Display	0	1	0	1	0	1	0	1	0 1	Set the Duty Ratio 0:No Icon 1:With Icon
(10)	Read Modify Write	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing
(11)	End	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode
(12)	Reset	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(13)	Output Assignment Register Set	0	1	1	0	0	A_3	*	*	*	Set the scanning order of common drivers to the Register
(14)	Internal Power Supply On/Off	0	0	0	1	0	0	1	0	0 1	0:Int. Power Supply Off 1:Int. Power Supply On
(15)	LCD Driving Voltage Set	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal(external) power supply is turned on
(16)	EVR Register Set	0	1	0	0	0	Setting Data				Set the V_5 output level to the EVR register
(17)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power save Mode

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	D_7							D_0
0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 6 is a Icon display data area which available only for the D_0.

A0	D_7							D_0
0	1	0	1	1	*	A_2	A_1	A_0

(*:Don't Care)

A_2	A_1	A_0	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6

(c) Column Address

When MPU access the Display Data RAM, page address set(refer(b) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting.This counter auto-increments up to $(A0)_H$,but accessing to the display data RAM over than $(4F)_H$ is forbidden.

After writing 1 page data, page address setting is refuired due to page address increase automatical.

	A0	D_7							D_0
Higher Order	0	0	0	0	1	A_7	A_6	A_5	A_4
Lower Order	0	0	0	0	0	A_3	A_2	A_1	A_0

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				.				.
				.				.
0	1	0	0	1	1	1	1	4F

(d) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without any address setting after the start address setting.

A0	D_7		D_0
1	WRITE DATA		

(e) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	D_7						D_0
0	1	0	1	0	0	0	0	D

D 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

(f) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Data RAM is no changed by this instruction execution.

A0	D_7							D_0
0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"
1: Inverse RAM data "0" correspond to "On"

(g) Whole Display On

This instruction executes the all pixel terns on regardless the contents of the Display Data RAM. In this time, the contents of Display Data RAM is no change and is kept. This instruction takes over precedence over the "Normal or Inverse On/Off Set Instruction".

A0	D_7							D_0
0	1	0	1	0	0	1	0	D

D 0: Normal Display
1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the power save mode(refer to the (p) Power Save) .

5

(h) Icon Display

This instruction set the 1/49 duty for the Icon Display. The COMI terminal operate as COM_{48} and output the icon display data stored in D_0 of Display Data RAM page 6(refer to the Fig. 1).

A0	D_7							D_0
0	1	0	1	0	1	0	1	D

D 0: 1/48 Duty
1: 1/49 Duty

(i) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the Read Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction is executed, but the address is no change when the Display Data Read Instruction is executed. This status is continued during End instruction execution. When the End instruction is entered the column address back to the address where the Read Modify Write instruction entering. By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

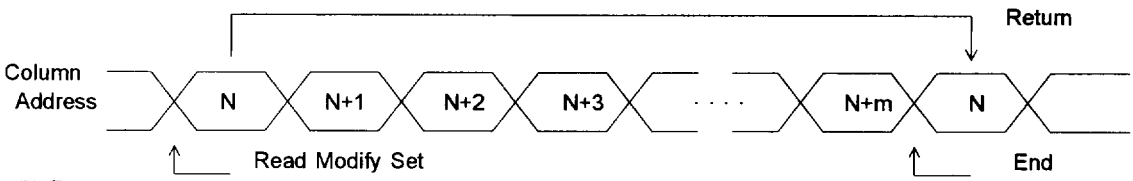
A0	D_7							D_0
0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

(j) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	D_7						D_0
0	1	1	1	0	1	1	1	0



(k) Reset

This instruction executes the following initialization.

Initialization

① Set the Address $(00)_H$ to the Column Address Counter.
② Set the page 0 to the Page Register.
③ Select the D_3 of the Output Assignment Register to 0.
④ Set $(00)_H$ to the EVR Register for the contrast control.

In this time, there are no influence to the Display Data RAM.

A0	D_7						D_0
0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal must be required for the initialization when the power terns on. Substitution of Reset Instruction for the reset signal input to the $\overline{RES}$ terminal is not allowed.

(l) Output Assignment Register

This instruction sets the Common Driver scanning order.

A0	D_7							D_0
0	1	1	0	0	A_3	*	*	*

(*:Don't Care)

A_3 : Set the Common Driver scanning order.(refer to 1-6)

(m) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is required.

A0	D_7							D_0
0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(n)LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 to V4 and output LCD driving waveform through the COM/SEG terminals.

A0	D_7						D_0
0	1	1	1	0	1	1	0	1

NJU6561 contains operational amplifiers for LCD bias voltage V1 to V4. These amplifiers current are reduced in order to realize low power consumption. Because of this reduction, LCD driving voltage V1 to V4 might be unstable just after the internal power supply is turned on.
LCD Driving Voltage Set instruction is prepared for this unstableness.

● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is tuned on/of.
When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence mentioned in (s) is required.

Turn ON sequence

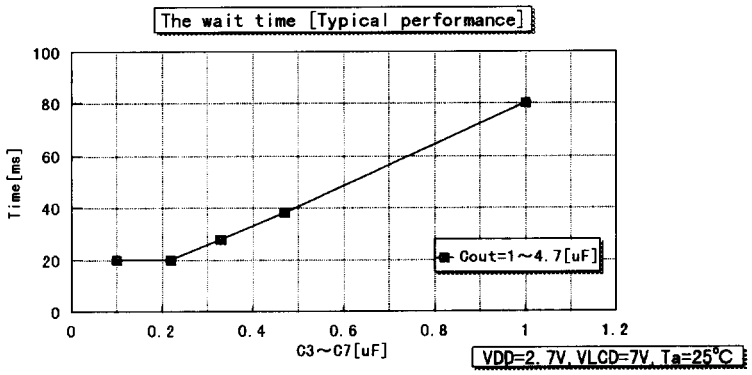
- Output Assign. Register Set
- Icon Display
- EVR Register Set
- Internal Power Supply ON or External Power supply ON
- (Wait Time) *2
- LCD Driving Voltage Set

Turn OFF sequence

- Display OFF
- Whole Display ON
- Internal Power Supply ON or External Power Supply ON

*1 This instruction is required in both cases of the internal and external power supply.
Until "LCD driving voltage Set" execution, NJU6561 operating current is higher than usual state and all COM/ SEG terminals output V_{DD} level continuously except LCD driving waveform.

*2 The wait time depends on the C_3 to C_7, C_{OUT} capasitors((4) (d)Fig.4), V_{DD} and V_{LCD} voltage.
Therefore a test on actual module should be practiced. Refer to the following graph.



(o) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this instruction execute, the internal Electrical Variable Resistor(EVR) to change the V_5 output voltage, generate, one voltage from 16 voltage state. The range of V_5 output level can be adjusted by the external resistance. For more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

A0	D_7							D_0
0	1	0	0	0	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	V_{LCD}
0	0	0	0	Low
	:			
	:			
1	1	1	1	High

$V_{LCD} = V_{DD} - V_5$

When EVR doesn't use, set the EVR register to (0,0,0,0).

(p) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits put on the power save mode and the operating current is reduced as same as stand by current.
The internal status in the Power Save Mode is as follows;

① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
③ Keeping the display data and operating mode as before the power save mode.
④ All of LCD driving bias voltage fixed to the V_{DD} level.

The power save and its release should be performed according to the following sequences.

Power Save Sequence

Display OFF
↓
Whole Display ON

Power Save Release Sequence

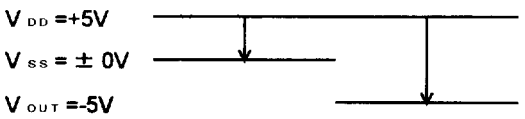
Normal Display
↓
Display ON
↓
(Wait Time)
↓
LCD Driving Voltage Set

*1 Power save mode requires dual-instruction. After the second instruction" whole Display ON", the power save mode starts.
*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.
*3 Until "LCD driving voltage set" execution, NJU6561 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.
*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.
*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

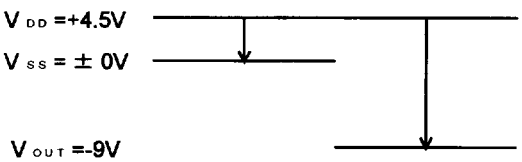
(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage(V_{DD} common) of the voltage V_{DD}-V_{SS} is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT}. In case of the voltage doubler operation, connect the two capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{OUT}, then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 4.5V.



Voltage Relation in Doubler



Voltage relation in Tripler

(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage can calculated by the following formula.

$$V_5 = V_{DD} - (1 + Rb/Ra) \cdot V_{REG} \quad \cdots\cdots ①$$

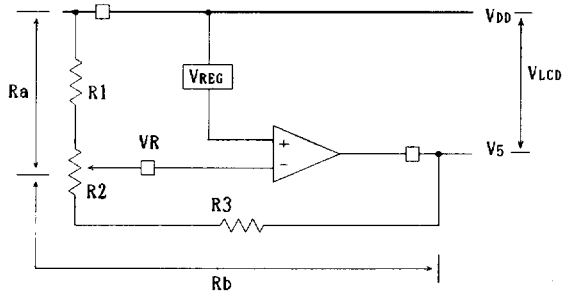


Fig. 3

Where, the V_{REG} is a constant voltage in the NJU6561 like as $V_{REG} \fallingdotseq 2.2V$.

To adjust the output voltage from V_5, connect the variable resistance among VR, V_{DD} and V_5 as shown in Fig. 3. When fine tuning for V_5 is needed, combine with the fixed resistance of R1, R3 and variable resistance of R2 is recommended as shown in Fig. 3.

Design example for R1, R2 and R3 (referrence)

- R1+R2+R3=5M Ω (Determined by the current flown between V_{DD}-V_5)
- Variable voltage range by the R2. -2.5V ~ -4.5V (V_{DD}-V_5 → 7V ~ 9V)
  (Determined by the LCD electrical characteristics)

R1, R2 and R3 are calculated by above conditions and the formula of ① to mentioned below;

R1=1.222M Ω
R2=0.349M Ω
R3=3.428M Ω

The voltage adjust circuits has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuits serially.

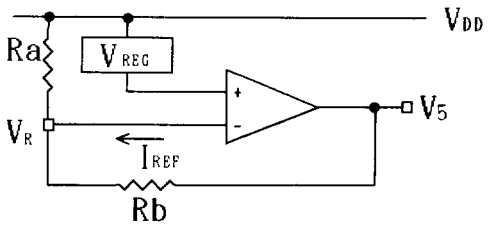
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_5 which controls LCD display contrast can adjust by the instruction. The EVR function is executed to set the 4 bits data into the EVR resistor and determine the one output voltage status out of 16 prefixed voltage status.

When execute the EVR function, set the T_1 and T_2 except the "H, H" and execute the Internal Power Supply On instruction.

[External parts constants setting example when EVR function using / reference]



(1) Determine the V_5 voltage range controlled by EVR.

LCD Driving Voltage V_{DD}-V_5 7V ~ 9V

The range of V_5 2V

(2) Determine the Rb.

Rb = [The range of V_5] / I_{REF} (16status I_{REF} ≒ 2.15 μA constant current)

Rb = 2V/2.15 μA = 0.93M Ω *Ta=25 °C V_{DD}-V_{OUT} =9V

(3) Adjust the Ra

$$Ra = \frac{V_{REG}}{([\text{LCD Driving Voltage}]-V_{REG})/Rb}$$

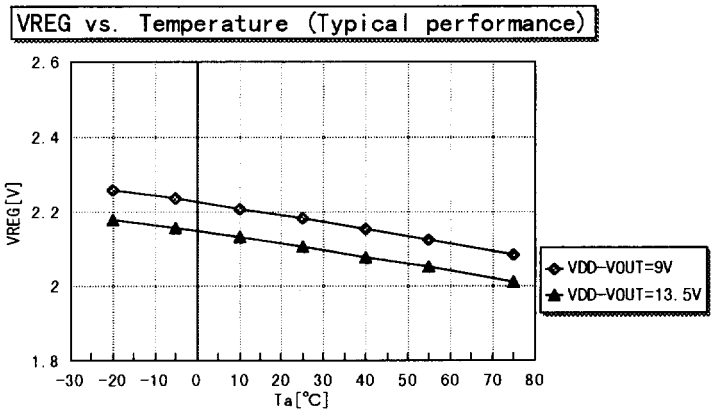
$$Ra = \frac{2.2\ V}{(7V-2.2V)/0.93M\ \Omega} = 0.43M\ \Omega$$

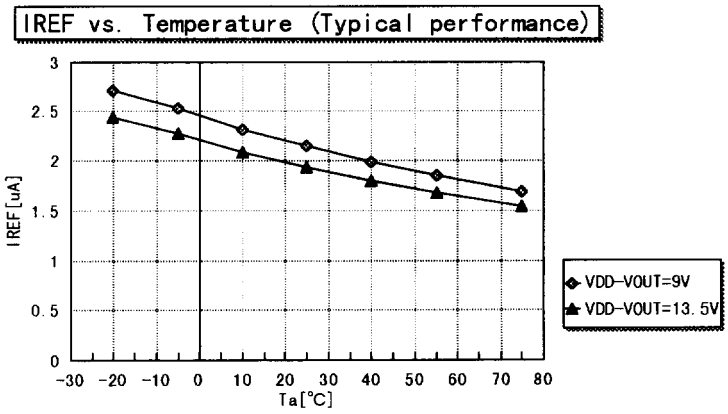
(4) Adjust the Ra

Adjust the Ra to good contrast of LCD display after the (D_3,D_2,D_1,D_0) of EVR register set to (1, 0, 0, 0) or (0, 1, 1, 1). When the EVR using, Ra use a variable resistance and contrast adjustment mentioned in (4) for each chip is required due to the I_{REF} is simple constant current source.

When the EVR function does not use, the (D_3,D_2,D_1,D_0) of EVR register set to (0, 0, 0, 0) by the RES signal or the EVR Register Set instruction.

*) V_{REG}, I_{REF} depends on the voltage between V_{DD} and V_{OUT}, the operating temperature. Please refer to the following graphs.





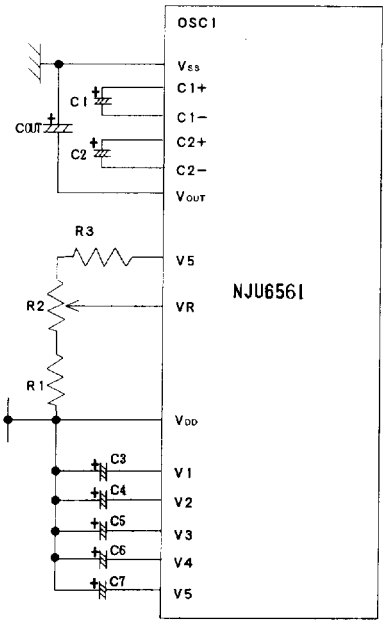
5

(d) LCD Driving Voltage Generation Circuits

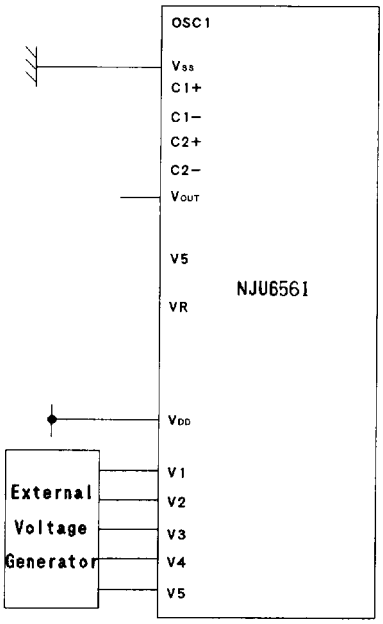
The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V_6 voltage by the bleeder resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 4. Five capacitors are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitors C3, C4, C5, C6 and C7 determine by combine with the actual LCD panel.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

$V_{DD}=V_{DD}-V5 \fallingdotseq 7 \sim 9$ V

Item	value
Cout	4.7~10μF
C1,C2	4.7~10μF
C3 to C7	0.1~4.7μF
R1	1.222MΩ
R2	0.349MΩ
R3	3.428MΩ

Fig. 4

*1 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.

*2 Following connection of V_{OUT} is required when external power supply using.

When $V_{SS} > V_6$ – $V_{OUT} = V_6$

When $V_{SS} \leqq V_6$ – $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type and the operation

NJU6561 is interfaced by using the serial interface.

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to $\overline{CS}$="L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal are MSB first like as the order of D_7 to D_0 and the data are entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or $\overline{CS}$ terminal becomes "H" in spite of the data less then 8 bits, NJU6561 recognizes wrong data as a instruction data. Therefore 8bits data is required for the input data. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface .

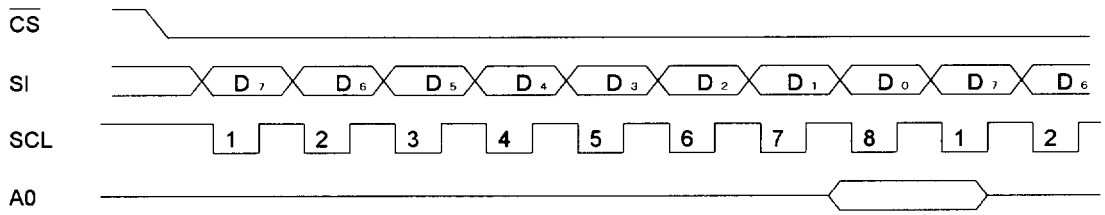


Fig. 5

(5-2) Access to the Display Data RAM and Internal Register.

The NJU6561 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6561 is available because of the limitation of access time of NJU6561 locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP operation cycle which equivalent to the waiting operation is useful.

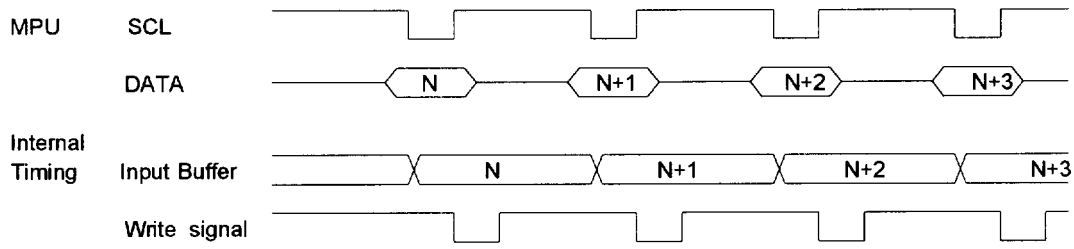


Fig. 6

(5-3) Chip Select

$\overline{CS}$ is Chip Select terminal. The Chip Select is executed by the setting of $\overline{CS}$="L". Only the select mode, the interface with MPU is available. In the non select period, A0, SI and SCL input are put on the disable state, and, the shift register and counter are reset. The reset input is regardless with the condition of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25 ℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 4.5 (used Tripler)	V
Supply Voltage (2)	V_5	V_{DD}-13.5 ~ V_{DD}+0.3	V
Supply Voltage (3)	V_1~V_4	V_5 ~ V_{DD}+0.3	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	℃
Storage Temperature	Tstg	- 55 ~ + 125 (Chip) - 55 ~ + 100 (TCP)	℃

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1)

(V_{DD} =5V ± 10%, V_{SS} =0V, Ta=-20 ~ +75 ℃)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage (1)	Recommend	V_{DD}			4.5	5.0	5.5	V	
	Available				2.4		5.5		5
Operating Voltage (2)	Recommend	V_5			V_{DD}-13.5		V_{DD}-3.5	V	
	Available				V_{DD}-13.5				
	Available	V_1, V_2	$V_{LCD}=V_{DD}-V_5$		V_{DD}-0.6xV_{LCD}		V_{DD}		
	Available	V_3, V_4			V_5		V_{DD}-0.4xV_{LCD}		
Input Voltage	1	V_{IHC1}	A0, $\overline{CS}$, $\overline{RES}$, SI, SCL Terminals		0.7xV_{DD}		V_{DD}	V	
		V_{IHC2}		V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
	2	V_{ILC1}			V_{SS}		0.3xV_{DD}		
		V_{ILC2}		V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		
Input Leakage Current		I_{LI}	All input terminals		-1.0		1.0	uA	
Driver On-resistance		R_{ON1}	Ta=25℃	V_{LCD}=13.5V		2.0	3.0	kΩ	6
		R_{ON2}		V_{LCD}=8.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	during Powersaye Mode			0.05	5.0	uA	
Operating Current		I_{DD12}	Display			28	45	uA	7
		I_{DD14}	V_{LCD}=8.0V	V_{DD}=2.7V		16	25		
		I_{DD21}	Accessing fcyc=200kHz			350	500	uA	8
		I_{DD22}		V_{DD}=2.7V		170	240		

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■ ELECTRICAL CHARACTERISTICS (2)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Input Terminal Capacitance		C_{IN}	A0, $\overline{CS}$, $\overline{RES}$, SI, SCL, T1, T2 Terminals Ta=25°C			10		pF	
Oscillation Frequency		fosc	Ta=25°C	V_{DD}=5.0V	15	18	21	kHz	
				V_{DD}=2.7V	11	16	21		
Voltage Tripler	Input Voltage	V_{DD1}	V_{DD}-V_{SS}		2.4		5.5	V	
		V_{DD2}	V_{DD}-V_{SS} used Tripler		2.4		4.5		9
	Output Volt.	V_{OUT}	V_{SS}-V_{LCD}, used Tripler		-9.0			V	
	On -resistance	R_{TRI}	V_{DD}=3V; C=4.7uF used Tripler			600	1000	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Tripler Circuit "OFF"		V_{DD}-13.5		V_{DD}-5.0	V	10
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"		V_{DD}-13.5		V_{DD}-5.0	V	
	Operating Current	I_{OUT1}	V_{DD}=4.5V, V_{LCD}=8V COM/SEG Term. Open, No Access Display check. pattern			70	T.B.D.	mA	11
		I_{OUT2}				30	T.B.D.		
		I_{OUT3}				25	T.B.D.		
	Voltage Reg.	V_{REG}	V_{DD}-V_{out}=9V; Ta=25°C		T.B.D.	2.2	T.B.D.	V	12
	Reference Current	I_{REF}	V_{DD}-V_{out}=9V; Ta=25°C		1.50	2.15	2.80	uA	

Note 5) NJU6561 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 7,8,11)Apply to current after "LCD Driving Voltage set".

Note 7) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 8) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DDTX}.

Note 9) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 10) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

Note 11) Each operating current of voltage supply circuits block is specified under below table conditions.

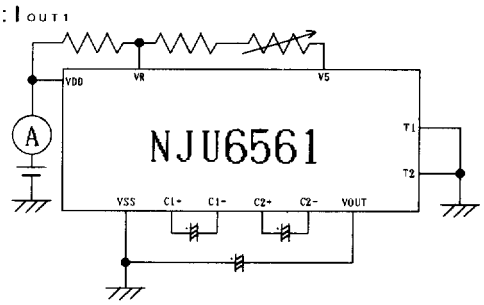
SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T1	T2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT}, V_5)

* = Don't Care

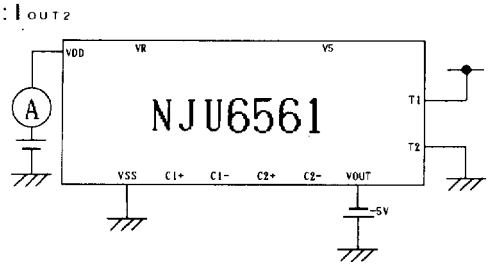
Note 12)Apply to the precision of Voltage on each EVR steps.

MEASUREMENT BLOCK DIAGRAM

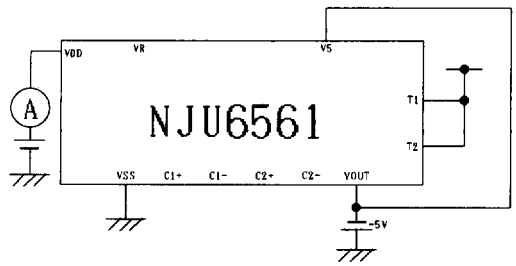
: I_{OUT1}



: I_{OUT2}



: I_{OUT3}

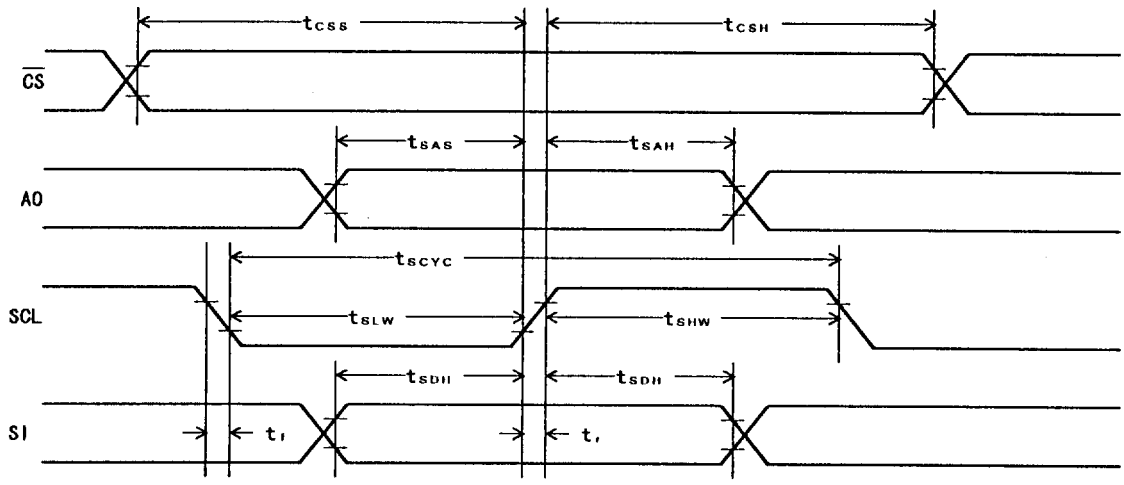


■ ELECTRICAL CHARACTERISTICS (3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	13
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	14

Note 13) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 14) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

■ MPU INTERFACE TIMING CHARACTERISTICS



(V_{DD} =5.0V ± 10%, Ta=-20 ~ 75 °C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	500			ns
SCL "H" pulse width		t_{SHW}	150			
SCL "L" pulse width		t_{SLW}	150			
Address Set Up Time	A0 Terminal	t_{SAS}	120			
Address Hold Time		t_{SAH}	200			
Data Set Up Time	SI Terminal	t_{SDS}	120			
Data hold Time		t_{SDH}	50			
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	t_{CSS}	30			
		t_{CSH}	400			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	t_r, t_f		15		

(V_{DD} =2.7V ~ 4.5V, Ta=-20 ~ 75 °C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	1000			ns
SCL "H" pulse width		t_{SHW}	300			
SCL "L" pulse width		t_{SLW}	300			
Address Set Up Time	A0 Terminal	t_{SAS}	250			
Address Hold Time		t_{SAH}	400			
Data Set Up Time	SI Terminal	t_{SDS}	250			
Data hold Time		t_{SDH}	100			
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	t_{CSS}	60			
		t_{CSH}	800			
Rise Time, Fall Time	SCL, A0, $\overline{CS}$ SI, Terminals	t_r, t_f		15		

Note 15) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 16) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

■ LCD DRIVING WAVEFORM

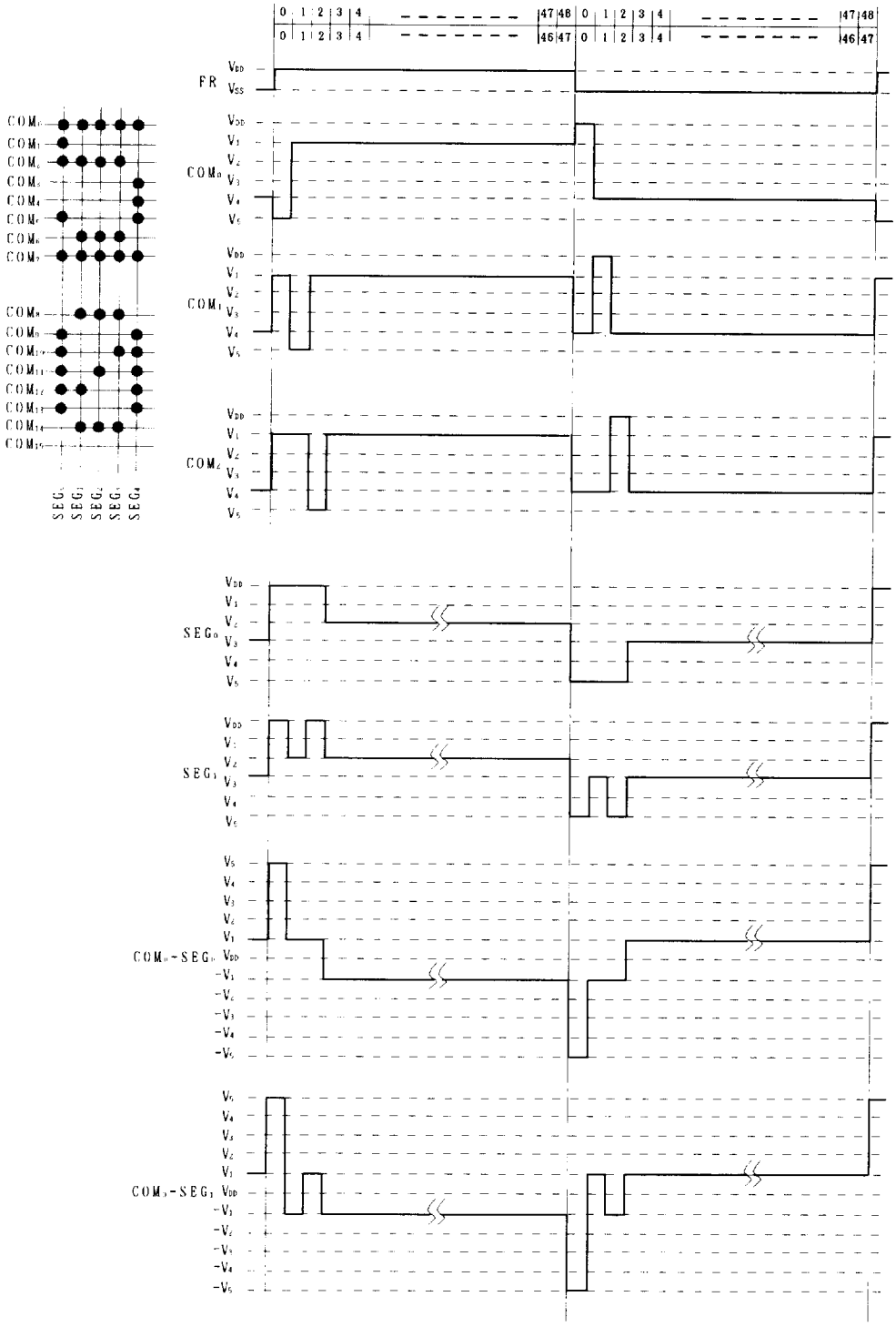
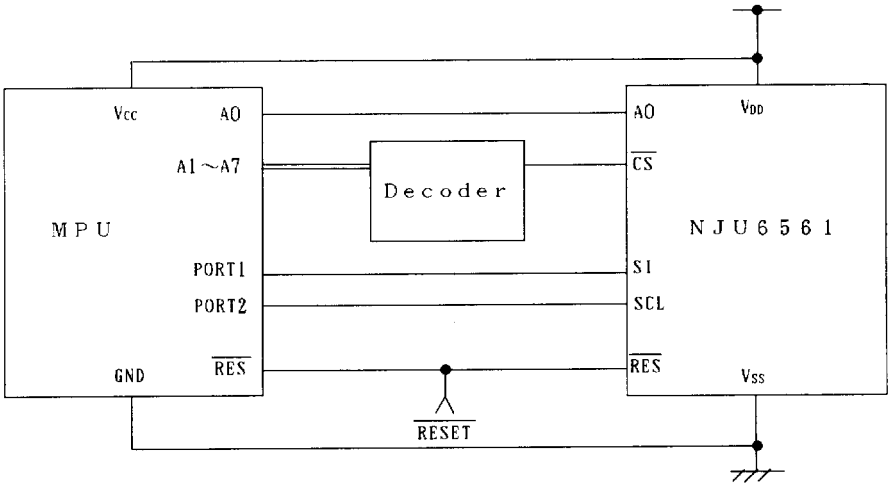


Fig.7.

■ APPLICATION CIRCUIT

·Microprocessor Interface Example

NJU6561 is interfaced by using the serial interface.
Therefore minimum wiring for the MPU interface is available.



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