

1/4 DUTY LCD DRIVER

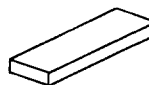
GENERAL DESCRIPTION

The NJU6439 is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 40-segment drives up to 160 segments.

The rectangle outline is useful the COG applications.

PACKAGE OUTLINE



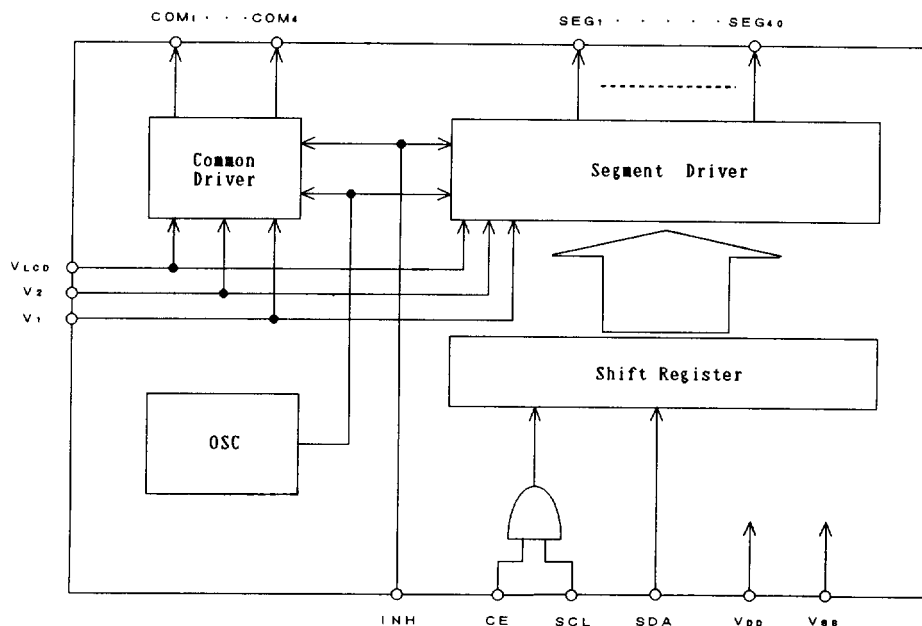
FEATURES

- 40 Segment Drivers
- Duty and Bias Ratio : 1/4Duty, 1/3Bias (up to 160 segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip
- Display Off Function (INH Terminal)
- Operating Voltage — 2.4~3.6V
- LCD Driving Voltage — 6.0V Max.
- Package Outline — Chip / Bumped Chip
- C-MOS Technology

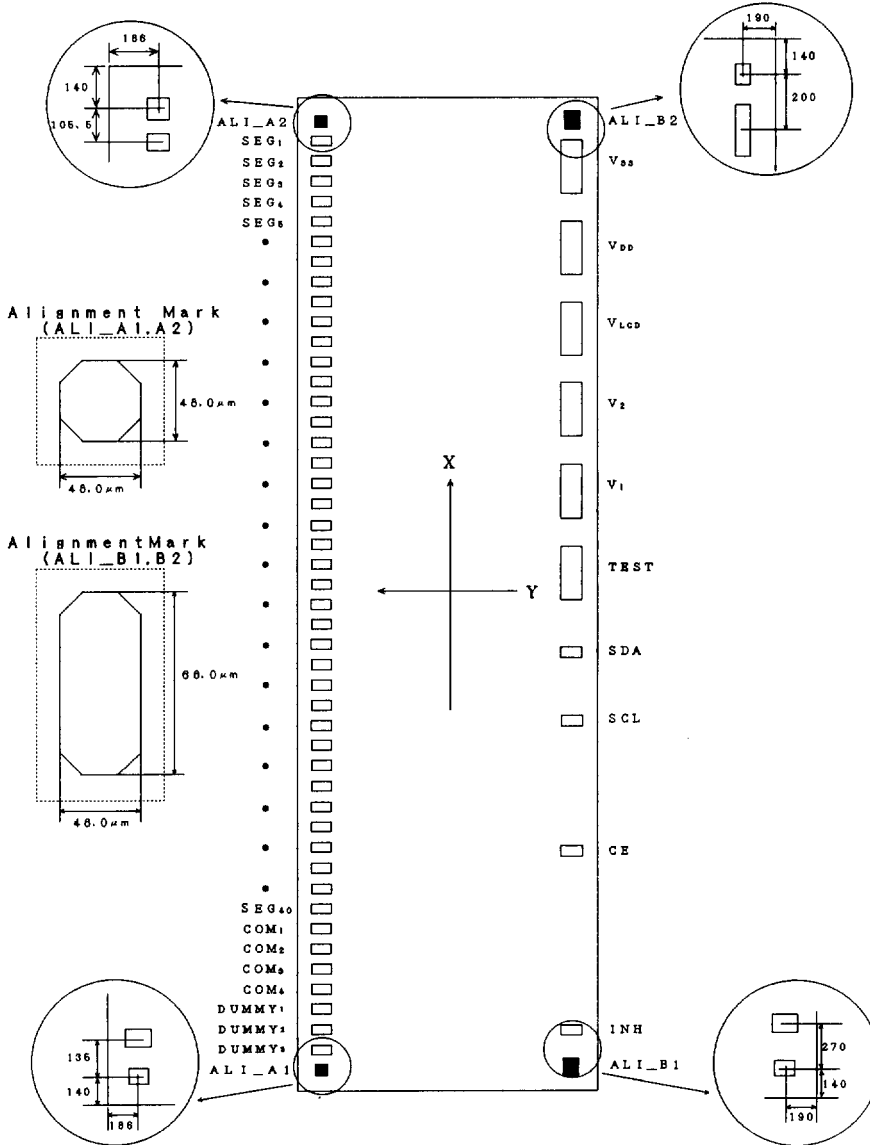
NJU6439C

5

BLOCK DIAGRAM



PAD LOCATION



Chip size : 5.12mm x 1.56mm

Chip center : X=0μm, Y=0μm

Chip thickness : 400±30μm

Pad size : 50μm x 100μm

V₁, V₂, V_{LCD}, V_{DD}, V_{SS} Terminal is 250μm x 100μm

Bump height : 25μmTYP.

Bump material : Au

■:4th Mark is the Alignment Mark.

The Alignment Mark is useful the COG Assembly.

■ COORDINATES

Chip Size 5.12x1.56mm(Chip Center X=0 μ m, Y=0 μ m)

No	PAD NAME	X=(μ m)	Y=(μ m)	No	PAD NAME	X=(μ m)	Y=(μ m)
1	INH	-2150.0	- 590.0	32	SEG ₂₂	214.5	594.0
2	CE	-1240.0	- 590.0	33	SEG ₂₃	114.5	594.0
3	SCL	- 494.0	- 590.0	34	SEG ₂₄	14.5	594.0
4	SDA	- 178.0	- 590.0	35	SEG ₂₅	- 85.5	594.0
5	TEST	206.0	- 590.0	36	SEG ₂₆	- 185.5	594.0
6	V _I	660.0	- 590.0	37	SEG ₂₇	- 285.5	594.0
7	V ₂	1040.0	- 590.0	38	SEG ₂₈	- 385.5	594.0
8	V _{LCD}	1430.0	- 590.0	39	SEG ₂₉	- 485.5	594.0
9	V _{DD}	1820.0	- 590.0	40	SEG ₃₀	- 585.5	594.0
10	V _{SS}	2220.0	- 590.0	41	SEG ₃₁	- 685.5	594.0
11	SEG ₁	2314.5	594.0	42	SEG ₃₂	- 785.5	594.0
12	SEG ₂	2214.5	594.0	43	SEG ₃₃	- 885.5	594.0
13	SEG ₃	2114.5	594.0	44	SEG ₃₄	- 985.5	594.0
14	SEG ₄	2014.5	594.0	45	SEG ₃₅	-1085.5	594.0
15	SEG ₅	1914.5	594.0	46	SEG ₃₆	-1185.5	594.0
16	SEG ₆	1814.5	594.0	47	SEG ₃₇	-1285.5	594.0
17	SEG ₇	1714.5	594.0	48	SEG ₃₈	-1385.5	594.0
18	SEG ₈	1614.5	594.0	49	SEG ₃₉	-1485.5	594.0
19	SEG ₉	1514.5	594.0	50	SEG ₄₀	-1585.5	594.0
20	SEG ₁₀	1414.5	594.0	51	COM ₁	-1685.5	594.0
21	SEG ₁₁	1314.5	594.0	52	COM ₂	-1785.5	594.0
22	SEG ₁₂	1214.5	594.0	53	COM ₃	-1885.5	594.0
23	SEG ₁₃	1114.5	594.0	54	COM ₄	-1985.5	594.0
24	SEG ₁₄	1014.5	594.0	55	DUMMY1 ※	-2085.5	594.0
25	SEG ₁₅	914.5	594.0	56	DUMMY2 ※	-2185.5	594.0
26	SEG ₁₆	814.5	594.0	57	DUMMY3 ※	-2285.5	594.0
27	SEG ₁₇	714.5	594.0		ALI_A1	-2420.0	594.0
28	SEG ₁₈	614.5	594.0		ALI_A2	2420.0	594.0
29	SEG ₁₉	514.5	594.0		ALI_B1	-2420.0	- 590.0
30	SEG ₂₀	414.5	594.0		ALI_B2	2420.0	- 590.0
31	SEG ₂₁	314.5	594.0		—	—	—

※DUMMY PAD

■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1	INH	Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-Off "L" : Display-On
2	CE	Chip Enable Signal Input Terminal : "H" : LCD display data "L" : Disable
3	SCL	Serial Data Transmission Clock Input Terminal : LCD display data are input synchronized SCL clock signal rise edge.
4	SDA	Serial Data Input Terminal Data input timing : SCL clock rise edge
6	V ₁	LCD Driver Voltage Adjust Terminal
7	V ₂	LCD Driver Voltage Adjust Terminal
8	V _{LCD}	Power Supply for LCD Driving
9	V _{DD}	Power Supply (+3V)
10	V _{SS}	Power Supply (0V)
11~50	SEG ₁ ~ SEG ₄₀	LCD Segment Output Terminals
51~54	COM ₁ ~ COM ₄	LCD Common Output Terminals

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit :

This circuits supply the basical clock signal to other circuits like as common driver and segment driver.

(1-2) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-3) Common Divider Circuit

This circuit divides the oscillating signal to generate the common timing.

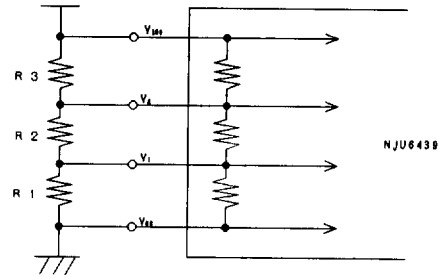
(1-4) Segment Divider Circuit

This circuit divides the oscillating signal to generate the segment timing.



(1-5) The LCD Driver Voltage Adjust circuit

The incorporate Bleeder Resistance sets 1/3 bias, and LCD Driver ability can be increased by connecting external resistance.



(2) Display Data input timing, correspond to segment and common terminal

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

When the power is turned on, whole data in the shift-resister are "L".

※ Whole 160bits data transfer to the shift register. When the input data in less than 160bits, parts which bit data is inputted corresponded to display, and segment which correspond to the rest part in "off".

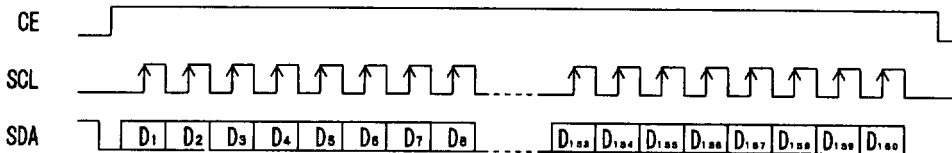
In care of over then 160bits, front 160bits from fall edge of "CE" signal is valid.

• Input data correspond to Segment Status

The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

Data (D1...D160)	Segment Status
"H"	ON
"L"	OFF

• Display Data Correspond to Segment Status



• Display Data Correspond to Segment and Common Terminals

Segment	Data	COM ₁	COM ₂	COM ₃	COM ₄
SEG ₁	D ₁ D ₂ D ₃ D ₄	○	○	○	○
SEG ₂	D ₅ D ₆ D ₇ D ₈	○	○	○	○
⋮	⋮	⋮	⋮	⋮	⋮
SEG ₃₉	D ₁₅₃ D ₁₅₄ D ₁₅₅ D ₁₅₆	○	○	○	○
SEG ₄₀	D ₁₅₇ D ₁₅₈ D ₁₅₉ D ₁₆₀	○	○	○	○

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Operating Voltage (1)	V _{DD}	-0.3 ~ +7.0	V
Operating Voltage (2)	V _{LCD}	0 ~ +7.0	V
Operating Voltage (3)	V ₁ , V ₂	0 ~ +7.0	V
Input Voltage	V _{IN}	-0.3 ~ V _{DD}	V
Operating Temperature	T _{OP}	-20 ~ +75	°C
Storage Temperature	T _{stg}	-55 ~ +125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V

Note 3) The relation: V_{LCD} ≥ V₂ ≥ V₁ ≥ V_{SS} must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=25°C, V_{DD}=3.0V, V_{SS}=0V, V_{LCD}=6.0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	Recommend V _{DD}	V _{DD} Terminal	2.4	3.0	3.6	V	
	Available V _{DD}	V _{DD} Terminal	2.4	3.0	5.5	V	
Operating Voltage (2)	V _{LCD}	V _{LCD} Terminal	2.0		6.0	V	
Operating Voltage (3)	V ₂	V ₂ Terminal	V ₁	2/3V _{LCD}	V _{LCD}	V	
Operating Voltage (4)	V ₁	V ₁ Terminal	0.7	1/3V _{LCD}	V ₂	V	
"H" Input Voltage	V _{IH}	CE, SCL, SDA, INH Terminals	0.7V _{DD}		V _{DD}	V	
"L" Input Voltage	V _{IL}	CE, SCL, SDA, INH Terminals	V _{SS}		0.3V _{DD}	V	
"H" Input Current	I _{IH}	CE, SCL, SDA, INH Terminals V _{IN} =V _{DD}			5	μA	
"L" Input Current	I _{IL}	CE, SCL, SDA, INH Terminals V _{IN} =V _{SS}			5	μA	
"H" Output Voltage (1)	V _{OH} (1)	SEG ₁ ~SEG ₄₀ Term, I _O = -1 μA	V _{LCD} -0.6			V	5
"L" Output Voltage (1)	V _{OL} (1)	SEG ₁ ~SEG ₄₀ Term, I _O = 1 μA			V _{DD} +0.6	V	5
Middle Level Voltage 1/3 (1)	V _{MS1/3}	SEG ₁ ~SEG ₄₀ Term, I _O =±1 μA	1/3V _{LCD} -0.6	1/3V _{LCD}	1/3V _{LCD} +0.6	V	5
Middle Level Voltage 2/3 (1)	V _{MS2/3}	SEG ₁ ~SEG ₄₀ Term, I _O =±1 μA	2/3V _{LCD} -0.6	2/3V _{LCD}	2/3V _{LCD} +0.6	V	5
"H" Output Voltage (2)	V _{OH} (2)	COM ₁ ~COM ₄ Term, I _O = -30 μA	V _{LCD} -0.6			V	6
"L" Output Voltage (2)	V _{OL} (2)	COM ₁ ~COM ₄ Term, I _O = 30 μA			V _{SS} +0.6	V	6
Middle Level Voltage 1/3 (2)	V _{MC1/3}	COM ₁ ~COM ₄ Term, I _O = ±1 μA	1/3V _{LCD} -0.6	1/3V _{LCD}	1/3V _{LCD} +0.6	V	6
Middle Level Voltage 2/3 (2)	V _{MC2/3}	COM ₁ ~COM ₄ Term, I _O = ±1 μA	2/3V _{LCD} -0.6	2/3V _{LCD}	2/3V _{LCD} +0.6	V	6
"L" Output Voltage (3)	V _{OL} (3)	SDA I _O = 30mA			V _{SS} +0.4	V	6
Operating Current (1)	I _{DD}	V _{DD} Terminal V _{DD} =3.0V V _{LCD} OPEN		15		μA	7
Operating Current (2)	I _{LCD}	V _{LCD} Terminal V _{DD} =3.0V V _{LCD} =6.0V		18		μA	8
Hysteresis Voltage	V _H	SCL Terminal, V _{DD} =3.0V	0.3			V	

Note 5) Segment terminals except measurement terminal are open.

Note 6) Common terminals except measurement terminal are open.

Note 7) CE, SCL, SDA terminals are connected V_{SS}. /INH terminal is connected V_{DD}. /TEST terminal is open.

Note 8) CE, SCL, SDA, INH terminals are measurement terminal are connected V_{SS}. /TEST terminal is open.

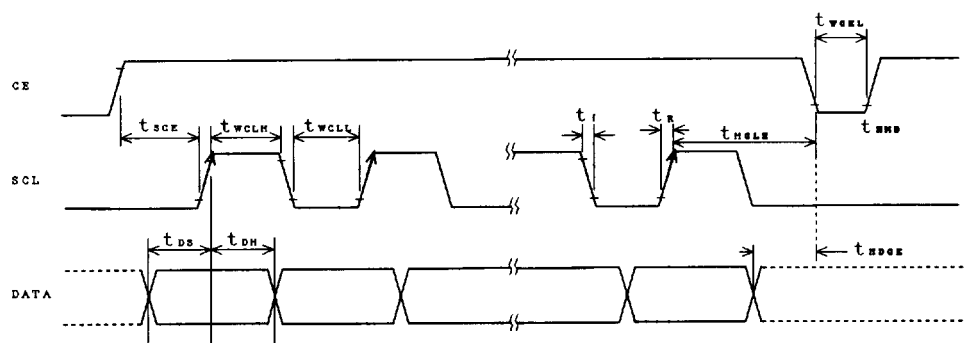


AC Characteristics

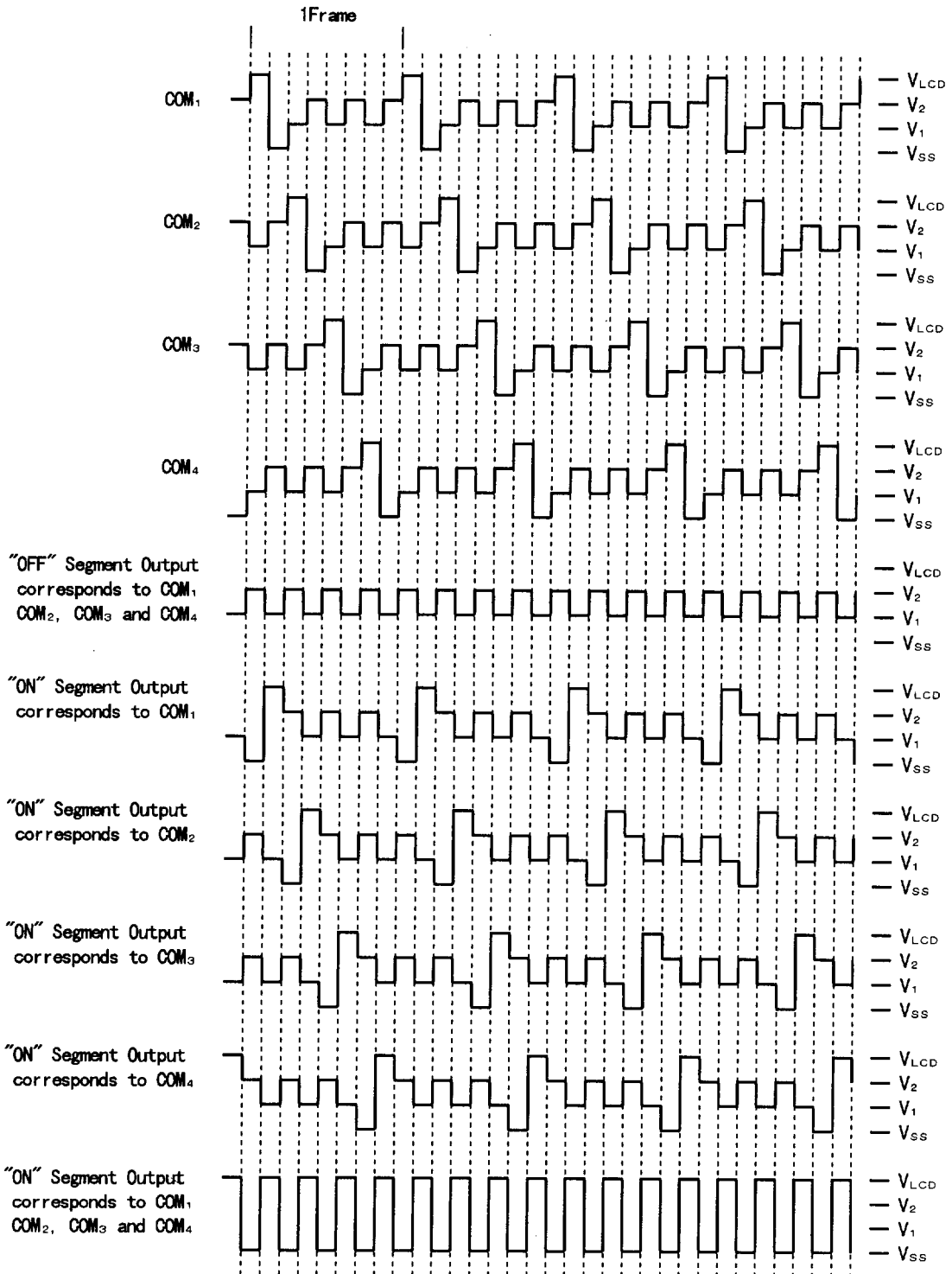
($T_a=25^{\circ}\text{C}$, $V_{DD}=3.0\text{V}$, $V_{SS}=0\text{V}$, $V_{LCD}=6.0\text{V}$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{WCLL}	SCL	0.25	—	—	μs
"H" Clock Pulse Width	t_{WCLH}	SCL	0.25	—	—	μs
Data Set-up Time	t_{DS}	SDA, SCL	0.25	—	—	μs
Data Hold Time	t_{DH}	SCL	0.25	—	—	μs
CE Set-up Time	t_{SCE}	CE, SDA	1.25	—	—	μs
CE Hold Time	t_{HCE}	SCL, CE	1.25	—	—	μs
"L" CE Pulse Width	t_{WCEL}	CE	4.00	—	—	μs
Frame Frequency	f_o	COM ₁ ~ COM ₄ , SEG ₁ ~ SEG ₄₀	—	70	—	

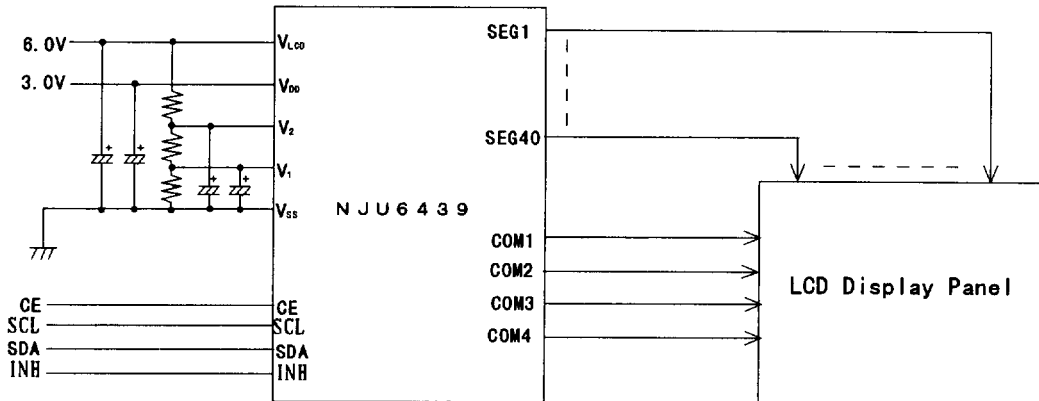
Input Timing Characteristics



■ LCD Driving Waveform(1/4DUTY - 1/3BIAS)



APPLICATION CIRCUIT



(Note) The internal display data is undefined when V_{DD} is just turned on.

To avoid the meaningless display, please keep the INH terminal at "H" until proper display data has been transferred.

In order to set the initial condition, 160-bit blank data or the first 160-bit data to be displayed should be transferred.