



ON SCREEN DISPLAY MIX IC

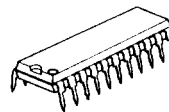
■ GENERAL DESCRIPTION

NJM2252 is the IC that has been developed for VCR application, which has the super-impose function as well as the function to drive the S-VHS, S-output pin by putting the external transistor.

NJM2252 has Y signal pin and C signal pin of each independent circuit in it. Y signal line is selectable of 4 inputs, and C signal line is selectable of 3 inputs, each by the inside switches.

Further more, it has function to adjust the output level of S-VHS, Spin.

■ PACKAGE OUTLINE



NJM2252L

■ FEATURES

- 9V spec. (Recommended operational voltage range 8.6~9.4V)
- Voltage gain can be controlled by the external resistor (Typ. ± 3 dB)
- Wide band (Y signal line 10MHz, C signal line 8MHz)
- Output sag. correction circuit incorporated (Y signal line)
- Video switch incorporated (Y signal line 4 input, C signal line 3 input)
- Clamp circuit (Y signal line) Bias circuit (C signal line) incorporated
- Package Outline SDIP22
- Bipolar Technology

■ APPLICATION

- VCR (Correspond to S-VHS)
- Laser Disc

■ PIN FUNCTION

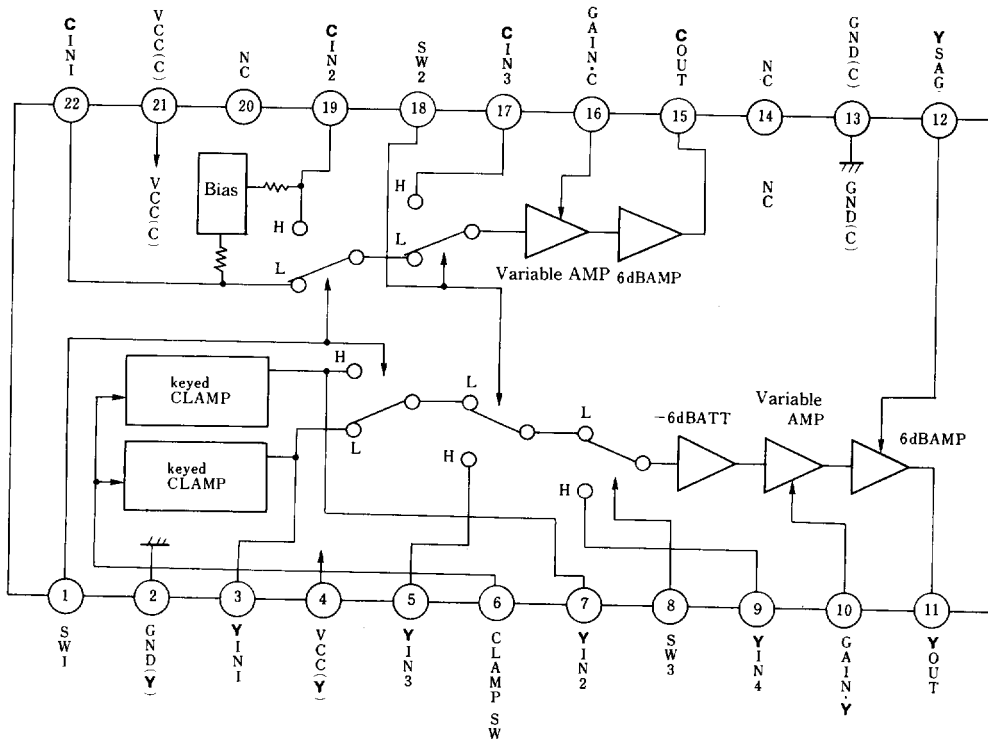
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	SW1	12	Y Line Sag Correction Pin
2	GND (Y Line)	13	GND (C Line)
3	Y Line Input Pin	14	NC
4	V ⁺ (L Line)	15	C Line Output Pin
5	Y Line Input Pin 3	16	c Line Gain Control
6	Clamp SW	17	c Line Input Pin 3
7	Y Line Input Pin	18	SW 2
8	SW 3	19	C Line Input Pin
9	Y Line Input Pin 4	20	NC
10	Y Line Gain Control	21	V ⁺ (C Line)
11	Y Line Output Pin	22	C Line Input Pin 1

■ RECOMMENDED OPERATING CONDITION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Supply Voltage Range	V ⁺		8.6	9.0	9.4	V
Y Signal Input Amplitude Range		Y _{IN}	—	—	3.0	V _{p.p}
Y Signal Output Amplitude Range		Y _{OUT}	—	—	3.0	V _{p.p}
C Signal Input Amplitude Range		C _{IN}	—	—	2.0	V _{p.p}
C Signal Output Amplitude Range		C _{OUT}	—	—	2.5	V _{p.p}
Gain Control Voltage Range		TP10, TP21 Input Voltage	2.0	—	3.0	V



■ BLOCK DIAGRAM



NJM2252L



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V*	12	V
Power Dissipation	P _D	700	mW
Operating Temperature Range	T _{opr}	-20~+75	°C
Storage Temperature Range	T _{stg}	-40~+125	°C

■ ELECTRICAL CHARACTERISTICS

(V*: 9V, V_C: 5V, TP10, TP21: 2.5V, Ta: 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I _{CC}	4pin, 21pin Sink Current	25	37	45	mA

Y Signal Line

Input Open Voltage	V _{if}	TP1, TP2: Measurement	4.0	4.1	4.2	V
Output Open Voltage	V _{oy}		3.60	3.95	4.30	V
Output Offset Voltage 1	V _{ofy}	TP1, 2, 2: 5V, TP5: Measurement	-20	—	20	mV
Output Offset Voltage 2	V _{ofy}	TP1, 4: 5V, TP5: Measurement	-10	20	50	mV
Clamp Sink Current	I _i	V _C : 5V, SW4: 2 Measurement	0.8	1.0	1.2	mA
Voltage Gain	G _{vy1}	Y _{IN} : 1MHz CW wave, Y _{OUT} : 2.0V _{P-P}	-0.5	0.5	1.5	dB
Voltage Gain Variable Width	G _{vy}	Y _{IN} : 1MHz CW Wave, Y _{OUT} : 2.0V _{P-P}	-2.0	—	2.0	dB
Frequency Gain	G _{fy}	10MHz/1MHz	-1.0	—	1.0	dB
Sag Gain	G _{ys}	TP16: 100kHz, 50mV _{P-P} V _{OUT} : Measurement	15	20	—	dB
Differential Gain	DG	Y _{OUT} : 2.0V _{P-P} Standard Staircase Signal	—	1.0	3.0	%
Differential Phase	DP	Y _{OUT} : 2.0V _{P-P} Standard Staircase Signal	—	1.0	—	deg
Crosstalk	CT _y	Y _{IN} : 4.43MHz, 2.0V _{P-P} CW Wave Input	—	-70	—	dB
Output Impedance	R _{oy}		—	6	—	Ω

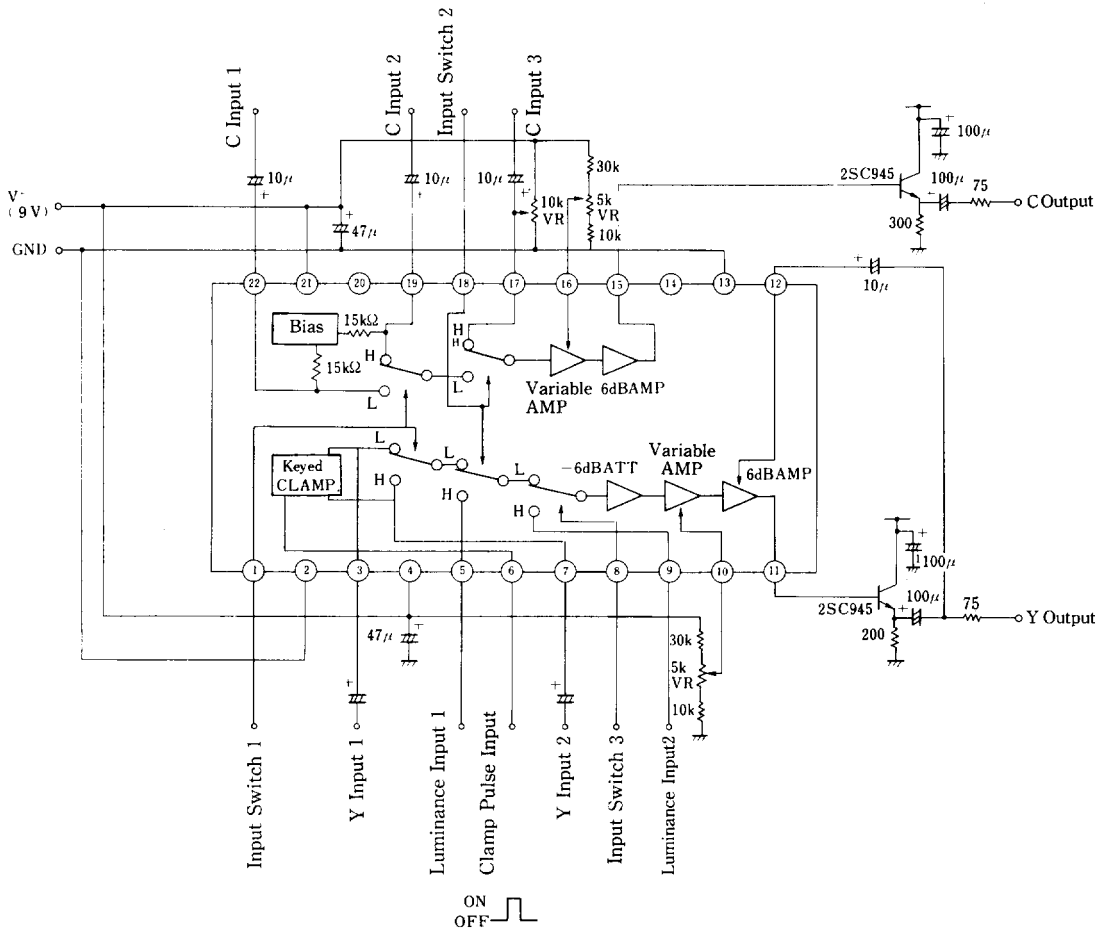
C Signal Line

Input Open Voltage	V _{ic}	TP6, TP7: Measurement	3.9	4.1	4.3	V
Output Open Voltage	V _{oc}	TP21: 2.5V	5.05	5.35	5.65	V
Output Offset Voltage	V _{ofc}	TP6, 7, 8: 5.0V, TP9: Measurement	-50	—	50	mV
Voltage Gain	G _{vc1}	C _{IN} : 1MHz CW Wave, C _{OUT} : 2V _{P-P}	6.0	7.0	8.0	dB
Voltage Gain Variable Width	G _{vc}	C _{IN} : 1MHz CW Wave, C _{OUT} : 2V _{P-P}	4.5	—	8.5	dB
Frequency Gain	G _{fc}	8MHz/1MHz	-1.0	—	1.0	dB
Crosstalk	C _{tc}	C _{IN} : 4.43MHz, 1.0V _{P-P} CW Wave Input	—	-70	—	dB
Input Impedance	R _{ic}	19pin, 22pin Input Impedance	11	15	19	Ω
Output Impedance	R _{oc}		—	6	—	Ω

Common Line

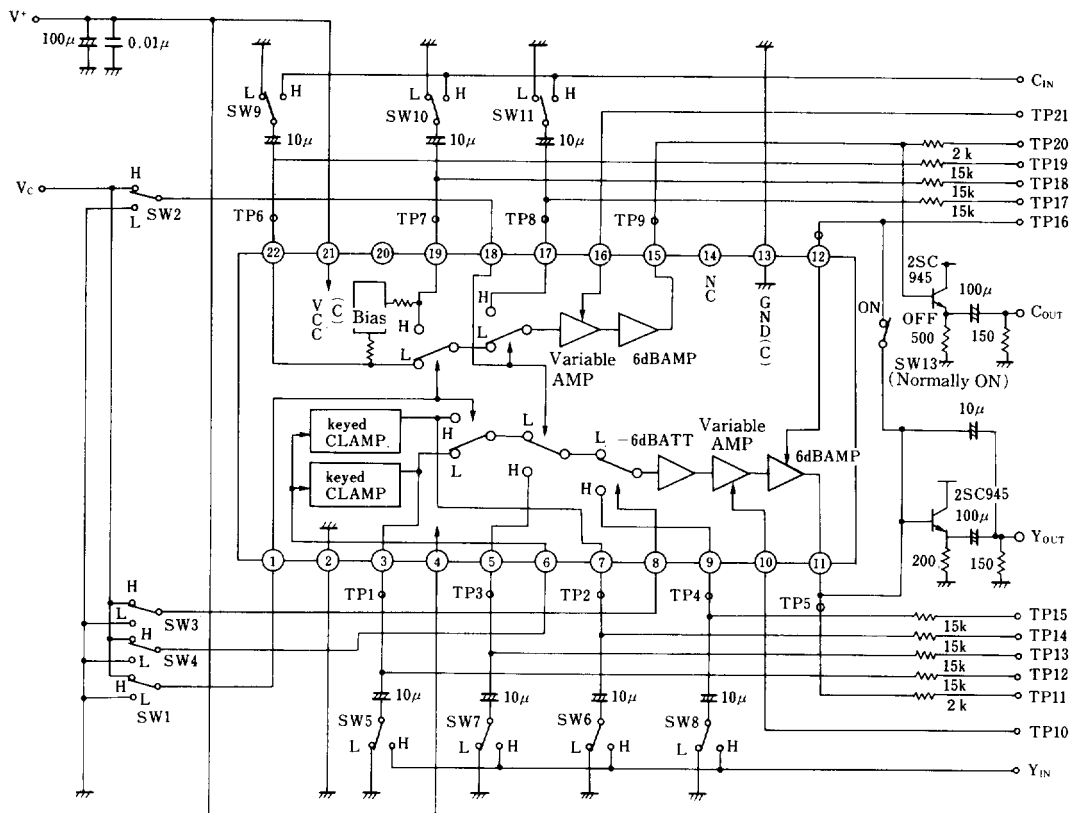
Control On Voltage	V _{c1}	Inner Switch on Level Guarantee	2.5	—	—	V
Control Off Voltage	V _{c2}	Inner Switch Off Level Guarantee	—	—	1.5	V
Key Clamp Control Voltage	V _{c3}	1 Pin Threshold Voltage	1.5	2.0	2.5	V

■ APPLICATION CIRCUIT





■ TEST CIRCUIT



■ VIDEO SWITCHING MOTION

SW1	SW2	SW3	Y LINE OUTPUT	C LINE OUTPUT
L	L	L	Yin1	Cin1
H	L	L	Yin2	Cin2
*	H	L	Yin3	Cin3
L	L	H	Yin4	Cin1
H	L			Cin2
*	H			Cin3

*:H or L



■ TERMINAL FUNCTION

PIN	PIN NAME	SYMBOL	FUNCTION
1	SW1	SW1	Video switch channel change over input. The L level is identified to be input when being left on at open state.
2	GND (Y Line)	GND Y	
3	Y Line Input Pin	Yin1	Video signal input pin (Y line) Key Clamp circuit internalized. The clamp function goes on when the key clamp is on H timing. Keyed clamp at L position indicates the normal sink chip clamp on operation. The clamp voltage is about 4.1V.
4	V _{CC} (Y Line)		Y line alone can not be used when C line supply voltage is off state.
5	Y Line Input Pin 3	Yin 3	Video signal input pin (Y line) The IC does not have bias or clamp function circuit in it, and its easy to have the external circuit, of the brightness level setting. It is most suitable for superimpose input.
6	Clamp Switch	Yin3	In case of L level, the sink chip clamp, Yin1, Yin2 on operation. In case of H level, Yin1, Yin2 become the clamp voltage compulsory. If the key clamp function is not used, apply it with the L level on fixed condition.
7	Y Line Input Pin 2	Yin2	Video signal input pin (Y line) Key clamp circuit internalized. The clamp function goes on when the key clamp is on H timing. Keyed clamp at L position indicates the normal sink chip clamp on operation. The clamp voltage is about 4.1V.
8	SW3	SW3	Video switch channel change over input. The L level is identified to be input when being left on open state.
9	Y Line Input Pin 4	Yin4	Video signal input pin (Y line) The IC does not have bias or clamp function circuit in it, and its easy to have the external circuit of the brightness level setting. It is most suitable for superimpose input.
10	Y Line Gain Control	GAIN Y	Y Line voltage gain can be adjusted when input of 2.0~3.0V. 2.0V input, at gain min. (-3.0dB) 3.0V input at gain max. (+3.0dB) In order to set the gain within the IC, the gain control circuit compares the voltage (Typ 2.5V), the one which was decided by the resistance the voltage (Typ 2.5V), the one which was decided by the resistance division, and the gain control pin voltage, and then it is advisable to apply voltage on the gain control pin after the process of the resistance division of the supply voltage.
11	Y Line Output Pin	Yout	Its the Y line video signal output pin. It can drive 75Ω line when connecting 25C945 & 25C1815 directly. No sag output can be performed by applying Y line sag correction at 12 pin.
12	Y Line Sag Correcting Pin	Y SAGU	In case when applying as 75Ω driver by connecting 25C945 to Yout, the sag can be generated by output coupling capacitance and load resistance. The output included the sag, when once again, being input at sag correctinn pin through coupling capacitance, and it can be done to take out the output from Y out in which that there is no sag at all. In case when the sag correction function is not required on operation, it is advisable to use it by connecting 11 pin directly.



■ TERMINAL FUNCTION

PIN	PIN NAME	SYMBOL	FUNCTION
13	GND (C Line)	GND C	
14	NC		
15	CLine Output Pin	Cout	It's the C line video signal output pin. It can drive 75Ω line when connecting 2SC945 & 2SC1815 directly.
16	C line Output Pin	GAIN C	C line voltage gain can be adjusted when input 2.0~3.0V. 2.0V input at gain min. (+3.0dB) 3.0V input at gain max. (+9.0dB) In order to set the gain within the IC, the gain control circuit compares the voltage (Typ 2.5V), the one which was decided by the resistance division, and the gain control pin voltage, and then it is advisable to apply voltage on the gain control pin, after the process of resistance division of the supply voltage.
17	C Line Input Pin 3	Cin3	Video signal input pin (C line) The IC does not have bias or clamp function circuit in it, and it's easy to set the brightness level with the external circuit. It is most suitable for superimpose input.
18	SW2	SW2	The L level is identified to be input when being left on open state.
19	C Line Input Pin 2	Cin2	Video signal input pin (C line) The bias voltage is about 4.1V, and the input impedance is about 15KΩ
20	NC		
21	V+ (C Line)	V+ C	C line alone can not be used while the Y line supply voltage is off state.
22	C Line Input Pin 1	Cin1	C line Input Pin 1. Video signal input pin (C line) Bias voltage is about 4.1V, input impedance is about 15KΩ

■ TEST CONDITION

(V_t: 9V, V_c: 5V, TP10, TP21: 2.5V, T_a: 25°C)

PARAMETER	SYMBOL												TEST CONDITION
		1	2	3	4	5	6	7	8	9	0	1	
Supply Current	I _{cc}	L	L	L	L	L	L	L	L	L	L	L	4pin, 21pin Total Current
Y Signal Line													
Input Open Voltage	V _{iy}	L	L	L	L	L	L	L	L	L	L	L	Type1: Measurement TP2: Measurement
Output Open Voltage	V _{oy}	L	L	L	L	L	L	L	L	L	L	L	TP5: Measurement
Output Offset Voltage 1	V _{ofy}	L	L	L	L	L	L	L	L	L	L	L	TP1, 2, 3: 5V TP5: Measurement→V1 V2→ V3→ V _{ofy} =V2-V1 V _{ofy} =V--V2 V _{ofy} =V3-V2 } Judgment
Output offset Voltage 2	V _{ofy}	L	L	L	L	L	L	L	L	L	L	L	tp1, 4: 5v tp5: MeasurementV1→ V4→ V _{ofy} =V4-V1 Judgment
Clamp Sink Current	I _i	L	L	H	L	L	L	L	L	L	L	L	③ pin Sink Current ① pin Sink Current
Voltage Gain Width	G _{vy1}	L	L	L	L	H	L	L	L	L	L	L	At left four switch conditions Tp10: 2.5V voltage gain→Gv1 TP10: 2.0V voltage gain→Gv2 TP10: 3.0V voltage gain→Gv3 G _{vy} =Gv2-Gv1 G _{vy} =Gv3-Gv1 } Judgment
Frequency Gain	G _{fy}	L	L	L	L	H	L	L	L	L	L	L	At left four switch Y _{in} 1MHz voltage gain→Gv4 Y _{in} 10MHz voltage gain→Gv5 G _{fy} =gV5-Gv4 Judgment
Sag Gain	G _{ys}	L	L	L	L	L	L	L	L	L	L	L	SW13: OFF TP16: 100kHz, 50mV _{P-P} input Y _{OUT} :Measure- ment Y _{OUT} /50mV _{P-P} Judgment
Differential Gain	DG	L	L	L	L	H	L	L	L	L	L	L	Y _{out} : 2.0V _{P-P} Standard Staircase Signal Judgment at left four switch conditions
Differential Phase	DP	L	L	L	L	H	L	L	L	L	L	L	Y _{OUT} : 2.0V _{P-P} Standard Staircase Signal Judgment at left four switch conditions



■ TEST CONDITION

(V_I: 9V, V_C: 5V, TP10, TP21: 2.5V, T_a: 25°C)

PARAMETER	SYMBOL	TEST CONDITION											
		1	2	3	4	5	6	7	8	9	0	1	
Crosstalk	CTy	H	L	L	L	H	L	L	L	L	L	L	Judgment by left 12 switch conditions Y _{IN} : 4.43MHz, 2.0V _{P-P} CW wave input Y _{OUT} Measurement Y _{out} /y _{IN} Judgment
		L	H	L	L	H	L	L	L	L	L	L	
		L	H	L	L	H	L	L	L	L	L	L	
		L	L	L	L	H	L	L	L	L	L	L	
		H	L	L	L	H	L	L	L	L	L	L	
		L	L	H	L	L	H	L	L	L	L	L	
		L	L	L	L	L	L	H	L	L	L	L	
		H	L	L	L	L	L	H	L	L	L	L	
		L	L	H	L	L	L	H	L	L	L	L	
		L	L	L	L	L	L	L	H	L	L	L	
		H	L	L	L	L	L	L	H	L	L	L	
		L	H	L	L	L	L	H	L	L	L	L	
Output Impedance	Roy	L	L	L	L	H	L	L	L	L	L	L	
C Signal Line													
Input Open Voltage	Vic	L	L	L	L	L	L	L	L	L	L	L	TP6: Measurement TP7: Measurement
		H	L	L	L	L	L	L	L	L	L	L	
Output Open Voltage	Voc	L	L	L	L	L	L	L	L	L	L	L	TP9: Measurement
Output Offset Voltage	Vofc	L	L	L	L	L	L	L	L	L	L	L	TP6, 7, 8: 5.0V, TP9: Measurement→V1 →V2 →V3 Vofc=V2-V1 Vofc=V3-V1
		H	L	L	L	L	L	L	L	L	L	L	
		L	H	L	L	L	L	L	L	L	L	L	
Voltage Gain	Gvl	L	L	L	L	L	L	L	L	H	L	L	G _{IN} : 1MHz wave, C _{OUT} : 2.0V _{P-P} Judgment by left three conditions
		H	L	L	L	L	L	L	L	L	H	L	
		L	H	L	L	L	L	L	L	L	L	H	
Voltage Gain Variable Width	Gvc	L	L	L	L	L	L	L	L	H	L	L	TP21: 2.5V voltage gain→Vv1 TP21: 2.0V voltage gain TP21: 2.0V voltage gain At left three switch conditions Gvc=Gv2-Gv1 } Judgment Gvc=Gv3-Gv1 }
		H	L	L	L	L	L	L	L	L	H	L	
		L	H	L	L	L	L	L	L	L	L	H	
Frequency Gain	Gfc	L	L	L	L	L	L	L	L	H	L	L	At left three switch conditions G _{IN} : 1MHz voltage gain→Gv4 G _{IN} 8MHz voltage gain→Gv5 Gfc=Gv5-Gv4 Judgment
		H	L	L	L	L	L	L	L	L	H	L	
		L	H	L	L	L	L	L	L	L	L	H	
Crosstalk	CTc	H	L	L	L	L	L	L	L	H	L	L	C _{IN} : 4.43MHz, 1.0V _{P-P} CW wave input C _{OUT} : Measurement
		L	H	L	L	L	L	L	L	H	L	L	
		L	L	L	L	L	L	L	L	L	H	L	
		L	H	L	L	L	L	L	L	L	H	L	
		L	L	L	L	L	L	L	L	L	L	H	
		H	L	L	L	L	L	L	L	L	H	L	
Input Impedance	Ric	L	L	L	L	L	L	L	L	H	L	L	TP19: 3.0V applied voltage, TP6: voltage measurement TP19: 5.0V applied voltage, TP6: voltage measurement Ric=15[kΩ]*(2-V19)/(2-(V2-V1)) Judgment TP22: 3.0V applied voltage, TP7: voltage measurement→V1 TP22: 5.0V applied voltage, TP7: voltage measurement→V2 Ric=15[kΩ]*(V2-V1)/(2-(V-V1)) Judgment
		H	L	L	L	L	L	L	L	L	H	L	
Output Impedance	Roc	L	L	L	L	L	L	L	L	H	L	L	