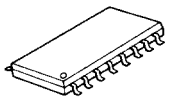
SYNCHRONOUS SEPARATION WITH AFC

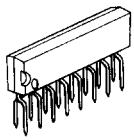
■ GENERAL DESCRIPTION

The NJM2229 has functions of getting the horizontal and vertical synchronous signal from the composit video signal by the synchronous separation circuit. Also the NJM2229 has a detective terminal of the input signal through the synchronous circuit.

■ PACKAGE OUTLINE



NJM2229M



NJM2229S

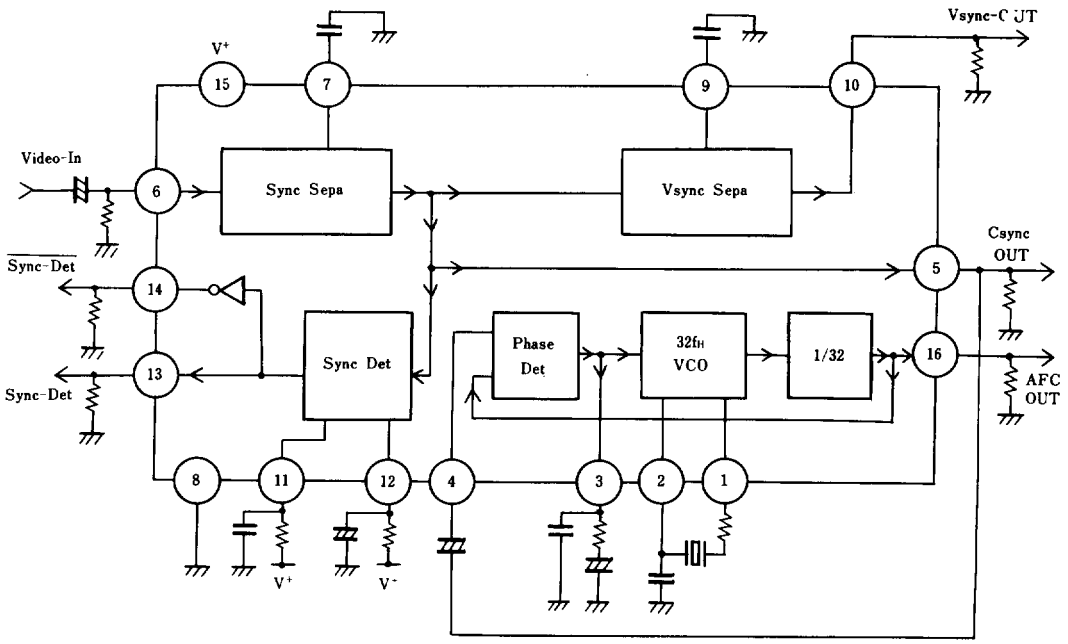
■ FEATURES

- Operating Voltage (+4.7V~+5.3V)
- Internal AFC circuit (Horizontal sync. signal)
- No adjustment of free run frequency.
- Internal detective circuit of sync. signal.
- Package Outline DIP16, ZIP-16
- Bipolar Technology

■ RECOMMENDED OPERATING CONDITION

- Operating Voltage 4.7 ~ 5.3V

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7	V
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	—	20	26	mA
AFC Free-run Frequency	f_{OH}	15.534	15.734	15.934	kHz
AFC Pulse Width	T_{HD}	3.7	3.9	4.1	μs
AFC Delay	T_{HA}	0.7	1.7	2.7	μs
AFC Lock Range	Δf_{HL}	+600 −900	+700 −1000	— —	Hz
AFC Capture Range	Δf_{HP}	+400 −700	+600 −900	— —	Hz
AFC Output Voltage High	V_{HAH}	4.0	4.2	—	V
AFC Output Voltage Low	V_{HAL}	—	0	0.1	V
Sync. Signal Detection Level	V_{HDS}	0.11	0.14	0.17	V
Sync. Signal Detection Delay Time	T_{HDC}	0	0.57	1.5	μs
Sync. Signal Detection Output Voltage High	V_{HDH}	4.0	4.2	—	V
Sync. Signal Detection Output Voltage Low	V_{HDL}	—	0	0.1	V
V_{SYNC} Threshold Voltage High	V_{DSH}	2.4	2.5	2.6	V
V_{SYNC} Threshold Voltage Low	V_{DSL}	1.4	1.5	1.6	V
V_{SYNC} Output Voltage High	V_{DH}	4.0	4.2	—	V
V_{SYNC} Output Voltage Low	V_{DL}	—	0	0.1	V
V_{SYNC} Pulse Width	T_{VD}	212	272	332	μs
V_{SYNC} Delay Time	T_{VDT}	9.6	12.3	15	μs
Sync. Detection Lock Voltage High	V_{LH}	2.53	2.68	2.83	V
Sync. Detection Lock Voltage Low	V_{LL}	1.25	1.40	1.55	V
Sync. Detection Capture High	V_{CH}	2.07	2.22	2.37	V
Sync. Detection Capture Low	V_{CL}	1.57	1.72	1.87	V
Sync. Detection Output Voltage High	V_{DEH}	4.0	4.2	—	V
Sync. Detection Output Voltage Low	V_{DEL}	—	0	0.1	V
Sync. Detection Output Voltage High	$\overline{V_{DEH}}$	4.0	4.2	—	V
Sync. Detection Output Voltage Low	$\overline{V_{DEL}}$	—	0	0.1	V

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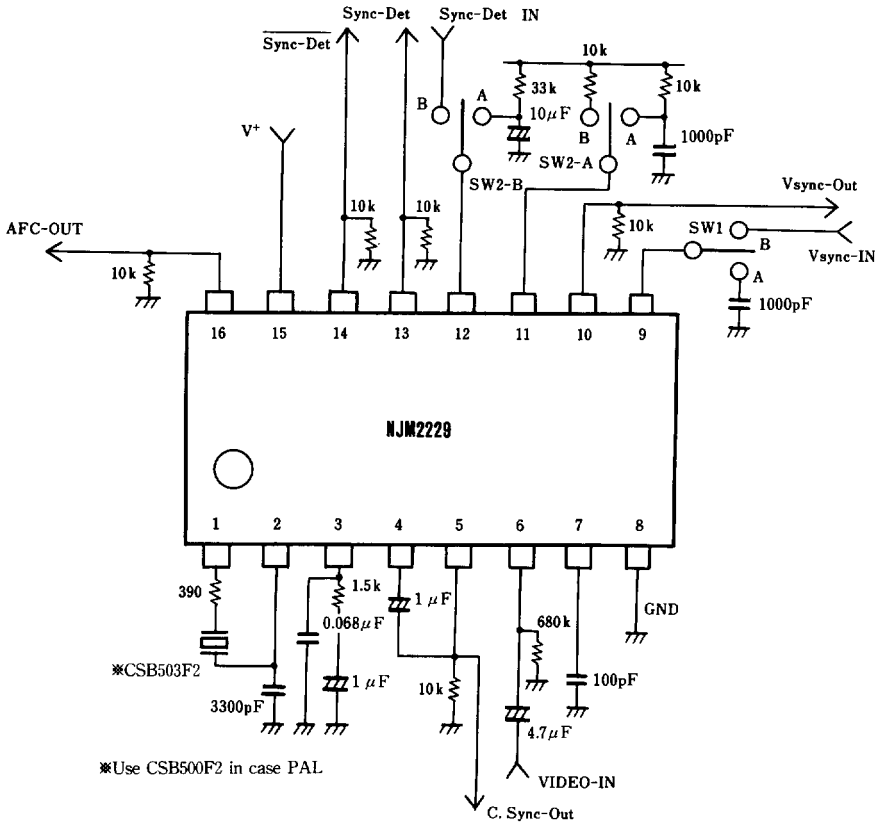
■ TEST CIRCUIT



■ ELECTRICAL PARAMETER TEST METHOD

Test Circuit:

PARAMETERS	SW-1	SW-2	SW-3	TEST CONDITION
Operating Current	A	A	A	No input signal. DC current at Pin15.
AFC Free-run Frequency	A	A	A	No input signal. Video-IN terminal to GND. Frequency at Pin16.
AFC Pulse Width	A	A	A	No input signal. Output Pulse width at pin16. (Note 1)
AFC Output Delay Time	A	A	A	Input $2V_{P-P}$ video signal on Video-IN terminal. Delay time between input and AFC output signal. (Note 1)
AFC Lock Range	A	A	A	Operating ferquency range of AFC output when the input pulse signal frequency with 5 μsec pulse width at Video-IN terminal changes.
AFC Capture Range	A	A	A	Frequency range when signal changes from AFC unlock condition to lock.
AFC Output Voltage	A	A	A	Output voltage at Pin16 in condition of load resistance R_L= 10kΩ.
Sync. Signal Detection Level	A	A	A	Putting $2V_{P-P}$ video signal on Video-IN terminal and reducing it to the level that pin5 output waveform is beginning to change. V_{HDS} is the sink-chip level at that point. (Note 2)
Sync. Signal Detection Output Voltage	A	A	A	Output voltage at Pin5 with load resistance R_L=10kΩ.
Sync. Signal Detection Delay Time	A	A	A	$2V_{P-P}$ video signal at Video-IN terminal. Time difference between input(Pin5) and output(Pin6) waveform.
V_{SYNC} Threshold Voltage High	B	A	A	Gradually increase DC voltage from 2V to 3V at V_{SYNC}-IN terminal. DC input voltage when output voltage at Pin10 changes from LOW to HIGH state.
V_{SYNC} Threshold Voltage Low	B	A	A	Gradually decrease DC voltage from 3V to 1V at V_{SYNC}-IN terminal. DC input voltage when output voltage at Pin10 changes from HIGH to LOW state.
V_{SYNC} Output Voltage	B	A	A	Output voltage at Pin10 with load resistance R_L=10kΩ.
V_{SYNC} Pulse Width	A	A	A	Putting $2V_{P-P}$ video signal on Video-IN terminal and measurring output pulse width at Pin10. (Note 3)
V_{SYNC} Delay Time	A	A	A	Putting $2V_{P-P}$ video signal on Video-IN terminal. Delay time between output at Pin10 and V_{SYNC} at Pin6. (Note 3)
Sync. Detection Lock Voltage High	A	B	B	Increase DC voltage from 2V to 4V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from HIGH to LOW. (Note 4)
Sync. Detection Lock Voltage Low	A	B	B	Decrease DC voltage from 2V to 1V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from HIGH to LOW. (Note 4)
Sync. Detection Capture High	A	B	B	Decrease DC voltage from 3V to 1V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from LOW to HIGH. (Note 4)
Sync. Detection Capture Low	A	B	B	Increase DC voltage from 1V to 2V put on Sync-Det-IN terminal and measure its DC voltage when output voltage at Pin13 changes from LOW to HIGH. (Note 4)
Sync. Detection Output Voltage	A	B	B	Output voltage at Pin13 with load resistance R_L=10kΩ.
$\overline{\text{Sync. Detection Output Voltage}}$	A	B	B	Output voltage at $\overline{\text{Pin14}}$ with load resistance R_L=10kΩ.

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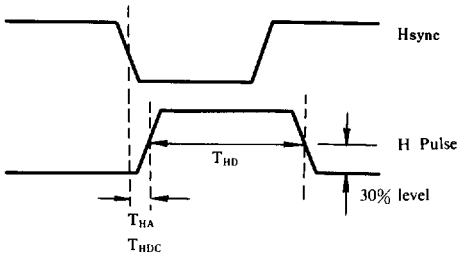
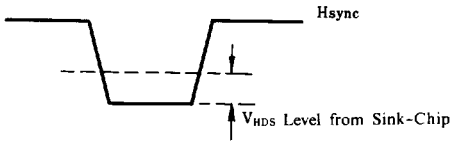
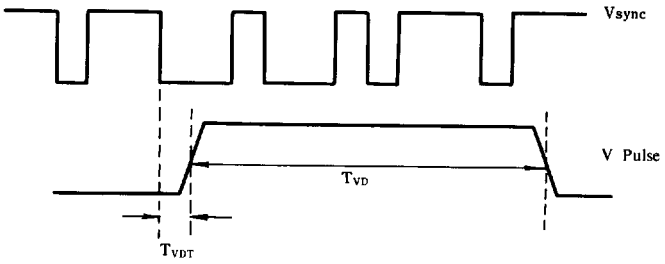
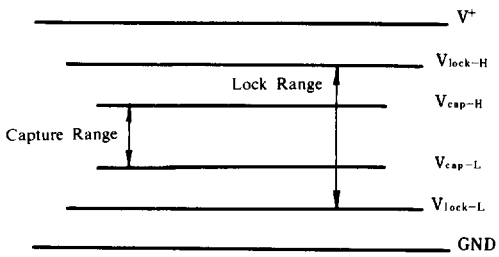
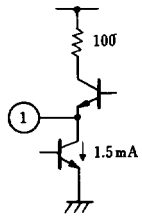
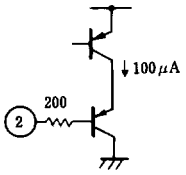
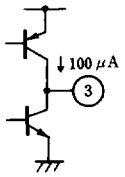
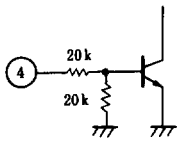
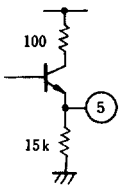

Hsync
H Pulse
30% level
T_{HD}
T_{HA}
T_{HDC}


Hsync
V_{HDS} Level from Sink-Chip


Vsync
V Pulse
T_{VD}
T_{VDT}


V^+
V_{lock-H}
Lock Range
V_{cap-H}
Capture Range
V_{cap-L}
V_{lock-L}
GND

■ PIN FUNCTION

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	VCO-OUT	Putting VCO output on ceramic resonator.	
2	VCO-FILTER	Deciding phase of ceramic resonator.	
3	AFC-FILTER	Low pass filter of AFC.	
4	AFC-IN	Input terminal of AFC. Putting composite. synchronous signal on it.	
5	C. SYNC-OUT	Sync. signal Detection output	

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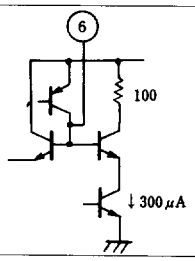
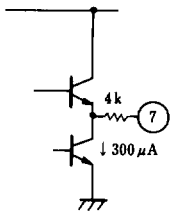
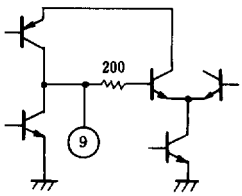
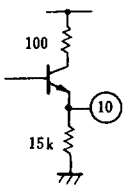
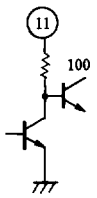
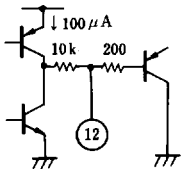
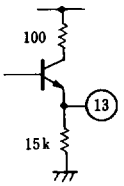
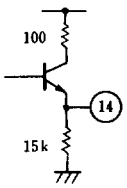
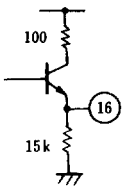
PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
6	VIDEO-IN	Input composite video signal.	
7	L. P. F	Low pass filter for chroma signal.	
8	GND	Ground.	
9	SYNC-INTEGR	Integrating composite synchronous signal and putting vertical synchronous reproducing circuit.	
10	VSYNC-OUT	Vertical synchronous output.	

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
11	M. M-TC	Deciding time constant of M. M. V. (monomulti vibrator)	
12	M. M-INTER	Smoothing M. M. V. output.	
13	SYNCDET-OUT	Signal detective output.	
14	$\overline{\text{SYNCDET-OUT}}$	Inversed output of Pin 13.	
15	V^+	Power supply.	
16	AFC-OUT	AFC output.	

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