



SYSTEM RESET IC

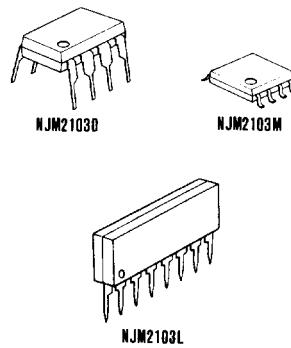
■ GENERAL DESCRIPTION

NJM2103 is supply voltage supervisory IC to detect the abnormal conditions, such as shut down of all supply voltages at once, or sudden voltage down and then generate the reset signal. It supervises both 5V supply voltage and the voltage optionally set up.

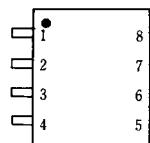
■ FEATURES

- Precise Detection of Supply Voltage Down ($V_{SA}=4.2V \pm 2.5\%$)
- Possible Detection of Optional Voltage Down ($V_{SB}=1.22V \pm 1.5\%$)
- Possible Detection of Optional Over-loading
- Low Operating Current ($I_{CC} \leq 500 \mu A @ V_{SB}=5V$)
- Reference Voltage can be taken out.
- Low Reset Validated Voltage ($V^+=0.8V$ Typ.)
- Voltage Detection with Hysteresis Feature
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

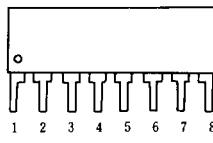
■ PACKAGE OUTLINE



■ PIN CONFIGURATION



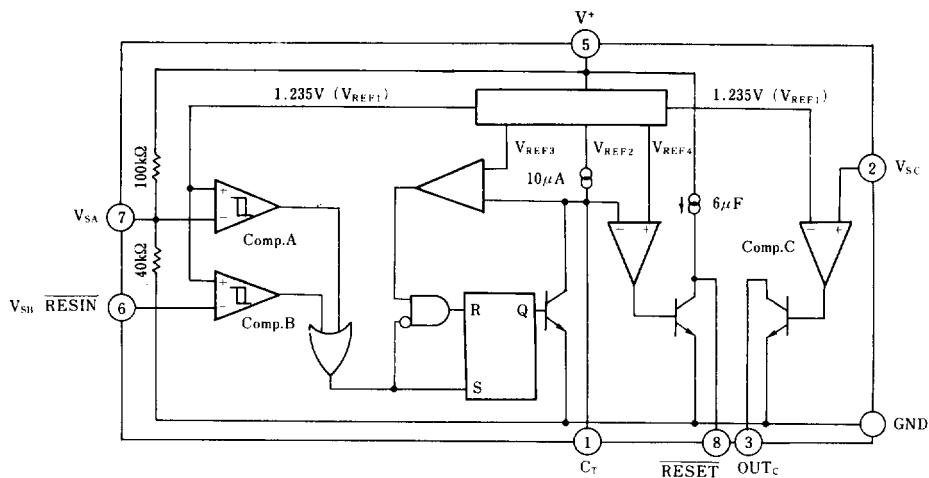
NJM2103D
NJM2103M



NJM2103L

| PIN FUNCTION | |
|--------------|----------------|
| 1. | C_T |
| 2. | V_{SC} |
| 3. | OUT_c |
| 4. | GND |
| 5. | V^+ |
| 6. | $V_{SB}/RESET$ |
| 7. | V_{SA} |
| 8. | RESET |

■ BLOCK DIAGRAM




■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-----------------------------|------------------|---------------------------------------|------|
| Supply Voltage | V ⁺ | 20 | V |
| Power Dissipation | P _D | (DIP8) 500 (DM8) 300 (SIP8) 800 | mW |
| Input Voltage A | V _{SA} | V ⁺ +0.3(<20) | V |
| Input Voltage B | V _{SB} | 20 | V |
| Input Voltage C | V _{SC} | 20 | V |
| Operating Temperature Range | T _{opr} | -20 ~ +75 | °C |
| Storage Temperature Range | T _{stg} | -40 ~ +125 | °C |

■ ELECTRICAL CHARACTERISTICS
• DC CHARACTERISTICS
(V⁺=5.0V, V_{SB}=0V, V_{SC}=0V, Ta=25°C)

| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------------|--|-------|-------|-------|-------|
| Operating Current (1) | I _{CC1} | V _{SB} =5V | — | 380 | 560 | μA |
| Operating Current (2) | I _{CC2} | — | — | 460 | 700 | μA |
| V _{SA} Detecting Voltage (1) | V _{SAL} | V ⁺ fall time V _{SB} =V ⁺ | 4.10 | 4.20 | 4.30 | V |
| V _{SA} Detecting Voltage (2) | V _{SAH} | V ⁺ rise time V _{SB} =V ⁺ | 4.20 | 4.30 | 4.40 | V |
| V _{SA} Hysteresis Width | V _{HRSA} | — | 50 | 100 | 150 | mV |
| V _{SB} Detecting Voltage | V _{SB1} | V _{SB} fall time | — | 1.202 | 1.220 | 1.238 |
| V _{SB} Detecting Supply Voltage Fluctuation | ΔV _{SB1} | V ⁺ =3.5~18V | — | 3 | 10 | mV |
| V _{SB} Hysteresis Width | V _{HRSB} | — | 14 | 28 | 42 | mV |
| V _{SB} Input Current (1) | I _{IHB} | V _{SB} =5V | — | 0 | 250 | nA |
| V _{SB} Input Current (2) | I _{ILB} | — | — | 20 | 250 | nA |
| High Level RESET Output Voltage | V _{OHR} | I _{RESET} =-5μA, V _{SB} =5V | 4.5 | 4.9 | — | μV |
| RESET Output Saturating Voltage(1) | V _{OLRI} | I _{RESET} =2mA | — | 0.20 | 0.40 | V |
| RESET Output Saturating Voltage(2) | V _{OLR2} | I _{RESET} =10mA | — | 0.30 | 0.50 | V |
| RESET Output Sink Current | I _{RESET} | V _{OLR} =1.0V | 20 | 80 | — | mA |
| C _T Charge Current | I _{CT} | V _{SB} =5V, V _{CT} =0.5V | 6.0 | 9.5 | 13.0 | μA |
| V _{SC} Input Current (1) | I _{IHC} | V _{SC} =5V | — | 0 | 500 | nA |
| V _{SC} Input Current (2) | I _{ILC} | — | — | 50 | 500 | nA |
| V _{SC} Detecting Voltage | V _{SC} | — | 1.215 | 1.235 | 1.255 | V |
| V _{SC} Detecting Supply Voltage Fluctuation | ΔV _{SC} | V ⁺ =3.5~13.5V | — | 3 | 10 | mV |
| OUT _C Output Leak Current | I _{ODC} | V _{OHC} =13.5V | — | 0 | 1 | μA |
| OUT _C Output Saturation Voltage | V _{OLC} | I _{OUT} =4mA, V _{SC} =5V | — | 0.10 | 0.40 | V |
| OUT _C Output Sink Current | I _{OUTC} | V _{OLC} =1.0V, V _{SC} =5V | 6 | 20 | — | mA |
| RESET Guarantee Minimum Supply Voltage | V ⁺ _L | V _{OLR} =0.4V, I _{RESET} =200μA | — | 0.8 | 1.2 | V |

7

• AC CHARACTERISTICS
(V⁺=5.0V, V_{SB}=5.0V, V_{SC}=0V, CT=0.01 μF, Ta=25°C)

| ITEM | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------------------------------|------------------|--|------|------|------|------|
| V _{SA} Input Pulse Width | t _{PIA} | — | — | 3.0 | — | μs |
| V _{SB} Input Pulse Width | t _{PIB} | — | — | 1.5 | — | μs |
| RESET Output Pulse Width | t _{PO} | V _{SB} =V ⁺ | — | 1.5 | — | ms |
| RESET Rise Time | t _r | V _{SB} =V ⁺ , R _L =2.2kΩ, C _L =100pF | — | 1.0 | — | μs |
| RESET Fall Time | t _f | V _{SB} =V ⁺ , R _L =2.2kΩ, C _L =100pF | — | 0.1 | — | μs |
| Output Delay Time | t _{PD} | V _{SB} fall time | — | 2 | — | μs |
| Output Delay Time | t _{PHL} | V _{SC} rise time, R _L =2.2kΩ, C _L =100pF | — | 0.5 | — | μs |
| Output Delay Time | t _{PLH} | V _{SC} fall time, R _L =2.2kΩ, C _L =100pF | — | 1.0 | — | μs |



NJM2103

■ TERMINAL FUNCTION

| PIN NO. | SYMBOL | FUNCTION | INSIDE EQUIVALENT CIRCUIT |
|---------|------------------|---|---------------------------|
| 1 | C _T | Pin Connection to Capacitor, Set the reset holding time. | |
| 2 | V _{SC} | Comparator Input | |
| 3 | OUT _C | Open Collector Output of Comparator C. | |

■ TERMINAL FUNCTION

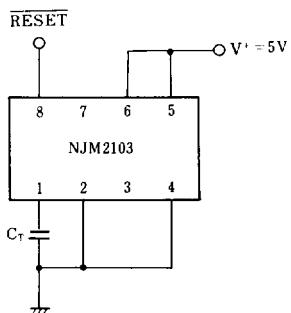
| PIN NO. | SYMBOL | FUNCTION | INSIDE EQUIVALENT CIRCUIT |
|---------|------------------------------------|--|---|
| 4 | GND | Ground | |
| 5 | V ⁺ | Operating Voltage | |
| 6 | V _{SB} /R _{ESIN} | Comparator B Input | <p>The circuit diagram for Pin 6 shows a differential input stage. It consists of two NPN transistors connected in an anti-series configuration. The base of the top transistor is connected to the input terminal (Pin 6) through a resistor. The collector of the top transistor is connected to the collector of the bottom transistor. The base of the bottom transistor is connected to ground (GND) through a resistor. The collector of the bottom transistor is connected to the output terminal (V_{REF}) through a resistor. The output terminal (V_{REF}) is also connected to ground (GND).</p> |
| 7 | V _{SA} | Comparator A Input | <p>The circuit diagram for Pin 7 shows a differential input stage. It consists of two NPN transistors connected in an anti-series configuration. The base of the top transistor is connected to the input terminal (Pin 7) through a resistor. The collector of the top transistor is connected to the collector of the bottom transistor. The base of the bottom transistor is connected to ground (GND) through a resistor. The collector of the bottom transistor is connected to the output terminal (V₊) through a resistor. The output terminal (V₊) is also connected to ground (GND).</p> |
| 8 | RESET | Reset Output Internalizing pull up resistor | <p>The circuit diagram for Pin 8 shows a reset output stage. It consists of two NPN transistors. The base of the top transistor is connected to the input terminal (Pin 8) through a resistor. The collector of the top transistor is connected to the collector of the bottom transistor. The base of the bottom transistor is connected to ground (GND) through a resistor. The collector of the bottom transistor is connected to the output terminal (V⁺) through a resistor. The output terminal (V⁺) is also connected to ground (GND).</p> |



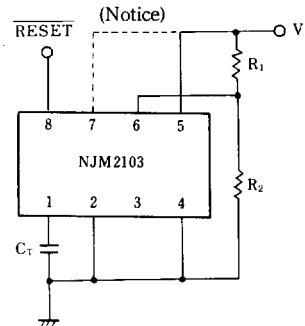
NJM2103

■ APPLICATION CIRCUIT

1) 5V Supply Voltage Monitor



2) Monitoring of Optional Supply Voltage (V⁺ ≤ 13.5V)

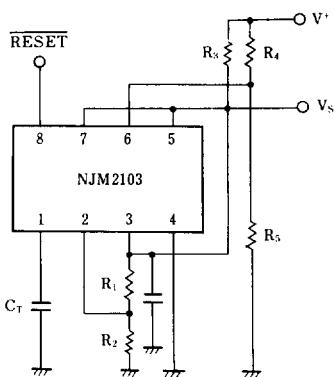


$$\text{Detecting Voltage} \doteq (1 + \frac{R_1}{R_2}) \times V_{SB}$$

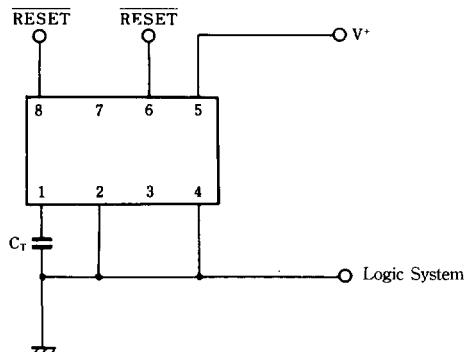
(Notice)

If it were that V⁺ indicates under 4.50V, Connect 7 pin to V⁺

3) Monitoring of Optional Supply Voltage (V⁺ > 13.5V)



4) Compulsory Reset

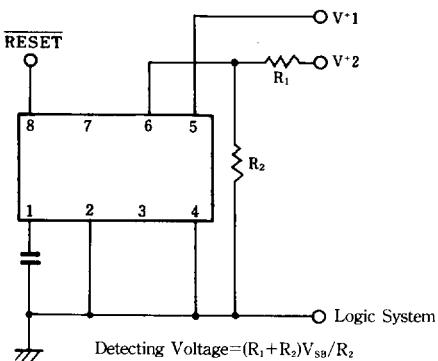


$$\text{Detecting Voltage} \doteq (1 + \frac{R_4}{R_5}) \times V_{SB}$$

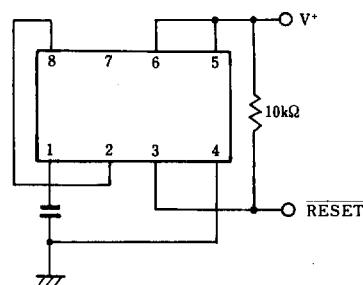
$$\text{Constant Voltage Output } V_S \doteq (1 + \frac{R_1}{R_2}) \times V_{SC}$$

$$\overline{\text{RESET}} \text{ Output} \doteq \begin{cases} V_S & (\text{High Level}) \\ OV & (\text{Low Level}) \end{cases}$$

Input Reset signal TTL level to V_{SB}-terminal

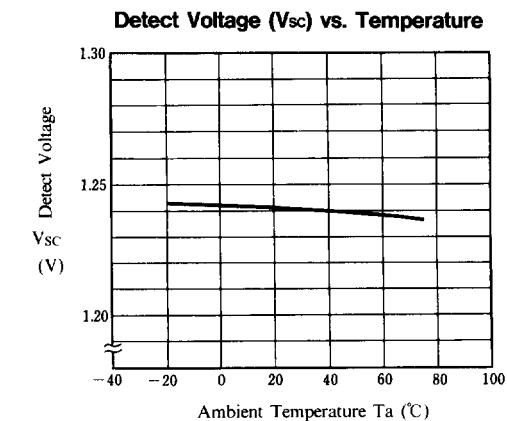
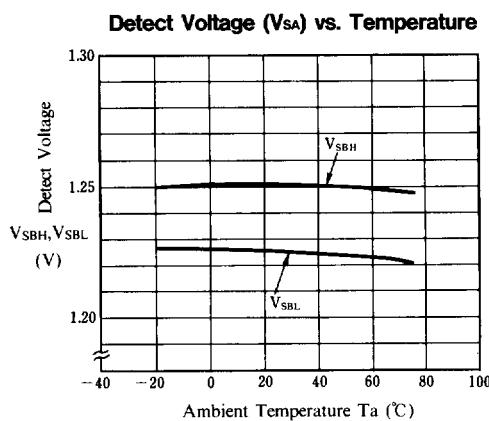
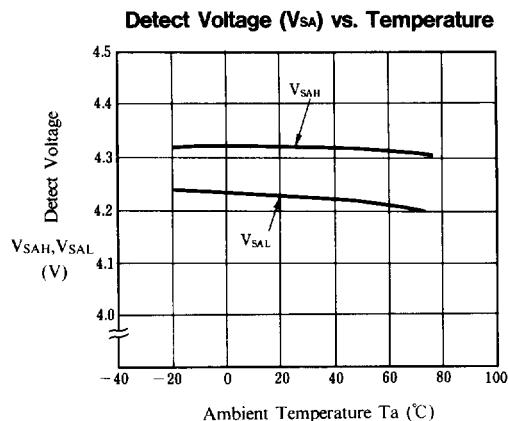
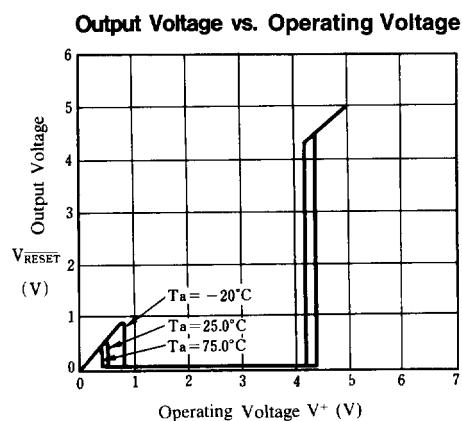
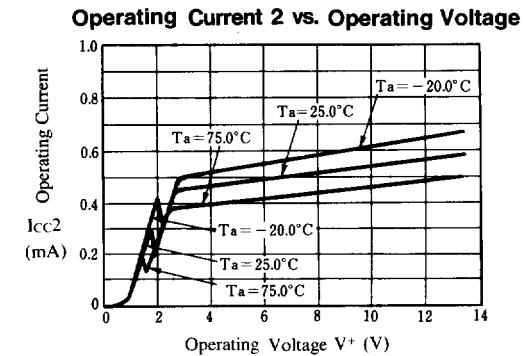
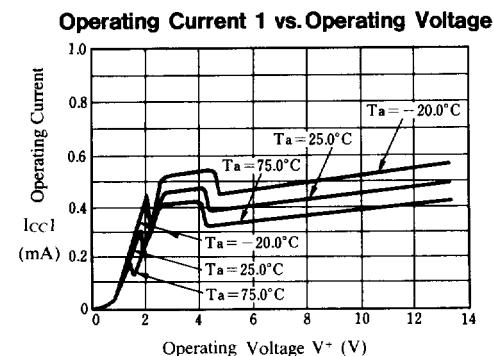
5) 5V,V_{CC}<12V Supply Voltage Monitor

6) Non-Inverting Reset





■ TYPICAL CHARACTERISTICS



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