A Systematic Approach for Testing Today's Power Semiconductors to Obtain a Generally Applicable Characterization

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Abstract: New characterization and testing methods have been developed with respect to the state of the art in power semiconductors. Their knowledge and use is decisive for reliable and efficient simulation and design of power electronic converters. This paper shows principles of characterization in a systematic approach. Their meaning for component applications is derived. Furtherly testing methods to gain the required data are derived. Testers recently developed for characterization and quality assurance measurements and results obtained with them are presented. Thus this paper shows the links between characterization, testing and application for fast switching power semiconductors. It focusses on insulated gate bipolar transistors (IGBT) as typical devices of this type.

Keywords: characterization, simulation, calculation, test, tester, IGBT

1 Characterization Principles

International standards and drafts as [1] define most of the parameters to be specified for power semiconductors — in this case IGBTs — and setups for measuring them. Table 1 gives a short summary. Data are sorted and commented according to the aim to provide a systematic approach with respect to applications and testing. Section 2 derives the use of these data usually given by the supplier of the power semiconductors for any application. Section 3.1 distinguishes the information of table 1 with respect to the different types of tests, section 3.2 with respect to the different types of components and their state in manufacturing process. Thus these sections provide the base for section 3.3: Several new concepts of testers and results obtained with them are presented there.

2 Meaning of Characterization Principles for Application

2.1 General

In the design phase of a converter usually calculations as in Buri [2] or Kolar et al [3], and simulations as in Ferrieux et al [4] or Scheible [5] are executed. They are based on topology, control method and operating conditions of the specific converter determining power semiconductors' stress and on semiconductor data as listed in table 1. These data usually consist of minimum and maximum values defining limits, and of typical values providing additional information.
The safe operating area for regular operation is usually limited by parameters as breakdown voltage or maximum junction temperature due to power losses according to

$$T_{Jmax} \geq T_J = R_{thJA} \cdot \sum_i P_{Vi} + T_A \qquad (1)$$

with P_{Vi} being the conducting, blocking, turn on and turn off losses respectively; they will be furtherly considered in the following sections. The calculation in equation 1 with the steady state value R_{thJA} may be replaced by taking into account a network of thermal capacities C_{thi} and resistances R_{thi}; values or curves for Z_{th} correspond to this.
Depending on the topology of the converter and the version of power semiconductor device used, free wheeling diodes may have to be taken into account additionally.
The equations given in the following defining approximations of characteristics have been verified with testing methods and testers as described later in section 3.3. They are of course not intended to replace more accurate models, however they have shown to be helpful for many calculations with the aim to estimate power semiconductor stress.

2.2 Conducting

Conducting losses in equation 1 are caused by the semiconductor switch having a forward voltage when forward current is flowing.
For bipolar devices as IGBTs often an exponential curve according to diodes' behaviour is given:

$$I_{AK} = I_S \cdot \left(e^{\frac{e \cdot U_{AK}}{k \cdot T}} - 1 \right) \qquad (2)$$

It describes the interference between forward voltage and current. Forward voltage is strongly influenced

Table 1: list of characterization data with respect to application and testing

name	symbol	remarks
constants		
mechanical	M_{mount}	for stability and thermal contact
thermal interface	R_{th}, C_{th}	under specific mounting conditions
max. junction temp.	T_{Jmax}	defined by chip design
functions		
forward voltage	$U_{CEsat}(I_C, U_{GE}, T_J)$	high current, low voltage static test
threshold voltage	$U_{GEth}(I_C, T_J)$	low voltage static test
breakdown voltage	$BU_{CE}(I_C, T_J)$	high voltage, low current static test
leakage current	$I_{CES}(U_{CE}, T_J)$	high voltage, low current static test
turn on/off energy	$E_{on/off}(I_C, U_{CE}, U_{GE}, R_G, T_J, Load)$	high voltage and current switching test
turn on/off times	$t_{don/ri/doff/fi}(I_C, U_{CE}, U_{GE}, R_G, T_J, Load)$	high voltage and current switching test
gate charge/capacity	$Q_G/C_{ies/oes/res}(U_{CE}, U_{GE}, f)$	switching test
sequences		
RBSOA	U_{CE}, I_{CM} at U_{GE}, R_G, T_J	maximum non destructive values
short circuit	U_{CE} at t_{on}, U_{GE}, R_G, T_J	maximum non destructive values
reliability	n: number of cycles	cycling test under various conditions

by saturation characteristic determined by gate voltage. For calculation purposes it is often sufficient to resolve and simplify equation 2 to:

$$U_{AK} = U_{T0} + r_T \cdot I_{AK} \tag{3}$$

Equation 3 can also be applied to MOSFETs with $U_{T0} = 0$.

2.3 Blocking

Blocking currents usually are quite low, however at high blocking voltage a considerable power loss may occur although. In some cases this may lead to thermal runaway as described in Rivet [6]. Blocking characteristics of devices being more complex than diodes cannot necessarily be described by equation 2. However blocking losses do usually not occur as a major contribution to total power losses $\sum_i P_{Vi}$. Anyway blocking voltage must not exceed breakdown voltage of the device.

2.4 Switching

Switching losses can be divided into turn on losses and turn off losses. They are usually specified as an energy value for one switching action under specified conditions. Thus applications with constant switching frequency can be covered according to

$$P_{on} = E_{on} \cdot f_{switch} \quad , \quad P_{off} = E_{off} \cdot f_{switch} \tag{4}$$

and control strategies minimizing switching operations, for example using space vector models, can also be considered.
While the temperature coefficient of switching energies is dependent on semiconductor technology the dependance on voltage and current can be estimated as linear by:

$$E_{on/off,app.} = E_{on/off,spec.} \cdot \frac{U_{CE,app.} \cdot I_{C,app.}}{U_{CE,spec.} \cdot I_{C,spec.}} \tag{5}$$

The approximation in equation 5 however is limited in case the specified values are too different from the actual values in the application. However few problems arise of this fact because the specification is to be done for about nominal operational conditions; only resonant topologies typically differ significantly from these conditions, but by zero voltage or current switching turn on or turn off losses are minimized anyway. In case turn on losses occur the reverse recovery behaviour of free wheeling diode is essential. The information on switching times in table 1 is necessary to determine if the switch is sufficiently fast for the application according to:

$$t_{don} + t_{ri} + t_{doff} + t_{fi} \ll \frac{1}{f_{switch}} \tag{6}$$

Gate charge and capacity values are important for driver design. Finally also during the switching intervals constant limits as breakdown voltage must not be exceeded which is particularly critical in case peaks occur.

2.5 Sequences

Sections 2.2, 2.3 and 2.4 deal with regular operation as mentioned in section 2.1. Besides this regular operation the converter is designed for, irregular operation may occur due to external or internal fault conditions. This usually leads to currents or voltages respectively to be applied to the power semiconductors higher than permitted according to equation 1. This type of operation can partially be considered

by taking into account the thermal behaviour due to R_{thi} and C_{thi} as mentioned in section 2.1. It is however helpful to specify typical sequences for such cases usually consisting of blocking, turning on, conducting, switching off and blocking again. In table 1 reverse bias safe operating area (RBSOA) and short circiut are listed. These data permit to judge what irregluar operation the component is rugged enough for.

Additionally sequences often are applied to characterize reliability. This has become an important subject especially with respect to the use of new types of semiconductors in connection with partially changed mounting methods in traction applications. Jacob et al [7] gives an insight into this subject.

3 Meaning of Characterization Principles for Testing

3.1 Types of Testing

3.1.1 Static Tests. Measurement times are significantly longer than the small time constants of the device under test which means steady state operation is characterized.

These tests usually are executed with either high voltage or high current to be applied to the device. This permits the measurement ranges of test equipment to be optimally matched to the values to be characterized. Energy dissipation during these tests is rather small.

A variety of automated test equipment is available for static testing. The optimization between the contradictuous aims of short test times and high accuracy is an engineering task.

3.1.2 Dynamic Tests. The transient intervals of switching on and off as described in section 2.4 can be characterized by these tests. So the device changes state from high voltage and low current to low voltage and high current or the other way round.

The characterization for irregular operation by sequences as mentioned in section 2.5 also belongs to this group — the respective tests are based on switching between different states, usually with the aim to finally turn the device off safely.

Anyway in most cases of dynamic tests high and low current and voltage occur subsequently which makes accurate measurements difficult: Resolution is determined by the high amplitudes and thus limits accuracy at low values. This is a severe problem determining for example switching energies — the standardized integration intervals are defined by full scale and 2 % voltage or current limits respectively. Furtherly the amount of energy stored in the test equipment is much higher. This would not be a problem executing some non repetitive tests in laboratory. If dynamic tests however are introduced in production as a means of quality control, the protection of operators and equipment must be adapted to the high number of pieces tested. Usually a limitation of energy dissipated in case of a failure of the device under test is required.

3.1.3 Reliability Tests. For the sake of briefness this paper does not furtherly consider reliability tests. Please refer to the references Jacob et al [8], Coquery et al [9], Jacob et al [10] and Neidig [11] for further information. It should however be mentioned that big effort is spent in this area to assure a high level of reliability, matched to and sufficient for any application.

3.2 Devices to be Tested

Testing begins in an early state of component production: Usually first electrical tests are applied to the wafers consisting of a high number of chips. This helps to control semiconductor production process and to appropriately select chips for mounting into packages. Tests on waferprobers or single chips are usually of static type according to section 3.1.1.

In case of discrete components the next state measurements are taken in is already the completely assembled device. The majority of discrete devices contains exactly one unidirectional switch — for example an IGBT. There are however also discrete components being configured as bidirectional switches — for example an IGBT with an antiparallel diode — or as buck or boost circuit — for example an IGBT with a free wheeling diode connected to emitter or collector respectively. Topology determines the way tests are carried out: Static tests according to section 3.1.1 measure the important parameters of IGBT and diode as listed in table 1. Dynamic tests according to section 3.1.2 at least measure characteristics of the controllable switch — for example the IGBT. Inductive switching should be carried out with a free wheeling diode corresponding to the internal diode as mentioned, because the type of free wheeling diode is decisive for switching losses as mentioned in section 2.4.

In module assembly the power semiconductor chips are in a first step soldered to a direct copper bond (DCB) substrate and wire bonded. One or several of these DCB substrates are in a second step assembled in a module package. This offers the opportunity to perform static and dynamic tests on the DCB substrates and on the finally assembled module. Tests are carried out for each bridge in the same way as described above for discrete components consisting of a controllable switch with a free wheeling diode. Some particularities regarding control side have to be taken into account testing intelligent power modules containing driver circuits.

3.3 Testers and Test Results

Two examples of recently developed testers including results obtained with them will be shown in the following. Both testers have been designed for dynamic testing of fast switching devices, however with different approaches:

3.3.1 General Purpose Dynamic Testing.

The schematic of a tester for general purpose dynamic testing can be seen in figure 1: The device under

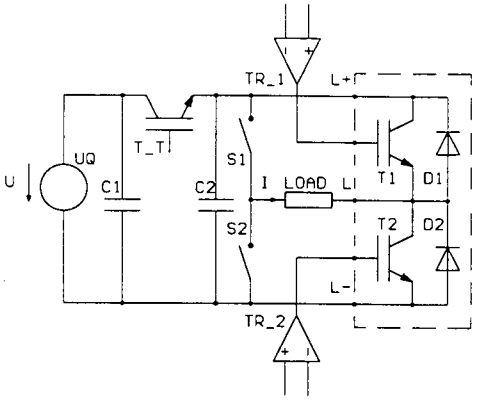

Figure 1: tester for resistive or inductive switching

test on the right — the schematic shows a module in phase leg configuration consisting of T_1, D_1, T_2 and D_2 — is controlled by two gate drivers Tr_1 and Tr_2. It is connected to an intermediate circuit $L+$ and $L-$. The ohmic or inductive load is connected to the latter's positive or negative potential by the switches S_1 or S_2, depending on which transistor or combination of diode and transistor is going to be tested — T_2 with D_1 or T_1 with D_2. The switch T_T seperates most of buffer capacity in intermediate circuit — with $C_1 \gg C_2$ — in case of a failure of the device under test. Control of the tester is computer based. Voltages and currents are monitored during the test sequence; afterwards the waveforms are analyzed by the computer: Characteristic values for the switching tests as listed in table 1 can be calculated. Figures 2 and 3 show waveforms obtained at a test that was executed with the aim to furtherly investigate the influence of diode characteristics on switching behaviour of a phaseleg consisting of an IGBT T_1 and a diode D_2 — see figure 1. For this purpose besides the IGBT's gate voltage U_{GE} and collector current I_C providing information about the IGBT's state, diode reverse voltage U_{KA} and diode current I_{AK} have been monitored. Figure 2 shows the succession of the intervals of the assymetrical double pulse test as programmed: IGBT on/diode off — IGBT off/diode on — IGBT on/diode off — IGBT off/diode on. Figure 3 shows the turn off of the IGBT and turn on of the diode with a high time resolution. It can be clearly seen diode voltage de-

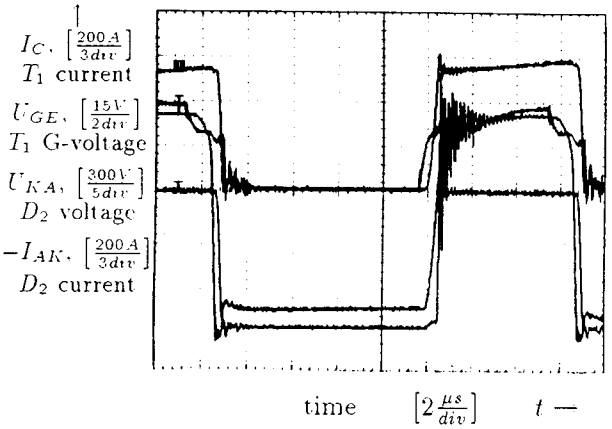

Figure 2: inductive switching waveforms of a phaseleg

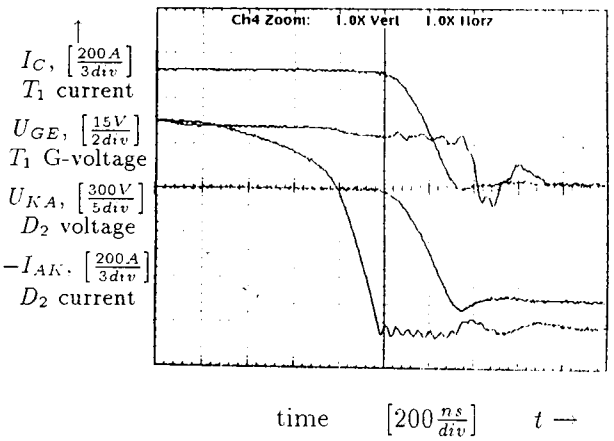

Figure 3: IGBT turn off and diode turn on interval waveforms of a phaseleg's inductive switching

cays from $U_{KA} \approx 300V$ towards $U_{KA} - 0$. Having reached it, diode current begins to rise from $I_{AK} = 0$ to $I_{AK} \approx 170A$; during this time there is a small forward voltage overshoot — forward recovery voltage U_{FR}. Accurate characterization data for this operational point including the conditions as current rise rate $\frac{di_{AK}}{dt}$ are gained by executing programmable waveform analysis.

This tester offers the opportunity to program a variety of test sequences and conditions and to do a detailed analysis. The programmer however must be aware of the high complexity of the system which requires a high amount of time and experience to create test plans.

The operational behaviour of a tester according to figure 1 may become unsatisfactory in case of test sequences to assure maximum non destructive values according to table 1. Due to the tester's complex hardware and control it is sensitive to disturbances, for example oscillations, that may occur at potentially destructive tests. Section 3.3.2 deals with another type of tester developed at IXYS for this kind

of tests:

3.3.2 Short Circiut Testing. A very rugged short circuit tester according to figure 4 has been created. Its control renounces on a feedback. Any disturbance of the measurement by a series switch as T_T in figure 1 and the possible failure of this switch are avoided by simply limiting the energy stored in the capacitors C_1 or C_2 the device under test T_1 or T_2 respectively is connected to:

$$W = \frac{1}{2} \cdot C \cdot U^2 \quad \text{with} \quad C = \frac{I_{max} \cdot T_{short,max}}{\Delta U_{max}} \quad (7)$$

C is the capacity, I_{max} the maximum short circuit current to be expected for passing devices, $T_{short,max}$ the maximum short circuit time used and ΔU_{max} the maximum permitted voltage decay during short circuit time. The mechanical layout of power section with copper plates provides low inductance; thus the test conditions highly correspond to the ones in a converter the power semiconductor device is designed to operate in.

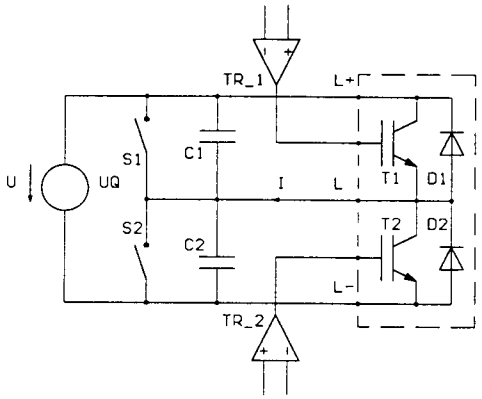

Figure 4: tester for short circuit test

Figure 5 shows collector current I_C of T_1 during short circuit test of an IGBT module according to figure 4. While nominal current of the module is $I_{C,N} = 150\ A$, peak short circuit current is measured to be $\hat{I}_{C,SC} \approx 1100\ A$. Due to desaturation collector emitter voltage is applied in the same time short circuit current flows, which leads to a very high power dissipation heating the chips. Temperature rise is the main reason for the decay of short circuit current during the test. The device the test is shown of in figure 5 has passed — it turns off safely after the specified time according to table 1 which is $t_{on} = 10\mu s$ here corresponding to industry standard for short circuit proof IGBTs.
Figure 6 shows a device failing short circuit test as it may happen in the whole time interval between turn on and turn off, however with increasing probability towards the latter. Please note although the tester's short circuit energy is limited according to

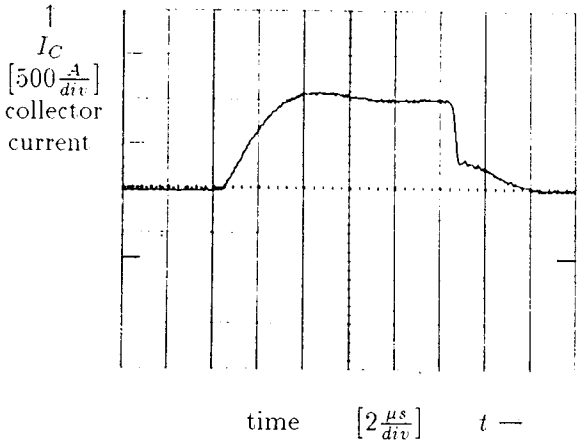

Figure 5: device under test passing short circuit test

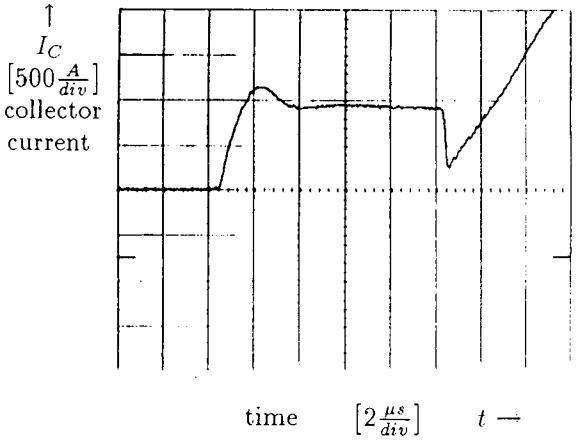

Figure 6: device under test failing short circuit test

equation 7, short circuit current is almost illimited in the interesting current range below $I_{C,SC} \leq 2kA$ as can be seen by the rise of collector current after the failure during turn off. Although short circuit test is a high current, voltage and power test, no oscillations that may additionally stress the sensitive device under test, occur. Depending on the failure mechanism much higher rise rates of collector current $\frac{di_{C,SC}}{dt}$ than shown have been observed, proving the low inductance of the tester's topology.
The short circuit tester thus generates the test conditions as needed to verify IGBTs' short circuit capability. It has proven to be rugged itself. Both has been achieved with — or due to — a design being as simple as possible.

4 Conclusion

An approach for characterization of fast switching power semiconductors and power semiconductor devices containing several types of switches has been presented.
The use of characterization data for calculation and

simulation of converters has been derived. Several interferences have been pointed out and equations were given. Their use permits to gain application specific parameters from general characterization. Furtherly different methods of testing have been derived. Their use has been explained. Testers recently developed to implement the testing methods have been presented. Advantages and restrictions of different tester concepts have been pointed out, leading to a selective choice of tester type depending on the measurements to be taken. Test results obtained with several testers have shown their operational principles and behaviour.
Thus the paper shows the subject of testing being linked via universal characterization with the subject of calculation and simulation of converters.

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