Design and Experimental Investigation of a Three-Phase High Power Density High Efficiency Unity Power Factor PWM (VIENNA) Rectifier Employing a Novel Integrated Power Semiconductor Module

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ABSTRACT

The topic of this paper is the development of guidelines for the practical application of a new power module (IXYS VUM25-E) realizing a bridge leg of a three-phase/switch/level PWM (VIENNA) rectifier system with low effects on the mains. The inner circuit structure of the power module is formed by a bidirectional bipolar switch (realized by a power MOSFET connected across the DC terminals of a diode bridge) and of two free-wheeling diodes. In a first step the switching losses of the power MOSFET and of the free-wheeling diodes are determined by measurement in dependency on the switched current for characteristic values of the junction temperature. For connecting the module to the passive components of the power circuit of the single-phase test arrangement an appropriate designed power print minimizing the parasitic lead inductances is applied. Furthermore, the isolated driving stage of the MOSFET is designed for minimum switching losses considering the occurring switching overvoltages and the ringing between the parasitic circuit elements. The conduction losses of the semiconductor elements are calculated directly via simple analytical approximations of the mean and rms values (related to a mains period) of the device currents. Based on the knowledge of the dependency of the main loss contributions of the semiconductors of the power module on the operating parameters (mains voltage, output voltage, heat sink temperature and switching frequency) the thermally maximum allowable mains current amplitude is calculated. Furthermore, for different switching frequencies an overview over the power loss contributions of the semiconductor elements is given. Also, the reduction of the efficiency caused by the total semiconductor losses is determined. Finally, the overall efficiency of a PWM (VIENNA) rectifier system realized by using the IXYS VUM25-E module is estimated and further possible developments of this module are discussed.

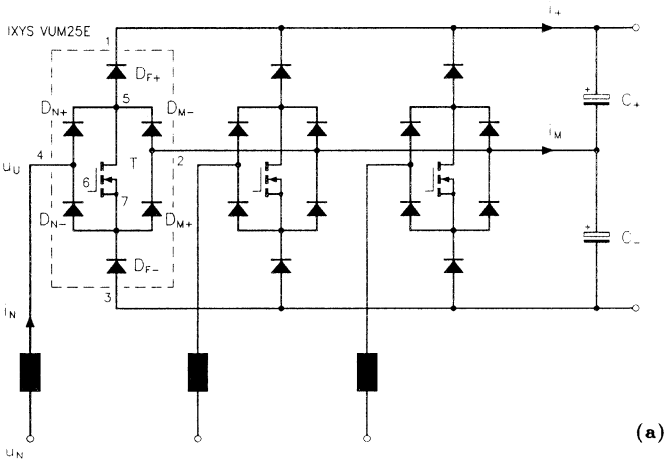
1 Introduction

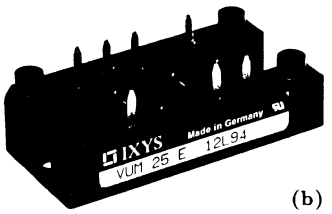
Due to the effort (based on guidelines [1], recommendations and regulations [2]) to limit the harmonic influence on the mains by power electronic systems the development of converter concepts having low effects on the mains becomes increasingly important. In general one strives for

- low circuit complexity and low component stress
- high power density
- high efficiency
- high reliability and
- controllability of the output voltage

besides obtaining a largely sinusoidal mains current shape (high power factor and low THD). In the area of three-phase unidirectional AC-to-DC power conversion these requirements can be met ideally by a three-phase/switch/level PWM (VIENNA) rectifier system proposed in [3]. The basic structure of the power circuit is shown in **Fig.1(a)**. The advantages of the system are especially

- the purely sinusoidal shape of the mains current (with the exception of harmonics having switching frequency) being in phase with the mains voltage (i.e., resistive fundamental mains behavior, high power factor);
- blocking voltage stress on the power semiconductors determined by only half of the output voltage (for a system operating in the European low voltage mains and for output voltages in the region U_O = 650...750 V the possibility of the application of power MOSFETs with a blocking voltage capability of U_{DSS} = 500 V and, therefore, with low on-resistance and low conduction losses is given; furthermore, low switching losses due to the low switching voltage of the valves and possibility of realization of the uncontrolled valves as fast recovery epitaxial diodes with a maximum blocking voltage U_{RRM} = 600 V; the parasitic intrinsic free-wheeling diodes (characterized by a high reverse recovery time) of the power MOSFETs are not used – high switching frequency and high power density of the system can be achieved;





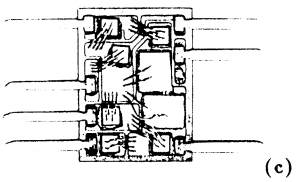


Fig.1: Structure of the power circuit of a three-phase unidirectional boost-type three-level PWM rectifier system according to [3] (cf. **(a)**). The combination of the power semiconductors of a bridge leg of the circuit developed at the Technical University Vienna/Austria (short: **VIENNA rectifier**) has been offered since 01/1995 by **IXYS Semiconductor GmbH** as power modul **IXYS VUM25-E**. The prototyp of this module is shown in **(b)**, the internal layout of the module is shown in **(c)** (dimensions of the ceramic base plate: 35mm x 26mm). The characteristics of the valves of the module are identical to those of a boost converter power module IXYS VUM24-05 as being used for single-phase power factor correction. Accordingly, the nominal output power of a VIENNA rectifier consisting of three modules **IXYS VUM25-E** amounts to $P_O \approx$ 16 kW (dependent on the switching frequency); the nominal value of the output DC voltage has to be set typically to U_O = 700 V if the system is employed in the European low-voltage mains (line-to-line voltage 400 V_{rms}).

- only one turn-off valve per phase (low control effort and high operating reliability); a short circuit of the output voltage in the case of a control error of the power transistors cannot occur due to the circuit structure);
- low rated power of the inductances connected in series on the mains side due to a three-level characteristic of the bridge legs (as compared to conventional two-level bridge circuits the value of the inductance can be reduced by about $\frac{1}{3}$ for equal harmonic level of the mains current and for equal switching frequency); this leads to an increase of the system power density and higher dynamic of the mains current control.

However, the circuit shows a relatively high assembly effort if a realization with discrete components is considered. This can be avioded to a large extent if the power semiconductors dies are contained in a power module.

Based on this consideration, ABB-IXYS Semiconductor GmbH has developed (in cooperation with the Power Electronics Section of the Technical University Vienna/Austria) the prototype of a power module shown in **Fig.1(b)** [4]. The basic thought has been to extend an already available single-phase PFC module (IXYS VUM24-05, cf. p. 86 in [5] or [6]) by adding of a power diode chip to the circuit structure of a bridge leg of the three-phase circuit shown in Fig.1(a). The inner structure of the module obtained thereby is shown in **Fig.1(c)**. The semiconductor chips are identical with the elements used in the discrete power semiconductor devices IXYS miniBLOC IXTN 36N50 (power MOSFET, cf. p. 75 in [5]) and IXYS miniBLOCK DSEI 2x30-06C (fast recovery epitaxial diode, cf. p. 28 in [7]). There, the power transistor is realized by a parallel conncetion of two MOSFET chips taken from the same wafer. For avoiding an influence of the power circuit on the contol circuit, the driving stages of the power transistors has been separated geometrically clearly from the power terminals and a Kelvin-Source contact has been provided (pin 7, cf. Fig.1(c)). For the package the outline known from three-phase bridge rectifier modules (series IXYS VUO16NO1 or IXYS VUO22NO1, cf. p. 18 or p. 20 in [8]) has been selected (overall dimensions of the module: 63mm x 31.6mm x 17mm). The power semiconductor chips are connected by a high temperature soldering process with a copper layer being applied directly on a ceramic-oxide substrate (direct copper bonding (DCB) process, cf. [9]). There, the connection of the single elements is realized by appropriate structurization of the copper layer and via wire bonding. The essential advantages of this construction are

- high packaging density
- minimization of parasitic lead inductances
- high isolation voltage
- very low thermal resistance of the ceramic substrate isolating the power semiconductors from the heat sink and, therefore, low thermal resistance of the power semiconductors (obtained by low thickness of the substrate (0.63mm) and high thickness (300 μm) of the copper layer).

Furthermore, one has to point out the higher reliability of the module as compared to assembling of discrete elements.

Remark: If the bridge legs of the circuit according to Fig.1 (a) are connected in delta, we receive a *two-level* PWM rectifier as introduced by W. Koczara in [10]. However, in this case the module cannot be applied in the European low voltage mains due to the higher blocking voltage stress on the valves for two-level operation (the blocking voltage of the two-level converter is determined by the total value of the output voltage).

The topic of this paper is now to summarize the results of the first practical tests of the power module and to develop guidelines for an industrial application of the module based on the determined characteristic values of the power semiconductors.

In **section 2** the switching losses of the power MOSFET and of a free-wheeling diodes of the module in dependency on the switched current for junction temperatures of T_j = 25°C and T_j = 110°C are determined. For the wiring of the semiconductor module with the passive components of the power circuit of a testing arrangement (corresponding to a phase leg of a three-phase system) we use a carefully designed printed circuit board (PCB) which minimizes the lead inductances. The current of the power switch is determined by using a shunt having high bandwidth. The turn-on and turn-off gate series resistors which essentially influence the switching losses are set with respect to the resulting switching overvoltages, the amplitude of the reverse recovery current and (as much as possible) avoidance of ringing between parasitic circuit elements (e.g., between output capacitance of the power transistor and lead inductances in connection with the inner inductance of the electrolytic capacitors on the DC (output) side). Based on the knowledge of the switching losses in dependency on the switched current the mean switching loss within a mains period are calculated for an assumed sinusoidal shape of the switched current via simple analytical approximations.

The calculation of the conduction losses of the power module is subject of **section 3**. The forward characteristic of the power diodes is approximated there by a current-independent forward voltage drop and a differential resistance. (The forward properties of the power MOSFET are characterized by its on-state resistance $R_{DS,on}$.) For the loss-determining average and rms values of the semiconductor currents analytical relationships are given which are derived under consideration of the phase-symmetrical structure of the power circuit and the symmetry of the mains current system. If these approximations are taken into account, the mean and rms values of all device currents (and, therefore, the on-state losses of the semiconductor elements) can be calculated directly for given peak value of the mains current and given voltage transformation ratio of the system (ratio of output voltage to the amplitude of the mains line-to-line voltage).

In **section 4** the relationships derived in section 3 are used for determining the maximum obtainable mains current amplitude and three-phase power of the rectifier system (for given switching frequency and given maximum allowable junction temperature and heat sink temperature). The power loss contributions of the semiconductor elements of the module resulting for different switching frequencies are compiled. Also, the efficiency reduction caused by the semiconductor losses is determined. Therefore, for a practical application of the module an essential support is given, especially concerning the selection of the switching frequency.

Finally, in **section 5** there is given an estimate of the overall efficiency of the rectifier system to be expected and the possibilities of further developments of the module are discussed.

2 IXYS VUM25-E Switching Evaluation

For measuring the switching losses of the power semiconductors of the module we use the arrangement shown in **Fig.2**. Between positive output voltage bus and output voltage center point a DC voltage ($\frac{1}{2}U_O$=350 V) is impressed having half of the nominal output voltage to be provided for a later realization. Between AC-side module input and positive output voltage bus a resistive-inductive load is inserted giving the test circuit the structure of a buck converter with free-wheeling diode D_{F+}. By the circuit arrangement the on-states and the commutation processes of the module within the positive mains current half period are determined. When the power transistor is in the on-state, we have a current flow via the mains side diode D_{N+}, the transistor T and the center point diode D_{M+}. Due to turning-off T the input current of the module commutates into the free-wheeling diode D_{F+}. Although the diodes D_{N+} and D_{M+} participate in conducting the current, they do not show any blocking voltage stress. The diodes D_{F-}, D_{N-} and D_{M-} remain free of current.

As section 2.4 shows, the total switching losses of the module are essentially determined by the turn-on and turn-off losses of the power transistor. As further switching loss contributions there occur forward-recovery losses and turn-off losses of D_{F+} (or of D_{F-} if the direction of the input current is reversed) and forward-recovery losses of D_{M+} (or D_{M-}).

As already mentioned before, no blocking voltage results across D_{M+} in the circuit according to Fig.2. The reason for this is that at turning-off of T the forward current becomes zero and no inverse current flow results which would remove the diffusion charge of the diode (an exception could be caused by oscillations between lead inductances and the output capacitance of T). The stored electric charge is decreased by recombination. Therefore, there is no special requirement concerning the reverse-recovery behavior of the diodes D_{M+} and D_{M-}.

A minimization of the switching losses of the power transistor can only be obtained by a switching speed as high as possible. In order to limit the switching overvoltages occurring there due to the high di/dt-rates we have to provide as closely as possible a biplanar arrangement of commutating current paths which can be achieved, e.g., using a proper designed double-sided printed circuit board.

For damping of the oscillations of the drain-source voltage of T following the turn-off process an RC-snubber is inserted between the circuit nodes 5 and 2' (cf. Fig.2). (For negative input currents the RC-snubber would have to be inserted between points 5 and 4.) The application of one RC-snubber each for each current direction is required here because the prototype of the module has only a Kelvin-source contact for the control of T. It does not have a power source terminal. In the case that the module would have an

explicite source terminal an RC damping network could be inserted directly between drain and source of T. The dimensioning of the RC-snubber will be treated in section 2.2.

We have to point out that wiring of the power circuit takes immediate influence on the possible minimization of the switching losses. Therefore, the layout of the printed circuit board used for measuring the switching losses (and the optimization of the gate drive) has to correspond already with the layout of a bridge leg of the three-phase system which finally has to be realized. In order to obtain phase building blocks of equal structure we therefore have decided to replace each output capacitor (C_+ or C_-, respectively) by a parallel connection of three individual capacitors. Therefore, two individual capacitors (330 μF/400 V, one for the positive half leg and one for the negative half leg) are allocated to each of the three phases. It is important to note that no oscillations (due to the switching process) can occur between the parallel capacitors. This is due to the relatively high parasitic equivalent series resistances of the electrolytic capacitors ($R_{\mathrm{ESR}} \approx 0.15\,\Omega$, $L_{\mathrm{ESL}} \approx 20\,nH$). If the electrolytic capacitors would be conneted in parallel with foil capacitors C_{F} in order to improve the buffering action for high frequencies (cf. Fig.6 in [11]) C_{F} would have to be <100 nF for retaining a sufficient damping of the overall system.

2.1 Power PCB Layout

Dependent on the sign of the mains current for a switching of the power transistor a commutation of the DC-side current flow is performed between positive output voltage bus and output voltage center point or between negative output voltage bus and output voltage center point. (Contrary to two-level converters no direct commutation between positive and negative output voltage bus takes place.) For minimization of the switching overvoltages we have to minimize the area enclosed by the respective connection leads (in Fig.2 marked by a dotted area, related to positive mains current), i.e., the parasitic inductance L_{c} of the commutation path has to be minimized. This is obtained by a planar design and biplanar arrangement of the critical wiring using a double-sided power printed circuit board. There, it is of advantage, to position the positive and negative voltage bus area above the area of the center point bus (which is located on the bottom side of the printed circuit board) and to orient the output capacitors terminals in the direction of the current flow (rectangular to the longitudinal axis of the power module) [12]. As measurements show there remains a wiring inductance of only $\approx$ 5 nH (especially caused by the isolation distances to be observed) for optimized layout of the power PCB. In connection with the inner inductance $L_{\mathrm{ESL}} \approx 20$ nH of the electrolytic capacitor (buffering one output partial voltage) and with the estimated lead inductance of the module of ($\approx$ 10 nH) there results a very low total value ($L_{\mathrm{c}} \approx$35 nH) of the inductance of the critical current path and/or low amplitudes of the turn-off overvoltages occurring across the power transistor also for high switching speed (50 V for 1500 A/μs). Therefore, one can achieve a minimization of the turn-off losses of the power semiconductors by appropriate gate control of the power transistor minimizing the turn-off time.

Remark: As mentioned previously, the switching losses of the module are investigated for one phase building block of the rectifier system. According to Fig.1(a) the output capacitors of the three single phase building blocks are connected in parallel for realization of the three-phase system. The contribution of the parasitic inductance of the output capacitors to the inductance of the critical current path is therefore reduced from $\approx$ 20 nH to $\approx$ 7 nH. In a three-phase arrangement we therefore have to expect a lower value of the switching overvoltages as compared to the single-phase test circuit (for equal value of the switched current) but a higher peak value of the reverse recovery current of the diode. Therefore, an application of separate foil capacitors connected in parallel to the electrolytic capacitors is not necessary.

2.2 Gate Drive

The switching speed of a power MOSFET can be defined via the value of the gate series resistor where also the source impedance of the driver circuit has to be considered. There, a compromise has to be found between the reduction of the switching losses (given for a reduction of the gate series resistance) and the increase of the occurring turn-off overvoltage or the increased amplitude of the reverse recovery current of the free-wheeling diode during turn-on. Furthermore, the higher excitation of high-frequency ringing between parasitic elements in the power and control circuits for higher switching speed has to be considered. (Such ringing might occur, e.g., between output capacitance of the power transistor and the wiring inductance or between the input capacitance of the transistor and the lead inductances of the driver circuit.)

As a more detailed analysis of the switching behavior shows (cf. section 2.4)

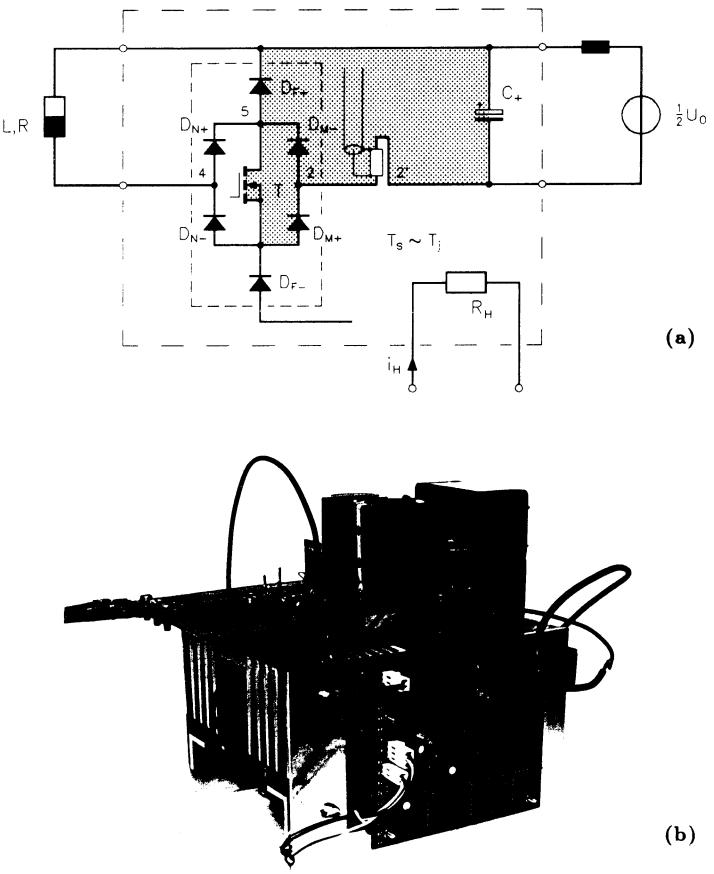


Fig.2: Experimental circuit for measuring the switching power losses; **(a):** structure of the power circuit of the test arrangement; **(b):** practical realization of the experimental circuit.

the insertion of an RC damping network $C_{\mathrm{D}} = 470\,\mathrm{pF}$, $R_{\mathrm{D}} = 10\,\Omega$ between the circuit nodes 5 and 2' (cf. Fig.2) results in a sufficient damping of the oscillation following the turn-off of T (cf. Fig.6). For the dimensioning of the damping resistor one has to consider $R_{\mathrm{D}} > 2\sqrt{L_{\mathrm{c}}/C_{\mathrm{D}}}$ in general (cf. e.g., p. 166 in [13]). Due to the low capacity value C_{D} there is no reduction of the turn-off overvoltage obtained, however. On the other hand, the energy loss in R_{D} remains limited to low values even for high switching frequency.

For an isolated gate drive of the power MOSFET the IC combination UC3724/ UC3725 of Unitrode Corp. is applied (cf. **Fig.3**). The realization of the driver circuit is described in [14]. Therefore, a more detailed description can be omitted here. With regard to low on-state losses of the MOSFET, $U_{GS,\mathrm{on}} = 15\,\mathrm{V}$ is chosen. For protection of the gate against voltage spikes a zener diode (break-down voltage 16V) connected immediately at the control terminals of the power module is applied.

In order to make a arbitrary adjustment of the turn-on and turn-off speed of the power transistor possible, a complementary emitter follower is connected in series to the integrated driver circuit. (The output current of the driver IC UC3725 is limited to <2A according to its data sheet.) The values $R_{G,\mathrm{on}} = 4.3\,\Omega$ and $R_{G,\mathrm{off}} = 1.2\,\Omega$ of the emitter resistors of the driver stage which define the switching times were determined experimentally during measurement of the switching losses.

For the purpose of a worst-case consideration, we have to analyze the turn-on process of the power transistor for the *maximum* junction temperature (here $T_{\mathrm{j}} = 110°\mathrm{C}$, cf. p. 282 in [15]) of the free-wheeling diode D_F in order to determine the resistance $R_{G,\mathrm{on}}$. Due to the fact that the reverse recovery current of D_F is increased with rising T_{j}, for this junction temperature the critical case regarding the peak current stress of the transistor is covered. In contrary, $R_{G,\mathrm{off}}$ is determined via consideration of the turn-off process for *low* junction temperature ($T_{\mathrm{j}} \approx 25°\mathrm{C}$). There the higher switching speed (and therefore the higher switching overvoltage) for lower junction temperature is considered.

For $R_{G,\mathrm{off}} = 1.2\,\Omega$ a maximum turn-off overvoltage (110V) of the power transistor occurs for $i_T = 50\,\mathrm{A}$ and $T_{T,\mathrm{j}} = T_{D_F,\mathrm{j}} = 25°\mathrm{C}$. Therefore, a

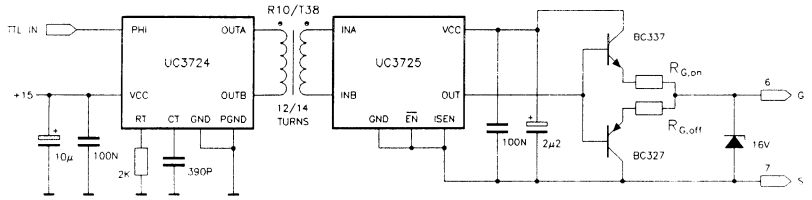


Fig.3: Circuit diagram of the driver stage as used for measurement of the switching losses of the power module. The driver circuit requires a PCB area of about 5cm x 1.5cm if realized in conventional (non-SMD) technology.

safety margin of 40 V remains for $\frac{1}{2}U_O = 350\,\mathrm{V}$ as compared to the drain-source break-down voltage of $U_{DSS} = 500\,\mathrm{V}$. With this, also for a transient unsymmetry of the partial output voltages a safe operation of the module is guaranteed. Furthermore, this makes possible to keep the actual blocking voltage resulting at the MOSFET chip (which is higher than the voltage stress measured at the terminals of the module due to its inner wiring inductance) safely below U_{DSS}.

$R_{G,\mathrm{on}} = 4.3\,\Omega$ leads for $i_T = 50\,\mathrm{A}$ and $T_{D_F,\mathrm{j}} = T_{T,\mathrm{j}} = 110°\mathrm{C}$ to a peak value $I_{D_F,RM} = 45\,\mathrm{A}$ of the reverse recovery current of the free-wheeling diode. Then, for low turn-on losses the thermally maximum allowable peak current stress of the transistor is not reached even for higher junction temperatures $T_{D_F,\mathrm{j}}$. The experimental analysis shows that a reduction of $R_{G,\mathrm{on}}$ only marginally reduces the turn-on losses but the peak value of the reverse recovery current is still increased.

Remark: As can be seen immediately from the structure of the power circuit (cf. Fig.1(a)), for the VIENNA rectifier (contrary to two-level bridge circuits) no short circuit of the output voltages can occur for a control failure of the power transistor. Therefore, the overcurrent protection feature of the driver IC UC3725 is not applied here.

2.3 Current Measurement Technique

Due to the system propagation delay ($\approx 30\,\mathrm{ns}$ [16]) of a clip-on type current probe in combination with a current probe amplifier (Tektronix A6302 in combination with Tektronix AM503) being too high for an exact determination of the switching power loss (cf. p. 1.702 in [17]) and due to the fact that an insertion of a current probe into the critical current path changes the inductance conditions and/or the switching overvoltages, the measurement of the transistor current is performed via a low-inductance shunt as proposed in [18] (cf. **Fig.4**). The shunt is realized by ten $1\,\Omega$-SMD resistors connected in parallel. They are inserted into the current path which is realized in a biplanar fashion via a PCB with a copper layer on both sides connected at the front end.

As can be checked by calculation the change of the lead inductance of the critical current path by the shunt is constrained to $< 2\,\mathrm{nH}$. Therefore, it can be neglected concerning measurement influences. The voltage drop of the current to be measured is taken directly across the SMD resistors by a coaxial cable RG174 (characteristic impedance $50\,\Omega$) with a matched termination in order to avoid reflections at the oscilloscope input. In connection with situating the cable in a zone of the shunt with low magnetic field (cf. Fig.9 in [18]) the influence by an inductive voltage component is avoided therefore. The length of the coaxial cable is chosen such that a signal delay time results which is identical to the delay time occurring for measuring the voltage drop across the shunt resistors by a voltage probe. By this a minimum error is guaranteed for the switching losses which are gained by multiplication of transistor current and transistor voltage.

A comparison measurement shows (with the exception of the signal delay mentioned before) an identical shape of the measurement signals for the current measurement system Tektronix A6302/AM503 (bandwidth: DC-to-50 MHz) and for the low-inductance shunt (cf. **Fig.5**).

Remark: The shunt is not applicable for measurements over extended on-intervals of T due to the generated heat caused by its high resistance ($100\,\mathrm{m}\Omega$). For measurement of the switching losses of the power module the temperature rise of the shunt remains low due to the short pulse duration and the low repetition frequency of the considered on-off-on-off-cycles. Considering the very low temperature coefficient of the used metal film SMD resistors the temperature error can be neglected therefore. An advantage of the relatively high resistance value is the higher corner frequency of the frequency response of the shunt (according to $\omega_K = R_R/L_R$) as compared to a low-resistance shunt of equal geometric design as would be applicable for continuous operation.

2.4 Switching Behavior

The results of the measurements of the switching losses of the power MOSFET of the module for $\frac{1}{2}U_O = 350\,\mathrm{V}$, $R_{G,\mathrm{on}} = 4.3\,\Omega$ and $R_{G,\mathrm{off}} = 1.2\,\Omega$ are compiled in **Fig.6**. The losses are measured based on on-off-on-off-switching cycles of short pulse duration and low repetition rate [19]. Due to the then following low junction temperature rise of the power semiconductors only a small deviation of the junction temperature from the case and heat sink temperature results. Therefore, the adjustment of the junction temperature (which has to kept constant for a measurement series) can be achieved using a proper pre-heating of the heat sink (cf. R_H in Fig.2).

The measurements have been carried out by using a digital storage oscilloscope TEK TDS 544A (500 MHz, 1 Gs). For the voltage acquisition probes TEK P6139A (500 MHz) have been used. It is important to point out that the voltage measurement has to be done directly between drain and Kelvin-source of the power transistor. (It must not be related to the ground terminal of the low-inductance shunt.) This can be explained by the fact that for turning-on of T there results a transient voltage (which cannot be neglected) consisting of the forward-recovery voltage of $D_{\mathrm{M}+}$ and the inductive voltage drop across lead inductances inside the module. This transient voltage would lead to an apparent increase of the turn-on voltage of T and, therefore, also to an increase of the measured turn-on loss. For the turn-off process the transistor voltage woud be apparently reduced by an inductive voltage drop of opposite sign. Besides the measurement of too low turn-off power losses there would exist (e.g., during the course of optimizing the turn-on gate resistor $R_{\mathrm{G,on}}$) the danger of exceeding the maximum admissible blocking voltage of the transistor. The reason is, that due to the error in the voltage measurement an apparent safety margin to the blocking voltage limit would be pretended.

As Fig.6(a) shows, the free-wheeling diodes D_F of the power module show a pronounced soft-recovery behavior. In connection with the low-inductance wiring design of the power circuit therefore no turn-off overvoltage of the free-wheeling diode occurs.

As a closer analysis shows and as can be checked for the power transistor by Fig.6(e), the measured switching power losses of the power devices (power transistor, free-wheeling diodes, center point diodes) can be expressed by a linear dependency

$$w_P = k_{\mathrm{P}} i_N \qquad (1)$$

on the switched current i_N with good approximation. For the sum of turn-on and turn-off loss of the power transistor T there follows according to Fig.6(e)

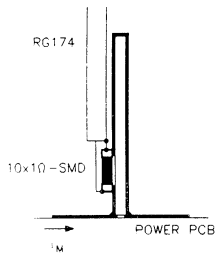


Fig.4: Low-inductance shunt for measurement of the transistor current; **(a)**: principle of design; **(b)**: practical realization.

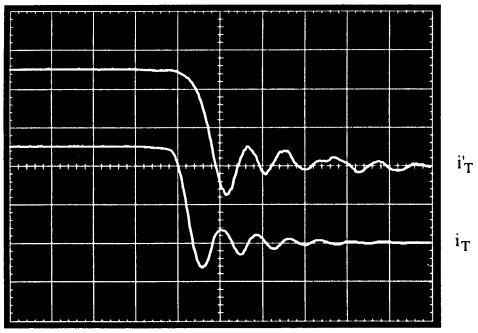


Fig.5: Comparison of the current measurement system TEK A6302/AM503 and of the current acquisition by a low-inductivity shunt (cf. Fig.4) for the example of turn-off of the power transistor. The current acquisition by the clip-on current probe A6302 (cf. i'_T) shows a delay time $T_t \approx 25\,\text{ns}$ being inadmissible high for an exact measurement of the switching power loss.

$$k_{T,\mathrm{P}}|_{T_{T,\mathrm{j}}=110^\circ\mathrm{C}} = 55\,\frac{\mu\mathrm{Ws}}{\mathrm{A}}\,.$$

The switching losses of the free-wheeling diodes (sum of forward-recovery loss and turn-off power loss) can be described by

$$k_{D_F,\mathrm{P}}|_{T_{D_F,\mathrm{j}}=110^\circ\mathrm{C}} = 6\,\frac{\mu\mathrm{Ws}}{\mathrm{A}}\,.$$

For determination of this characteristic value the forward-recovery losses are calculated based on the data sheet (cf. p. 29, Fig.6 in [7]); the turn-off losses are determined based on the signal shapes measured for the turn-on process of the power transistor.

The switching losses of the center point diodes D_M are caused exclusively by the forward-recovery losses. There follows

$$k_{D_M,\mathrm{P}}|_{T_{D_F,\mathrm{j}}=110^\circ\mathrm{C}} = 2\,\frac{\mu\mathrm{Ws}}{\mathrm{A}}\,.$$

Based on the characterization of the switching losses of the semiconductor devices according to Eq.(1) one can now (as shown in more detail in the next section) calculate in a simple way the switching losses of the elements averaged within the mains period.

3 Calculation of the Average Values of the Switching Power Losses

If the power module is applied as bridge leg of a three-phase PWM rectifier system a sinusoidal variation of the switched current and, therefore, also of the switching power losses results over the mains period. Due to the thermal inertia of the power semiconductors (cf. [5], p. 89, Fig.19) one can limit the consideration to the average value of the switching power losses related to one mains period, however.

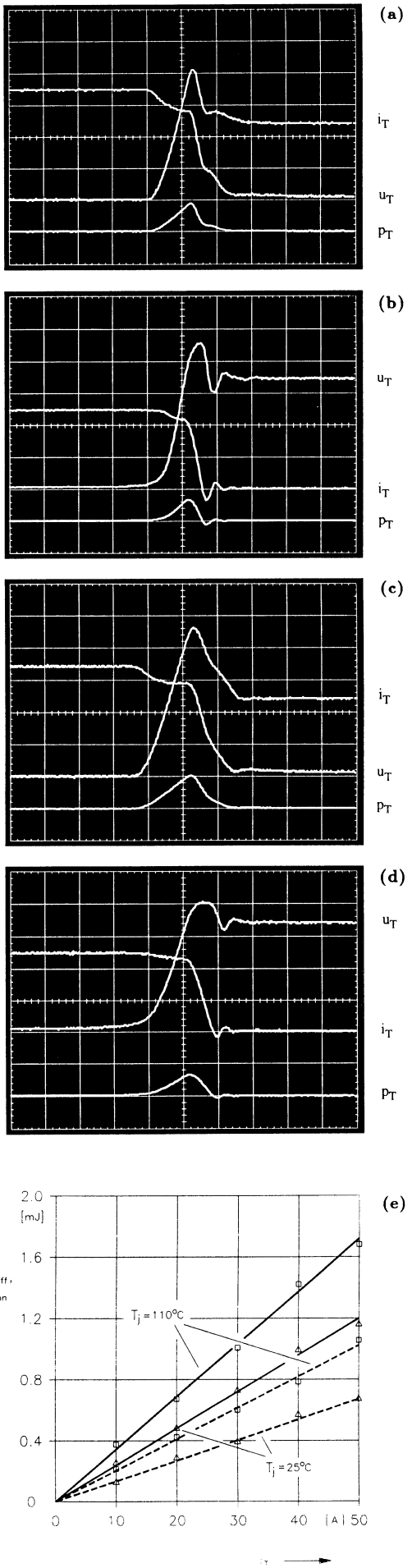


Fig.6: Analysis of the turn-on and turn-off behavior of the power transistor. **(a)** and **(b)**: turn-on and turn-off for $T_\mathrm{j} = 25^\circ\mathrm{C}$ (refers to all semiconductor elements of the module), representation of transistor current i_T (20 A/div), transistor voltage u_T (100 V/div) and power loss p_T (25 kW/div). **(c)** and **(d)**: as (a) and (b) but $T_\mathrm{j} = 110^\circ\mathrm{C}$. **(e)**: dependency of transistor turn-on and turn-off energy loss on the switched current and on the junction temperature T_j; current dependency of the turn-off energy shown by dashed lines. Time scale: 50 ns/div. Gate voltage levels: $U_\mathrm{GS} = 0, +15\,\mathrm{V}$, emitter resistors of the driver stage: $R_{G,\mathrm{on}} = 4.3\,\Omega$, $R_{G,\mathrm{off}} = 1.2\,\Omega$. The reduction of i_T during the rise of u_T during turn-off is based on the effect of the RC damping network (inserted between nodes 5 and 2', cf. Fig.2) as turn-off snubber. The reduction of u_T during the rise of i_T during turn-on shows the parasitic inductance L_c of the critical current path (cf. Fig.2).

For the calculation of simple analytical expressions of the average values of the the switching power losses of the semiconductor devices we assume (i) constant switching frequency f_P and, (for the sake of concentrating on the essentials) (ii) a purely sinusoidal shape of the switched current (neglection of the current ripple)

$$i_N = \hat{I}_N \sin(\varphi_N) \qquad \varphi_N = \omega_N t \ . \tag{2}$$

Within a mains period one can now assign to each pulse interval a switching loss energy

$$w_P = w_{P,\text{off-on}} + w_{P,\text{on-off}} = k_P i_N\{\varphi_N\} \tag{3}$$

of the respective considered device being dependent on the local value $i_N\{\varphi_N\}$. Also, one can define a local switching power loss

$$p_P = \frac{1}{T_P} w_P = w_P \, f_P \ . \tag{4}$$

The average value of the switching power loss related to a mains period follows therefore for the power transistor via

$$P_{T,P} = \frac{1}{\pi} \int_0^{\pi} k_{T,P} \, i_N\{\varphi_N\} f_P \, d\varphi_N \ . \tag{5}$$

For the free-wheeling diodes D_F and the center point diodes D_M we have due to the limitation of the current flow to a mains half period

$$P_{D,P} = \frac{1}{2\pi} \int_0^{\pi} k_{D,P} \, i_N\{\varphi_N\} f_P \, d\varphi_N \ . \tag{6}$$

There, we have to insert for the factor $k_{D,P}$ (corresponding to a linear current dependency of the switching losses) the values $k_{D_F,P}$ or $k_{D_M,P}$ as given in section 2.4.

3.1 Power Transistor

Besides the power loss contribution defined by Eq.(5) (which can be determined by measuring the external transistor current) we have to consider for a more detailed analysis also the power loss occurring for each turn-on process due to discharging the output capacitance C_{oss} of the power MOSFET. For the voltage dependent capacitance we use – as a first approximation – the value valid for the nominal blocking voltage ($C_{oss} \approx 1\,\text{nF}$, cf. [5], p. 88, Fig.8). For the average value of the total switching losses of the power transistor there follows then by considering of Eq.(5)

$$P_{T,P} = \frac{2k_{T,P}}{\pi} f_P \hat{I}_N + \frac{1}{2} C_{oss} \left(\frac{U_O}{2}\right)^2 f_P \tag{7}$$

($k_{T,P}|_{T_{T,j}=110°C} = 55 \, \frac{\mu Ws}{A}$, cf. section 2.4).

3.2 Power Diodes

For the average values of the switching power losses of the diodes D_F and D_M there follows under consideration of Eq.(6)

$$P_{D_F,P} = \frac{k_{D_F,P}}{\pi} f_P \hat{I}_N \qquad P_{D_M,P} = \frac{k_{D_M,P}}{\pi} f_P \hat{I}_N \ . \tag{8}$$

($k_{D_F,P}|_{T_{D_F,j}=110°C} = 6 \, \frac{\mu Ws}{A}$, $k_{D_M,P} \approx 2 \, \frac{\mu Ws}{A}$, cf. section 2.4).

4 Calculation of the Average Values of the Forward Losses

4.1 Forward Characteristics of the Power Semiconductor Devices

4.1.1 Power Diodes

The forward characteristics of the power diodes as known from the data sheet (cf. p. 88, Fig.10 in [5]) are approximated according to

$$u_{D,F} = U_{F,0} + r_D i_D \tag{9}$$

by a current-independent forward voltage drop $U_{F,0}$ in addition to a differential resistance r_D. In general, the average forward power loss of a power diode can be calculated then by

$$P_D = U_{F,0} I_{D,\text{avg}} + r_D I^2_{D,\text{rms}} \ . \tag{10}$$

The forward characteristics of the diodes D_M are described by $U_{F,0} = 1.25\,\text{V}$ and $r_D = 10\,\text{m}\Omega$ (related to $T_{D_M,j} \approx 85°C$, cf. section 6). For the diodes D_N and D_F we set $U_{F,0} = 1.15\,\text{V}$ and $r_T = 10\,\text{m}\Omega$ (related to $T_{D,j} \approx 100°C$) due to the current stress (being higher than for D_M) and due to the then higher junction temperature.

4.1.2 Power Transistor

Basically one has to consider the dependency of the on-state resistance on the gate voltage, the junction temperature and the magnitude of the drain current for calculation of the conduction losses of a power MOSFET. The current dependency of the on-state resistance is neglected on purpose for the sake of simplifying the calculation. This is due to the fact that the overall losses of the power transistor are essentially determined by the switching losses as the considerations in section 6 show. The on-state characteristic of the power transistor is described by a resistor $R_{DS,\text{on}}\{T_j\}$ which is only dependent on the junction temperature due to the fixed gate voltage $U_{GS,\text{on}} = 15\,\text{V}$. As reference value we set $R_{DS,\text{on}}|_{T_j=25°C} = 0.122\,\Omega$ (for $I_T = 25\,\text{A}$). The correction factor for the calculation of the actual resistance for a defined junction temperature can be taken from the data sheet; e.g., we have for $T_{T,j} = 110°C$

$$R_{DS,\text{on}}|_{T_j=110°C} = 1.85 \; R_{DS,\text{on}}|_{T_j=25°C} = 0.225\,\Omega$$

(cf. p. 88, Fig.5 in [5]).

The average value of the forward power losses related to a mains period follows via

$$P_{T,F} = I^2_{T,\text{rms}} R_{DS,\text{on}}\{T_j\} \ . \tag{11}$$

4.2 Current Stresses of the Power Semiconductor Devices of a Bridge Leg

In the following the current average and rms values are calculated as required for the calculation of the on-state losses of the semiconductor elements according to section 4.1. Simple approximation formulas are derived which can be used beyond the scope of this paper for dimensioning of the power semiconductors of a bridge leg of the VIENNA rectifier system. As already assumed for the calculation of the switching losses (cf. section 3) we again assume

- purely sinusoidal phase current shape and
- constant switching frequency f_P .

To this the assumption of

- purely resistive behavior of the mains voltage and current fundamentals (no phase displacement between mains voltage and the related mains current)

is added. Furthermore, we

- neglect the mains frequency voltage drop across the AC side input inductances L (cf. Fig.1(a))

(this voltage drop shows typically a few percent of the mains voltage amplitude). For the simplest case the gating of the power transistor has to form a local voltage average at the input of the module

$$u_{U,\text{avg}}\{\varphi_N\} = (1 - \alpha_T\{\varphi_N\}) \frac{U_O}{2} \approx u_N\{\varphi_N\} = \hat{U}_N \sin\varphi_N \tag{12}$$

being equal to the related mains phase voltage. The time variation of the relative on-time α_T of the power transistor (essentially determining the forward losses of the module) can, therefore, be given directly for given output voltage independently of the amplitude of the mains phase current.

Remark: Regarding the assumption of constant switching frequency we have to point out that (as a digital simulation shows) the approximations calculated here are valid with high accurracy also for not constant switching frequency (e.g., for hysteresis control of the mains current). Regarding the local averaged (averaging within the pulse period) voltage at the input of the power module we want to point out that this voltage (dependent on the modulation method selected) also can obtain a non-sinusoidal shape. (A non-sinusoidal

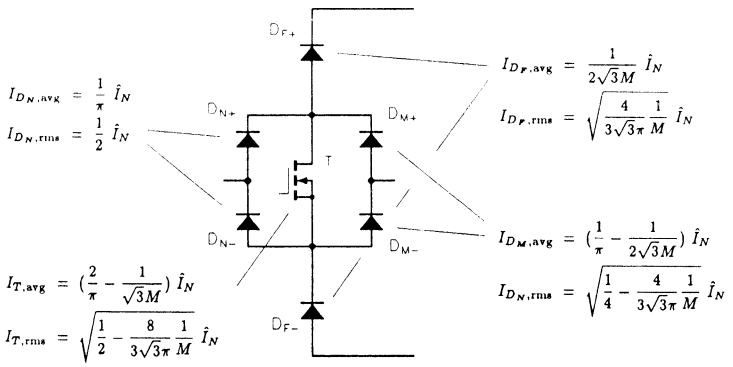


Fig.7: Compilation of the results of the analytical approximating calculation of mean and rms values of the device currents and of the averaged switching power losses (in dependency on the mains current amplitude $\hat{I}_N$ and on the voltage transformation ratio $M = U_O/\sqrt{3}\hat{U}_N$, $\hat{U}_N$: amplitude of the mains phase voltage).

shape is present, e.g., for minimization of the mains current harmonics of the three-phase system via addition of zero-voltage components.) According to the results of a checking calculation (which is omitted here for the sake of brevity) this only influences essentially the local conduction losses. The average values of the local conduction losses within a mains period remain largely unchanged.

For the sake of brevity in the following only basic considerations regarding the derivations are discussed. The resulting characteristic values of the semiconductor currents are compiled in **Fig.7**.

4.2.1 Diodes D_{N+} and D_{N-}

Dependent on the sign of the mains current only diode D_{N+} or diode D_{N-} takes part in conducting the current during the half fundamental (mains) period. The average and rms values of the diode current i_{D_N} therefore are calculated via

$$I_{D_N,\mathrm{avg}} = \frac{\sqrt{2}}{\pi} I_{N,\mathrm{rms}} \qquad I_{D_N,\mathrm{rms}} = \frac{1}{\sqrt{2}} I_{N,\mathrm{rms}} \; . \tag{13}$$

4.2.2 Power Transistor T

Based on the given time behavior of α_T (cf. Eq.(12)) there follow approximations of the transistor average and rms values via

$$I_{T,\mathrm{avg}} = \frac{1}{\pi}\int_0^\pi i_N\, \alpha_T\, d\varphi_N \qquad I^2_{T,\mathrm{rms}} = \frac{1}{\pi}\int_0^\pi i_N^2 \alpha_T\, d\varphi_N \; . \tag{14}$$

The average value of the transistor current can be calculated alternatively also via using the node equations

$$i_T = \begin{cases} i_{D_{N+}} - i_{D_{F+}} & \text{for } i_N > 0 \\ i_{D_{N-}} - i_{D_{F-}} & \text{for } i_N < 0 \end{cases} \tag{15}$$

(diode currents counted positive in forward direction) and

$$I_{T,\mathrm{avg}} = 2I_{N,\mathrm{avg}} - 2I_{D_F,\mathrm{avg}} \; . \tag{16}$$

The average value $I_{D_F,\mathrm{avg}}$ of the free-wheeling diode current required there will be derived in section 4.2.4.

4.2.3 Center Point Diodes D_{M+} and D_{M-}

During the positive mains current half cycle the transistor current flows in the diode D_{M+}, during the negative mains current half cycle in the diode D_{M-} to the output voltage center point. The average and rms values of the center point diode current follow therefore via

$$I_{D_M,\mathrm{avg}} = \frac{1}{2} I_{T,\mathrm{avg}} \qquad I_{D_N,\mathrm{rms}} = \frac{1}{\sqrt{2}} I_{T,\mathrm{rms}} \; . \tag{17}$$

4.2.4 Free-Wheeling Diodes D_{F+} and D_{F-}

If the reduction of the output power (caused by the losses) of the rectifier

average value $I_{D_F,\mathrm{avg}}$ of the free-wheeling diode current directly based on the power balance

$$P_N = \frac{3}{2}\hat{U}_N\hat{I}_N \approx I_{+,\mathrm{avg}}U_O + I_{M,\mathrm{avg}}\frac{U_O}{2} = P_O \; . \tag{18}$$

There, a time-constant output voltage U_O is assumed. Because a control of the potential of the output voltage center point suppresses the existance of an average value $I_{M,\mathrm{avg}} \neq 0$ of the center point current, the output power is only determined by $I_{+,\mathrm{avg}}$. This current average value is produced in equal parts by the single bridge legs due to the phase symmetry of the circuit structure and due to the always same direction of the free-wheeling diode currents (of the phases) feeding the positive output voltage bus. Therefore we receive

$$I_{D_F,\mathrm{avg}} = \frac{1}{3} I_{+,\mathrm{avg}} \; . \tag{19}$$

For calculation of the rms value $I_{D_F,\mathrm{rms}}$ we have to apply the node equation

$$i_{D_{F+}} = i_{D_{N+}} - i_T \tag{20}$$

being valid for the positive mains current half cycle $i_N > 0$. Furthermore, we have to consider that the free-wheeling diode $D_{F,+}$ and the transistor T carry the current flow always alternatively. Therefore, we have

$$i_{D_F+} i_T \equiv 0 \; . \tag{21}$$

From this there follows

$$\frac{1}{2\pi}\int_0^\pi i^2_{D_{N+}} d\varphi_N = \frac{1}{2\pi}\int_0^\pi i^2_{D_{F+}} d\varphi_N + \frac{1}{2\pi}\int_0^\pi 2 i_{D_{F+}} i_T d\varphi_N + \frac{1}{2\pi}\int_0^\pi i^2_T d\varphi_N \tag{22}$$

or

$$I^2_{D_N,\mathrm{rms}} = I^2_{D_F,\mathrm{rms}} + \frac{1}{2} I^2_{T,\mathrm{rms}} \tag{23}$$

respectively. Thereby the rms value $I_{D_F,\mathrm{rms}}$ of the free-wheeling current can be given directly with consideration of Eqs.(13,14).

5 Mains Current Peak Value Allowable with Regard to Temperature

In connection with a practical realization of a PWM rectifier system especially the obtainable maximum output power $P_{O,\max}$ (for a specific switching frequency f_P and heat sink temperature T_s) is of interest.

According to Eq.(18) for fixed mains voltage amplitude the maximum rectifier power is defined by the allowable maximum value $\hat{I}_{N,\max}$ of the mains current amplitude and, therefore, finally by the switching and conduction losses in connection with the allowable thermal stress on the power semiconductors.

For a calculation of $\hat{I}_{N,\max}$ we have to set for each power semiconductor device of the module a maximum allowable value of the junction temperature $T_{j,\max}$. With this, we have to determine the maximum allowable semiconductor loss

$$P_{\max} = \frac{1}{R_{\mathrm{th,j-s}}}(T_{j,\max} - T_s) \tag{24}$$

for a given heat sink temperature T_s. If one sets this power loss equal to the sum of the conduction and the switching losses (known from section 3 and section 4 in dependency on the mains current amplitude)

$$P_{\max} = P_F\{\hat{I}_{N,\max}\} + P_P\{\hat{I}_{N,\max}\} \; , \tag{25}$$

then one can calculate directly the mains current amplitude $\hat{I}_{N,\max}$ for the respective considered device. The allowable stress on the module is then defined by that semiconductor element which shows the lowest value $\hat{I}_{N,\max}$.

As a comparison (which is not presented here in detail) of the thermal stresses

For a calculation of $\hat{I}_{N,\max}$ we have to set for each power semiconductor device of the module a maximum allowable value of the junction temperature $T_{\mathrm{j,max}}$. With this, we have to determine the maximum allowable semiconductor loss

$$P_{\max} = \frac{1}{R_{\mathrm{th,j-s}}}(T_{\mathrm{j,max}} - T_{\mathrm{s}}) \tag{24}$$

for a given heat sink temperature T_{s}. If one sets this power loss equal to the sum of the conduction and the switching losses (known from section 3 and section 4 in dependency on the mains current amplitude)

$$P_{\max} = P_{\mathrm{F}}\{\hat{I}_{N,\max}\} + P_{\mathrm{P}}\{\hat{I}_{N,\max}\} \ , \tag{25}$$

then one can calculate directly the mains current amplitude $\hat{I}_{N,\max}$ for the respective considered device. The allowable stress on the module is then defined by that semiconductor element which shows the lowest value $\hat{I}_{N,\max}$.

As a comparison (which is not presented here in detail) of the thermal stresses on the power semiconductor devices of the module shows (cf. Tab.1), in the case at hand in the technically interesting switching frequency region $f_{\mathrm{P}} = 25\,\mathrm{kHz}\ldots 100\,\mathrm{kHz}$ the obtainable output power of the rectifier system is limited by the value $\hat{I}_{N,T,\max}$ which is related to the power transistor. Considering Eq.(7), Eq.(11), Fig.7, Eq.(24) and Eq.(25) there follows the characteristic value $\hat{I}_{N,\max} = \hat{I}_{N,T,\max}$ for the allowable stress on the module via a solution of the quadratic equation

$$\frac{1}{R_{\mathrm{th},T,\mathrm{j-s}}}(T_{T,\mathrm{j,max}} - T_{\mathrm{s}}) = (\frac{1}{2} - \frac{8}{3\sqrt{3}\pi}\frac{1}{M})R_{DS,\mathrm{on}}\{T_{\mathrm{j,max}}\}\hat{I}^2_{N,\max} + \\ + \frac{2k_{T,\mathrm{P}}\{U_O, T_{\mathrm{j,max}}\}}{\pi} f_{\mathrm{P}}\hat{I}_{N,\max} + \frac{1}{2}C_{\mathrm{oss}}(\frac{U_O}{2})^2 f_{\mathrm{P}} \ . \tag{26}$$

The operating conditions are described there by the heat sink temperature T_{s}, the maximum junction temperature $T_{T,\mathrm{j,max}}$, the switching frequency f_{P}, the voltage transfer ratio M (cf. Fig.7) and the output voltage U_O.

Based on Eq.(26) one can also, e.g., calculate in a simple manner the dependency of the thermally maximum allowable mains current amplitude or the maximum mains power on the heat sink temperature

$$I_{N,\max} = I_{N,\max}\{T_{\mathrm{s}}\}_{f_{\mathrm{P}},M,U_O,T_{\mathrm{j,max}}} \tag{27}$$

(for fixed switching frequency f_P, voltage transfer ratio M, output voltage U_O and junction temperature $T_{\mathrm{j,max}}$). In the same manner, this can be done for the dependency of $\hat{I}_{N,\max}$ on the level of the mains voltage or on the voltage transfer ratio

$$I_{N,\max} = I_{N,\max}\{M\}_{f_{\mathrm{P}},U_O,T_{\mathrm{j,max}},T_{\mathrm{s}}} \tag{28}$$

(for fixed switching frequency, output voltage, junction temperature and heat sink temperature).

If one does not want to determine the mains current amplitude related to a maximum junction temperature but, vice versa, the junction temperature of the power transistor resulting for a given mains current amplitude we have to extend Eq.(26) by analytical approximations of the temperature dependency of the turn-on resistance $R_{DS,\mathrm{on}}$ and of the factor $k_{T,\mathrm{P}}$ determining the switching losses. For the sake of brevity, we have to omit a more detailed discussion of the calculation procedure.

The results of an evaluation of Eq.(26) for the switching frequency region $f_{\mathrm{P}} = 25\,\mathrm{kHz}\ldots 100\,\mathrm{kHz}$ (as interesting for a practical realization of the rectifier system) are shown in **Fig.8**. The calculations are based on the following operational parameters of the system and characteristic values of the power transistor

$$\begin{aligned} T_{T,\mathrm{j,max}} &= 110°\mathrm{C} \\ T_{\mathrm{s}} &= 75°\mathrm{C}\ (P_{T,\max} = 92.1\,\mathrm{W}) \\ U_O &= 700\,\mathrm{V} \\ M &= 1.242\ (U_{N,\mathrm{rms}} = 230\,\mathrm{V}) \\ R_{DS,\mathrm{on}} &= 0.224\,\Omega \\ k_{T,\mathrm{P}} &= 55\,\frac{\mu\mathrm{Ws}}{\mathrm{A}} \\ C_{\mathrm{oss}} &= \approx 1\,\mathrm{nF} \ . \end{aligned}$$

The value $T_{T,\mathrm{j,max}} = 110°\mathrm{C}$ (lying below the maximum allowable junction temperature ($T_{T,\mathrm{j,max}} = 125°\mathrm{C}\ldots 150°\mathrm{C}$) as given in the data sheet) is selected regarding a sufficient safety margin for the calculation which is based on a multitude of approximations and with respect to a high operational safety of the rectifier system (cf. p. 282 in [15]). The value $T_{\mathrm{s}} = 75°\mathrm{C}$ corresponds to a value being usual for dimensioning of an apparatus for a maximum ambient temperature in the region $T_{\mathrm{a}} = 40°\mathrm{C}\ldots 50°\mathrm{C}$.

As **Fig.8** shows, we have to reduce the mains current amplitude and, therefore, the on-state power loss for maintaining the maximum allowable junction

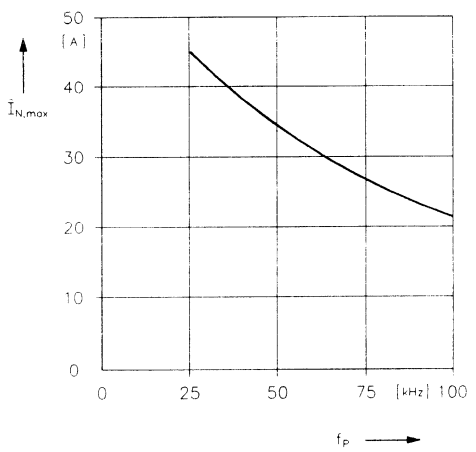


Fig.8: Dependency of the maximum allowable amplitude of the mains current $\hat{I}_{N,\max}$ on the switching frequency f_{P} for application of the power module.

temperature of the thermally critical power transistor for rising switching frequency and for rising switching loss. The curvature of the characteristics can be explained by the quadratic dependency of the on-state losses on the amplitude of the mains current (cf. Eq.(11) and Fig.6). The linear increase of the switching losses for rising switching frequency can, therefore, be compensated by a less than linear decrease of the mains current amplitude.

6 Power Loss Break-Down of the Module

In order to give an overview over the losses resulting for the stationary thermally maximum allowable amplitude $\hat{I}_{N,\max}$ of the mains current (and over the thereby given thermal utilization of the different power semiconductors of the module) **Tab.1** shows the switching and conduction losses and the junction temperatures of the semiconductor elements for characteristic values of the switching frequency. Thereby, a heat sink temperature $T_{\mathrm{s}} = 75°\mathrm{C}$ is assumed. For the thermal resistance of the power diodes according to the data sheet (cf. p. 87 in [5]) $R_{\mathrm{th},D,\mathrm{j-s}} = 1.8\,\frac{\mathrm{K}}{\mathrm{W}}$ is set there. Furthermore, in Tab.1 the total power loss of the module

$$P_M = P_T + 2(P_{D_N} + P_{D_F} + P_{D_M}) \ , \tag{29}$$

the efficiency reduction of the system

$$\Delta\eta_M = \frac{3P_M}{P_N} \tag{30}$$

due to the power loss of the module and the mains power P_N (being approximately equal to the output power) of the system are given.

Based on a maximum allowable junction temperature of the power diodes being higher than $T_{T,\mathrm{j,max}}$ for equal operational safety the original assumption is checked (cf. section 5), namely, that the stationary maximum allowable mains current is determined by the power transistor.

Remark: According to Tab.1 there exist junction temperatures $T_{D_F,\mathrm{j}} \approx 100°\mathrm{C}$ for the free-wheeling diodes. The switching losses of the power transistor being determined essentially by the chip temperature of the free-wheeling diodes have been measured for $T_{D_F,\mathrm{j}} = 110°\mathrm{C}$, however (cf. section 2.4). The factor $k_{T,\mathrm{P}}$ included in Eq.(26) (which almost exclusively determines the maximum allowable mains current amplitude for higher switching frequency) therefore increases the safety margin of the dimensioning. In fact, therefore, for the calculated values $\hat{I}_{N,\max}$ we have to expect a junction temperature of the power transistor lying below $T_{T,\mathrm{j,max}}$.

According to Tab.1 we have for higher switching frequencies due to the higher transistor switching losses a lower value of the thermally maximum allowable mains current amplitude (or the obtainable mains power), and, therefore, a lower utilization of the rated power of the module. Due to the decreasing on-state losses of the diodes for decreasing mains current the total losses of the module drop witch increasing switching frequency (for constant junction temperature and power loss of the power transistor). However, the total losses are still dominated by the transistor losses. Therefore, due to the lower mains power for higher switching frequency a higher efficiency reduction $\Delta\eta_M$ results. If for realization of the rectifier system a high power density (and therefore a high switching frequency $f_{\mathrm{P}} \approx 100\,\mathrm{kHz}$) is required, we

$f_{P,avg}$ [kHz]	25	50	75	100
$\hat{I}_{N,max}$ [A]	45.2	34.2	26.7	21.6
$P_{N,max}$ [kW]	22.1	16.8	13.1	10.6
$P_{T,F}$ [W]	50	29	17	11
$P_{T,P}$ [W]	42	63	75	81
$T_{T,j}$ [°C]	110	110	110	110
$P_{D_N,F}$ [W]	21	15	11	8.7
$P_{D_N,P}$ [W]	–	–	–	–
$T_{D_N,j}$ [°C]	112	102	95	91
$P_{D_F,F}$ [W]	16	11	8.2	6.4
$P_{D_F,P}$ [W]	2.2	3.3	3.8	4.1
$T_{D_F,j}$ [°C]	107	101	97	94
$P_{D_M,F}$ [W]	5.0	4.2	3.1	2.5
$P_{D_M,P}$ [W]	0.7	1.1	1.3	1.4
$T_{D_M,j}$ [°C]	85	84	83	82
$P_{M,F}$ [W]	134	89	62	46
$P_{M,P}$ [W]	48	72	85	92
P_M [W]	182	161	147	138
$\Delta\eta_M$ [%]	2.5	2.9	3.4	3.9

Table 1: Power loss break-down of the semiconductor module, maximum allowable amplitude of the mains current $\hat{I}_{N,max}$ and obtainable mains power of the rectifier system P_N ($U_{N,rms} = 230\,V$, heat sink temperature $T_s = 75°C$) in dependency on the switching frequency f_P. P_M denotes the total loss of one module, $\Delta\eta_M$ the efficiency reduction of the three-phase system caused by $3\,P_M$.

have to tolerate a reduction of the efficiency of about 1% (as compared to $f_P \approx 50\,kHz$ for equal output power) caused by semiconductor losses. The maximum output power of the rectifier system is reduced by $\approx 35\%$ if the switching frequency is increased from 50 kHz to 100 kHz.

7 Efficiency of the Rectifier System for Application of Power Module VUM25-E

Finally, we want to give an estimate for the total efficiency which can be expected for application of the module (especially of interest for application of the rectifier system in a telecom power supply). Also, the distribution of the losses to the components of the system shall be shown graphically. For the switching frequency we choose

$$f_P = 50\,kHz$$

with regard to an always necessary compromise (for a practical realization) between high utilization of the module (high output power) and high efficiency on one side and high power density (high switching frequency) on the other side. With Tab.1 there follows then for the maximum obtainable mains power

$$P_{N,max} = 16.8\,kW\ (\hat{I}_N = 34.2\,A).$$

Besides the losses of the semiconductors of the module (already compiled in Tab.1) we now have to consider for a loss break-down of the whole system

- the resistive losses P_L of the input inductances L, of the EMI filter to be provided on the mains side and of the wiring,
- the losses P_C of the capacitors C_+ and C_- buffering the DC output voltage,
- the power consumption P_E of the gate driver stages, of the control circuit, electro-mechanical control elements (start-up relays etc.) and
- the power consumption P_V of the cooling fans.

The loss contribution P_L is approximately represented by the assumption of an equivalent loss resistor of about 80 mΩ per phase (to be thought inserted into the leads connecting to the mains), giving a total of

$$P_L = 95\,W\ .$$

The core losses of the input inductances L can be neglected in a first approximation for the application of ferrite material. (In the case at hand an inductance of $L \approx 250\,\mu H$ per phase is required for achieving a mains current ripple of $\pm 5\,\%$ of the maximum mains current amplitude.)

For the further loss contributions we set the values known from experience

$$\begin{aligned} P_C &= 15\,W \\ P_E &= 30\,W \\ P_V &= 40\,W\ . \end{aligned}$$

The total efficiency of the rectifier system

$$\eta = \frac{P_O}{P_N} = 1 - \Delta\eta_M - \frac{1}{P_N}(P_L + P_C + P_E + P_V) \qquad (31)$$

then follows as

$$\eta|_{P_{N,max}} \approx 0.96\ .$$

8 Conclusions

In this paper the switching losses and on-state losses of a new power module for realization of a bridge leg of a three-phase/switch/level PWM (VIENNA) rectifier are analyzed. Based on this the maximum output power of the rectifier system is determined (which is limited by the junction temperature of the power transistor) in dependency on the switching frequency. Also the power loss break-down of the module is calculated and the efficiency of the rectifier system is estimated.

The considerations show that a system output power of $\approx 16\,kW$ with a total efficiency of $\eta \approx 96\,\%$ can be achieved for a mains voltage of $400\,V_{rms}$ (line-to-line), a DC output voltage of 700 V, a heat sink temperature of $T_s = 75°C$ and an average switching frequency of $f_P = 50\,kHz$. The module therefore is extremely well suited for the realization of sinusoidal current input stages for telecom power supply systems, for uninterruptable power supplies (UPS), for battery chargers, electronic welding current sources or, in general, power supplies for process technologies.

Concerning the loss break-down of the rectifier system we have to summarize that the total system losses for $f_P = 50\,kHz$ (for maximum output power) are essentially determined by the power semiconductor losses ($\Delta\eta_M \approx 3\,\%$, cf. **Fig.9**). The main part of this loss contribution ($\approx 58\,\%$) is caused by the transistor losses (switching losses $\approx 40\,\%$, on-state losses $\approx 18\,\%$). As a whole the power loss of the module is caused for $f_P = 50\,kHz$ to about equal parts by switching-frequency-dependent ($\approx 55\,\%$) and switching-frequency-independent ($\approx 45\,\%$) losses.

If the switching frequency (e.g., regarding a higher power density of the rectifier system) is increased to $f_P = 100\,kHz$, this loss distribution is shifted noticeable towards the switching losses, and, also, the relative losses of the module are increased as a whole ($\Delta\eta_M \approx 4\,\%$). The part of the switching frequency dependent losses amounts to $\approx 66\,\%$, the part of the switching-frequency-independent losses to $\approx 34\,\%$. The total losses are caused with a part of already 67 % by the losses of the power transistors (switching losses $\approx 59\,\%$, on-state losses $\approx 8\,\%$). The dominance of the switching losses of the transistors shows clearly the importance of minimizing the switching losses via optimizing the gate drive of the power MOSFETs and the optimization of the layout of the PCB used for wiring the power components. An essential

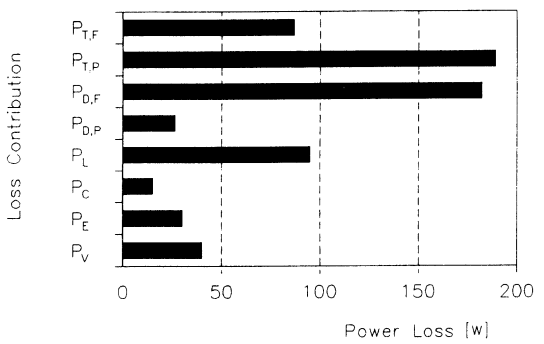


Fig.9: Graphical representation of the loss contributions of the components of a rectifier system realized with the power module IXYS VUM25-E. Operating parameters: $f_P = 50\,kHz$, $U_{N,rms} = 230\,V$, $U_O = 700\,V$, $T_s = 75°C$; $P_O \approx 16\,kW$, $\eta = 0.96$.

increase of the efficiency of the rectifier system can be obtained, however, by changing from hard-switching to soft-switching techniques, or by usage of non-dissipative (active) snubber circuits [20]. A (theoretically) complete avoidance of the switching losses would result for $f_P = 100\,\text{kHz}$ in an overall system efficiency (for maximum output power) of $\eta' = 97.7\,\%$ ($\Delta\eta'_M \approx 1.3\,\%$). For practical realization a total efficiency of $\eta \approx 97\,\%$ seems to be achievable.

Regarding possible further developments of the power module we want to point out that (as Tab.1 shows clearly) the center point diodes D_M have only a low thermal utilization. For a new module generation one could consider, therefore, a reduction of the chip size of D_M. The effect on the total power loss of the module can be neglected in a first approximation, however. A modification of the module should be considered also concerning the diodes D_N. This diodes are presently realized using fast-recovery epitaxial devices; due to the operation principle of the VIENNA rectifier system they are not stressed with switching frequency blocking voltages. Therefore, they could be replaced by conventional rectifier diodes resulting in a lower forward voltage drop (lower on-state losses) and lower cost. This is also valid for the center point diodes D_M. For a simple way of designing a snubber for the power transistor providing a power source terminal would be advantageous. Besides using a RC damping network in this case an over-voltage limiting element could be connected between drain and source of T. The power transistor is designed concerning the blocking voltage capability based on half the value of the output voltage which is typically present for operation of the rectifier system in the European low-voltage mains. A limitation of the (stationary) blocking voltage of the power transistor has to be provided (in order to obtain a high operating safety) because, e.g., for a no-load condition the distribution of U_O among the free-wheeling diodes D_{F+} and D_{F-} and the transistor T is only defined by non-idealities of the devices (leakage currents). As opposed to the blocking voltage stress of the diodes there is no direct limitation (caused by the circuit structure) of the blocking voltage of T to half of the output voltage given. Finally we have to mention however, that during the course of extensive experimental tests of the module such a blocking voltage limitation has been omitted. Despite this fact, no failure of the module has occurred.

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