Contents

Standard IGBT, "G" Series

IGBTs are a class of power semiconductors that combine advantages of MOS gated drive simplicity with the current handling capability of bipolar devices.

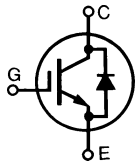
The basic cell design characteristics of the IGBT are very similar to Power MOSFETs. The drive circuitry required to control up to 200 A and 600 to 1200 V is basically the same as a Power MOSFET with 9000 pF of input capacitance.

During turn-on of the IGBT, minority carrier injection into the N-base region modulates the body on-resistance to a level 10 to 20 times lower than an equivalently sized MOSFET, resulting in proportionate 5 to 10 times increase in current handling capability. Minority carrier recombination during turn-off results in a fall time of 0.2-1.0 µs which is similar to bipolar devices. Therefore, the IGBT is more suitable in low to medium frequency, high current, power switching applications ranging from 50 Hz to 80 kHz.

HDMOS™ is a planar, high density process which incorporates new techniques to improve operating characteristics and stability at high voltages. This technology, combined with a unique polysilicon gate cell structure, gives the IGBT a peak current capability of two times its 90°C current rating. This advantage makes the IGBT ideal for many industrial and commercial applications in power conversion and motor control.

The “U1 and D1” family of products feature an IGBT with an ultra-fast diode connected emitter-collector (Fig. 1) to handle the reverse currents that occur in motor controls and other similar applications. Devices rated up to 75 A are encapsulated in the standard TO-220, TO-247 and TO-264 packages while the higher current versions come in the new miniBLOC™ (SOT-227B) package. The many advantages of this package include an electrically isolated mounting base plate, low inductance leads, and reduced collector-to-case capacitance. Either package combination saves space, reduces parts count and assembly costs, and increases reliability and efficiency.

Fig. 1 IGBT with Diode in one package, Co-Pack



The fast recovery epitaxial diodes were designed to provide optimized performance with ultra-fast recovery times and soft recovery behavior. This combination of the IGBT and diode minimizes losses in power conversion and motor control circuits.

Definition of Switching Times and Energies

Fig. 2 shows a typical circuit schematic for testing dynamic parameters such as switching times and energies. Typical current and voltage waveforms are shown in fig. 3 with the definition of the switching times specified in the data sheets. Turn off energy E_{off} is defined as the integral of $i_C \cdot v_{CE}$ within the limits of 10% v_{CE} rise to 90% i_C fall. Normally E_{off} plays the major part of total switching losses. The amount of turn on energy E_{on} depends on the reverse recovery behaviour of the free wheeling diode, so special attention must be paid. If there is a free wheeling diode within the package of the IGBT (Co-Pack), the same type is used for measuring E_{on}, otherwise turn on energy is derived from a resistive test. E_{on} is defined as the integral of $i_C \cdot v_{CE}$ within the limits of 10% i_C rise to 90% v_{CE} fall.
Estimating switching energies other than specified can be easily done by multiplying the datasheet value with the relation of the actual current or voltage to the specified one.
If not otherwise stated IXYS IGBTs are tested with a gate voltage switched from +15 V to 0 V. To reduce switching losses it is recommended to switch off the gate with a negative voltage (-15 V).

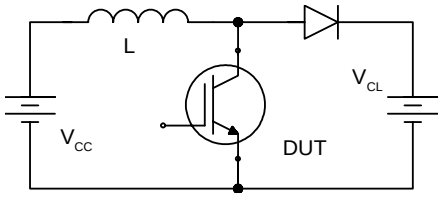


Fig. 2 Switching Time Test Circuit

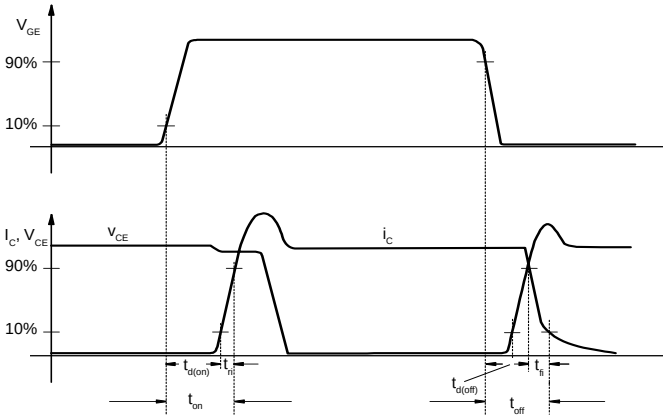


Fig. 3 Definition of Switching Times

What is a HiPerFET™ Power MOSFET?

The HiPerFET™ family of Power MOSFETs is designed to provide superior intrinsic rectifier dv/dt ruggedness while eliminating the need for discrete, fast recovery "freewheeling" diodes in a broad range of power conversion and control applications.

This new class of Power MOSFET uses IXYS' HDMOS II™ process, improving the ruggedness of the FET while reducing the reverse recovery time of the intrinsic rectifier to less than 150 ns to 250 ns. The performance of the intrinsic rectifier is comparable to discrete high voltage fast recovery rectifiers, and is tailored to minimize power dissipation and switching stress in the MOSFET.

HiPerFETs™ offer extended dv/dt ruggedness. These devices have an improved stress withstand capability in applications where the intrinsic rectifier is used as a freewheeling diode. Both static and commutating dv/dt have been improved significantly to typically 60 V/ns and 20 V/ns, respectively. This offers a significant margin of safety in the high stress conditions found in many types of inductive power switching applications.

HDMOS II™ eliminates trade-offs. This fifth generation Power MOS technology has been developed by IXYS, incorporating the ultra-low $R_{DS(on)}$, high unclamped inductive energy capability (UIS), and high transconductance of the original HDMOS™ process. HDMOS II™ now includes proprietary lifetime control, reducing the recovery time (t_{rr}) of the intrinsic rectifier without increasing the on-resistance of the MOSFET. In addition, HDMOS II™ has an improved cell design, improving dv/dt ruggedness.

Figure 1 shows a cross-sectional view of one DMOS cell, one of many thousands that operate in parallel to form a Power MOSFET. The MOSFET is subject to failure if the parasitic NPN transistor turns-on because this dramatic increase in drain current will burn out this MOSFET cell. This failure mechanism is triggered whenever the base-emitter voltage V_B of the NPN exceeds 0.6 V. This can occur in three different ways:

1. High drain current flow due to avalanche voltage breakdown.
2. Base current flow during reapplied forward voltage ($I_B = C_{DG}$ dv/dt).
3. Reverse recovery current after the intrinsic diode has conducted.

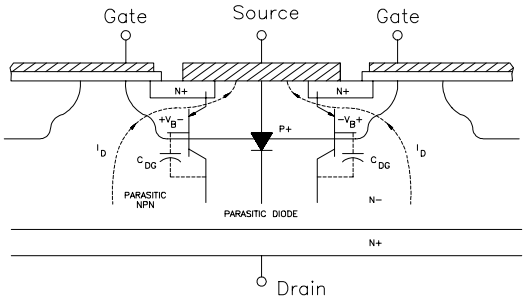


Fig. 1 Cross-sectional view of a Power MOSFET

A HiPerFET™ is an IXYS Power MOSFET with an intrinsic rectifier that has been improved with a proprietary lifetime control process. This process makes several important changes to the MOSFET's operating characteristics:

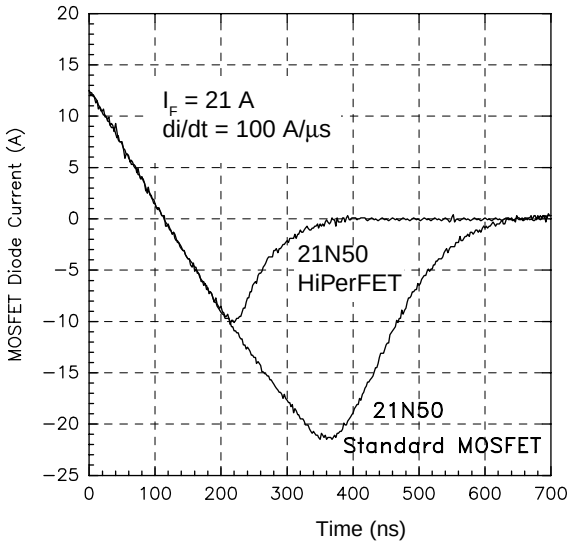


Fig. 2 HiPerFET™ and Standard MOSFET intrinsic diode reverse recovery.

1. The reverse recovery of the internal, intrinsic diode is markedly improved. Diode reverse recovery time t_{rr} is decreased by 60 % or more and reverse recovery current I_{RM} and Q_{rr} are decreased correspondingly. Figure 2 illustrates the dramatic improvement in reverse recovery for a 21 A, 500 V HiPerFET™ commutating off rated diode current at di/dt = 100 A/µs.
2. Intrinsic rectifier **C**ommutating **S**afe **O**perating **A**rea (CSOA), sometimes called commutating dv/dt, is markedly improved.

Commutating Safe Operating Area (CSOA) is a measure of the capability of the transistor to withstand intrinsic diode reverse recovery stresses, which are a combination of the reverse recovery current and C_{DG} dv/dt while the diode regains its reverse blocking capability as the MOSFET is becoming forward biased. HiPerFET™ carry a 5 V/ns commutating dv/dt rating. They are now capable of reliable, efficient operation in a variety of power circuits that Standard MOSFETs alone have never been able to address. These include AC, DC, and brushless motor controls, UPS inverters, welding equipment, resonant power converters and sonar amplifiers.

HiPerFET™ Advantage

In the past, in order to use a Power MOSFET in one of the applications mentioned above, it was necessary to provide an external path for reverse diode currents. As illustrated in Figure 3, this is usually accomplished by blocking the intrinsic rectifier (typically with a series Schottky diode) and placing an external fast recovery rectifier in antiparallel with this series combination of MOSFET and Schottky.

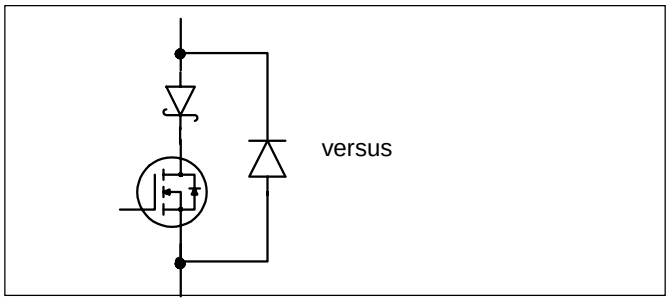


Fig. 3. Reduction in parts count with HiPerFET™

The diode in the HiPerFET™ has been improved to the point that it is rugged, reliable, and efficient enough to eliminate these external components. In a 3-phase motor control, this eliminates twelve power components, their heatsink insulator pads, mounting hardware, and the labor required to mount them. This is a significant cost and parts count reduction, resulting in a reduction in size, weight, assembly labor and cost and in improvement in performance and reliability.

HiPerFET™ Characteristics

Figures 4 and 5 illustrate the typical behavior of the HiPerFET™ intrinsic rectifier under a wide range of operating conditions. This data is taken on the same device shown in Figure 2. Figure 5 shows the dependence of diode t_{rr} and I_R on forward current and temperature. As current increases, more charge injection occurs so that more minority carriers are stored in the parasitic NPN collector region. This increases t_{rr} and I_R. At higher temperatures, the junction injection efficiency increases so again more carriers are stored in the collector with the same result as before.

Avalanche Voltage Testing

A well known, standard industrial test for ruggedness is avalanche voltage testing, also known as **U**nclamped **I**nductive **S**witching (UIS) testing. The test circuit is shown in Figure 6. Peak test current is normally set at the 25°C DC current rating of the D.U.T. and the D.U.T. is checked electrically after the test to ensure that no degradation occurred during the test. This test guarantees that the HiPerFET™ will survive voltage transients that may be in excess of its repetitive collector-drain voltage rating due to some abnormal switching condition, (e.g.. open circuit or short circuit operation, lightening or load bank switching, etc.).

Design and Handling Considerations

MOSFET Switching Speeds: Device Switching speeds are dependent on the drive circuit impedance. By driving the gate from a low impedance voltage source, extremely fast switching speeds can be attained. Turn-on and turn-off times are essentially independent of device temperature.

Intrinsic Diode Switching Speed: Intrinsic rectifier t_{rr}, Q_R, and I_R are strong functions of diode operating temperature and power circuit operating conditions, including turn-off di/dt, gate drive impedance, and stay source inductance.

Gate Voltage Ratings: It is important not to exceed the gate voltage ratings V_{GSS} (continuous) and V_{GSM} (transient). Exceeding V_{GSM} poses an immediate risk of permanent damage to the gate oxide layer on the MOSFET chip.

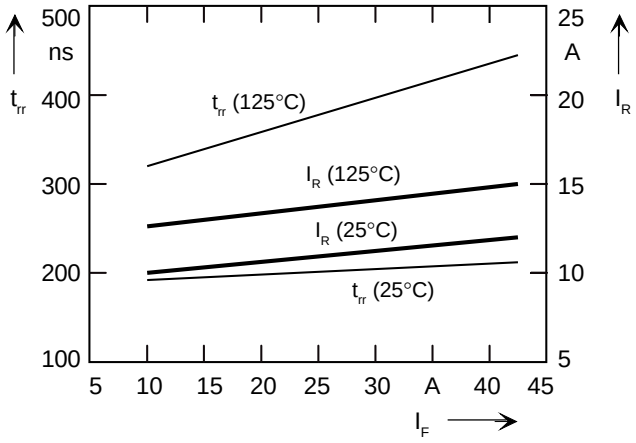


Fig. 4. Dependence of t_{rr} and I_R on diode current I_F

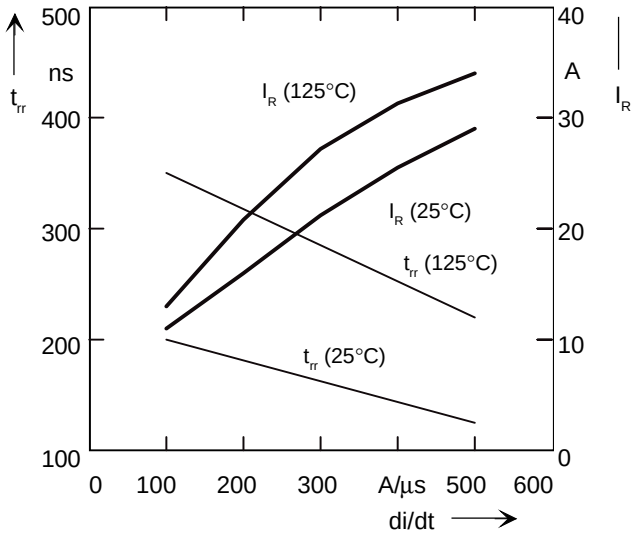


Fig. 5 t_{rr} and I_R vs. commutation di/dt

Gate Termination: Because the gate is essentially a capacitor, circuits that leave the gate open-circuit or floating can result in unwanted turn-on of the device or gate overvoltage damage. Voltage buildup on the input capacitance can occur from device or PC board leakage currents or capacitive coupling from the drain or other circuit nodes. If gate drive impedance is high, it is frequently advisable to add an external Zener diode from gate to source to protect the device.

Gate protection and ESD: IXYS HiPerFETs™ do not have an internal Zener diode from Gate to Source, and are subject to damage from static discharge. Reasonable precautions in handling and packaging, similar to those required for MOS ICs, must be employed.

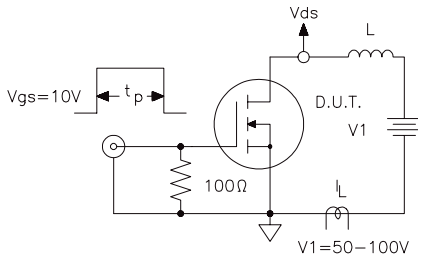


Fig. 6 UIS test circuit

New 1600V BIMOSFET™ Transistors Open Up New Applications

by
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Introduction

There are many applications today using high voltage MOSFETs and IGBTs, which would benefit from a higher voltage part. Examples are sweep circuits, radar pulse modulators, capacitor discharge circuits, solid state relays, auxiliary power supplies on traction equipment and other high voltage switch mode power supplies. MOSFETs are connected in series-parallel strings to overcome their voltage and high $R_{DS(on)}$ limitations. High voltage IGBTs are too slow for some applications. A new family of high voltage BIMOSFET™ transistors is fulfilling these needs.

The conventional construction for both MOSFETs and IGBTs is commonly referred to as DMOS (double-diffused-metal-oxide-silicon), which consists of a layer of epitaxial silicon grown on top of a thick, low resistivity silicon substrate, as shown in Fig. 1b. However, at voltages in excess of 1200V, the thickness of the N- silicon layer required to support these blocking voltages makes it more attractive and less costly to use a non-epitaxial construction as illustrated in Fig. 1a. This type of construction is also known as "homogeneous base" or "non-punch through" (NPT).

Referring to Figure 1a, the typical pnpn-structure for the IGBT has been maintained, but note that an N+ collector-short pattern has been introduced in order to reduce the current gain of the PNP transistor and consequently its turn-off switching behavior. However, now there is a "free" intrinsic diode from emitter to collector , not unlike that found in a MOSFET, which led us to coin the acronym 'BIMOSFET™ transistor.' The turn-off behavior of the BIMOSFET™ transistor is controlled by the amount of collector shorting. In order for the diode to be usable and not cause commutating dV/dt problems, the lifetime of the minority carriers must be reduced by irradiation. The end result is a device, which can be optimized for either high frequency or low frequency switching by tailoring its collector short pattern along with suitable amounts of ir-

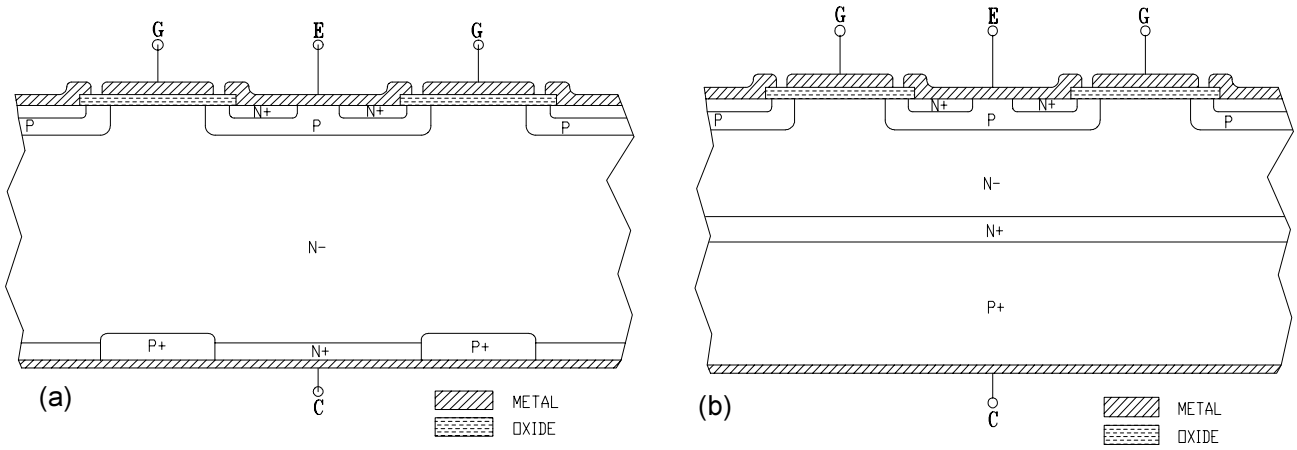


Figure 1. Comparison of the BIMOSFETTMIXBH40N160 cross-section (a) to an IGBT with epitaxial construction (b).

Table 1: Comparative Electrical Performance

Parameter	IXBH40N160	IXLH45N160
DC Parameters (Tj = 25C)		
BVces	1600V	1600V
Vge(th)	5-9V	5-9V
Vce(sat) @ Ic = 25A	7V	2.5V
Qg(on)	121nC	108nC
Ic(on) @ Vge = 15V	110A	100A
Switching (Tj = 125C)		
Turn-on (Note 1)		
td(on)	50ns	50ns
tri	195ns	168ns
E(on)	0.78mJ	0.66mJ
Turn-off (Note 2)		
trv	195ns	335ns
tfi	240ns	1980ns
E(off)	3.0mJ	29mJ

Notes: 1. Turn-on test conditions: V_C = 960V; I_C = 30A; R_G = 2.7Ω; Resistive load
2. Turn-off test conditions: V_C = 1440V; I_C = 25A; R_G = 22Ω; Inductive load

radiation.

Since there are many applications in which the electrical characteristics of the intrinsic diode are not optimum for the application, e.g. high on-voltage or reverse recovery current or too high power dissipation, a modified fabrication process has been developed to block the intrinsic diode without impacting the effectiveness of the collector shorts. The first member of the family with the diode blocked is the 1600V rated IXLH45N160 BIMOSFET™ transistor intended for high current applications with low repetition rates. This part has a much lower saturation voltage (3.5V at I_c = 30A) because it is not irradiated. Its switching speed is controlled by the amount of collector shorting; more shorting results in higher saturation voltages due to loss of conducting area but faster switching performance.

DC Electrical Performance

It is foreseen that the BIMOSFET™ transistor family will span the range of high voltage applications, from a simple high voltage switch to increasing the upper frequency performance of high voltage IGBTs. Table 1 offers a comparison of their electrical performances.

In examining this table and some of the figures below, we can note the following:

1. The typical threshold voltage of the BIMOSFET™ transistor family is higher than normal IGBTs but its $Q_{g(on)}$ is comparable. This

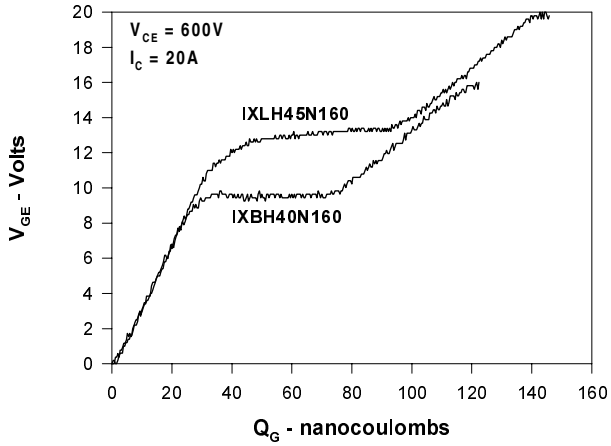


Figure 2a: Gate charge

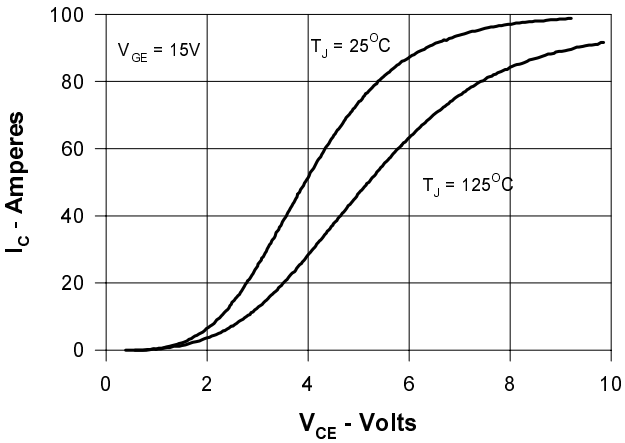


Figure 3a: $V_{CE(sat)}$ of the IXLH45N160 showing the effect of increasing T_J.

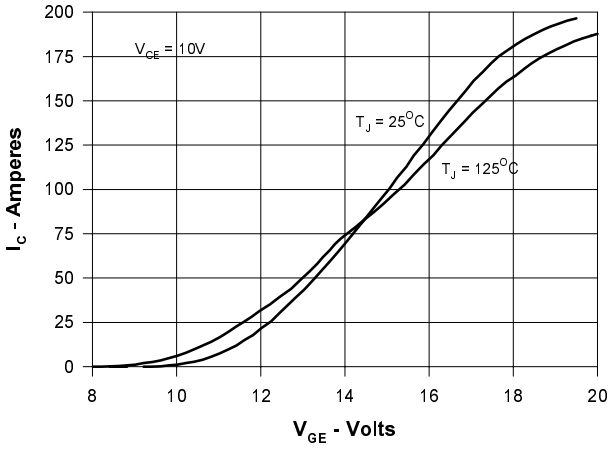


Figure 2b: IXLH45N160 output current vs. gate-emitter voltage

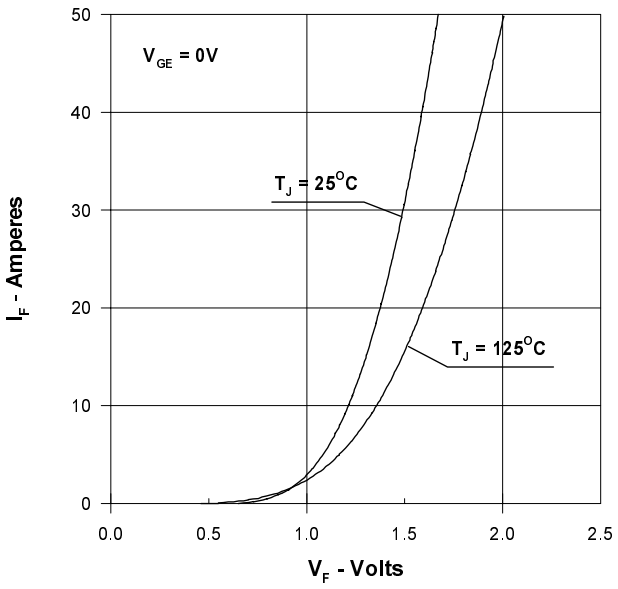


Figure 3b. Forward voltage drop of the IXBH40N160 intrinsic diode.

is due to its relatively low Miller gate capacitance resulting in low Miller gate charge as can be seen in Figure 2a. In one sense, a high threshold voltage can be considered as an advantage in electrically noisy environments. The low $V_{CE(sat)}$ version also has a 2V higher $V_{GE(on)}$. Figure 2b plots its transconductance at room and elevated temperatures and shows that the output current vs. V_{GE} is relatively independent of temperature.

2. The $V_{CE(sat)}$ of the IXLH45N160 is almost one-third of the IXBH40N160, 2.5V and 7.0V respectively at I_C = 25A. The saturation voltage of both parts has a strong, positive temperature coefficient as evidenced in Fig. 3a, depicting the $V_{CE(sat)}$ curves for the IXLH45N160. Fig. 3b plots the diode voltage drop of the IXBH40N160 and shows that it too has a positive tempco. Consequently it is easier to operate BIMOSFET™ transistors in parallel than either DMOS IGBTs or MOSFETs.

3. In order to survive short circuit testing (SCSOA) at higher voltages, low transconductance, yielding low short circuit current $I_{CE(on)}$ is required. So with $I_{CE(on)}$ values in the order of 100A, the BIMOSFET™ transistors can be used in applications where survivability to this type of fault is a must.

4. However in many pulse applications, the capability to conduct high peak currents is more

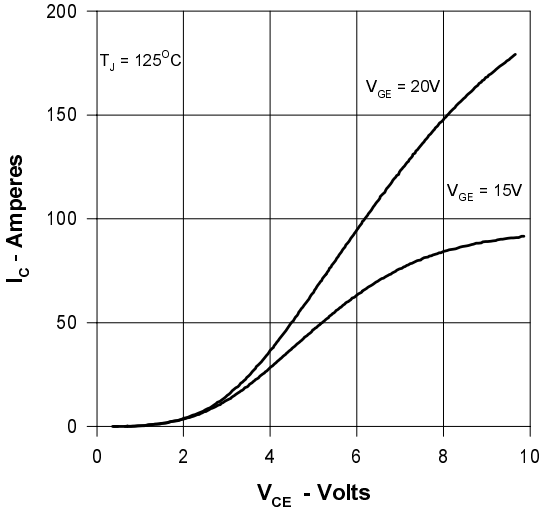


Figure 4. Saturation voltage curve for the IXBH45N160. Note increased output current capability and lower $V_{CE(sat)}$ voltage with 20V gate drive.

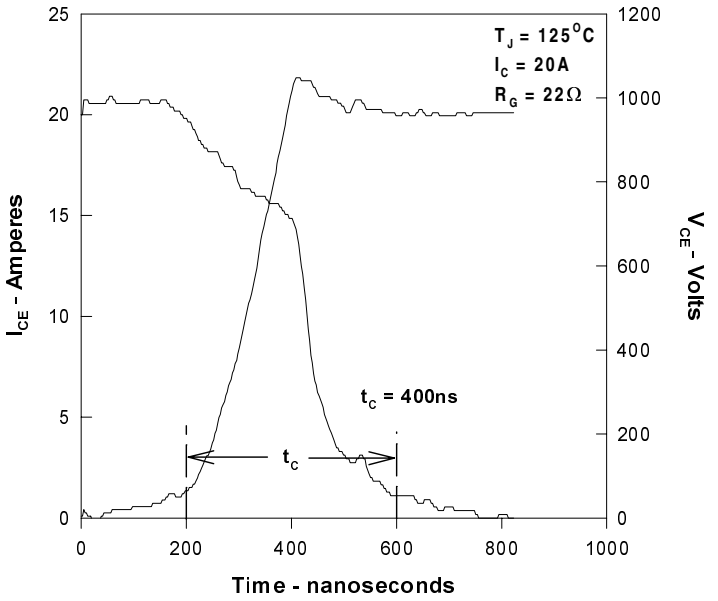


Figure 5. Turn-off current and voltage waveforms of the IXBH40N160.

important than SCSOA. One way to overcome low transconductance is to increase gate voltage. Figure 4 shows that $I_{C(on)}$ almost doubles from 100A to over 200A as V_{GE} is increased from 15V to 20V, while gate charge only increases by 20nC. This is easily done using either discrete MOSFETs or bipolar transistors in the gating circuit or by using commercially available IC drivers, such as the Telcom TC4431 or TC4432 MOSFET drivers.

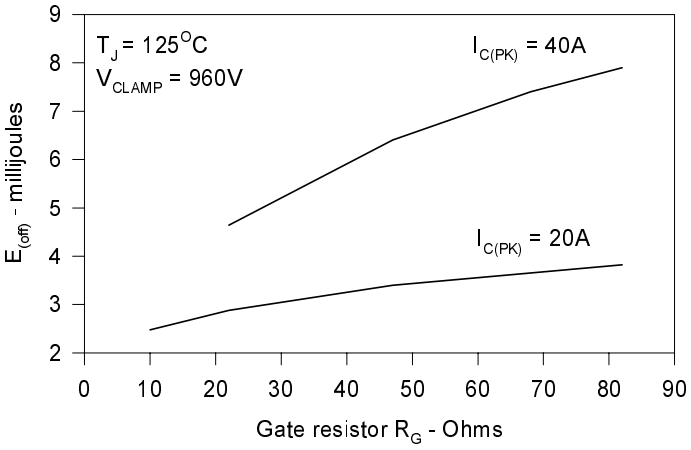


Figure 6. Turn-off energy versus gate resistor R_G for the IXBH40N160.

Switching Performance Comparison

Both BIMOSFET™ transistors switch exceptionally fast for 1600V rated parts. The resistive turn-on time of the IXLH45N160 with a 2.7Ω gate resistor is typically 168ns, which edges out the IXBH40N160 (t_{ri} = 195ns) because the latter is irradiated. But Figure 5, illustrating the IXBH40N160 turning off a 20A inductive load into a 1000V clamp at the elevated temperature of 125°C, shows where it shines. There is relatively little tail current so that the $E_{(off)}$ is 2.4mJ, which is 50% less than a comparable IGBT. Figure 6 plots its turn-off energy as a function of the series gate resistor R_G. This resistor primarily determines the rate-of-rise of collec-

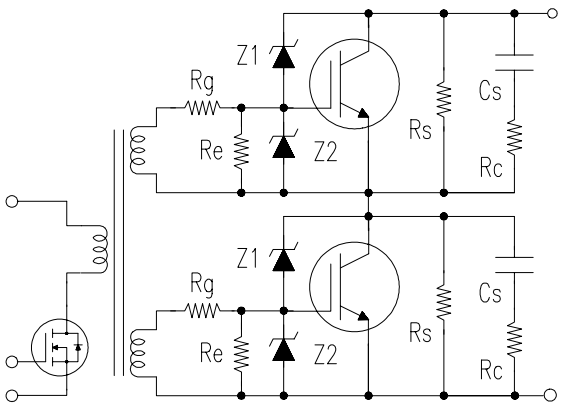


Figure 7. Series connection

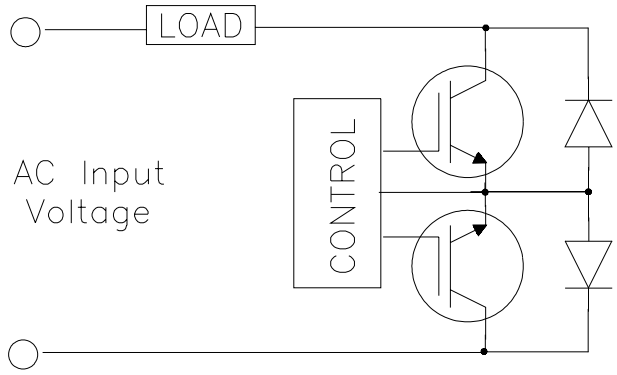


Figure 8a: Bi-directional AC switch.

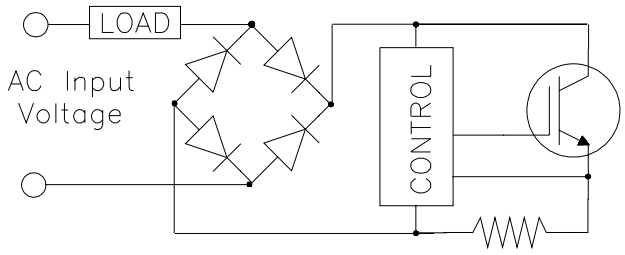


Figure 8b: AC current control using diode bridge.

tor voltage, which increases as R_G decreases and correspondingly $E_{(off)}$ decreases. The low $V_{CE(sat)}$ IXLH45N160 has a much longer tail current, which is only marginally affected by R_G. Consequently its operating frequency range is less than 5kHz.

Applications

Some of the many applications have already been mentioned but let us a review a few to see the advantages of the availability of high voltage switches.

One fast growing type of application is capacitor discharge circuits, such as found in laser power supplies, defibrillators, spot welders and similar circuits. The use of high voltage is an advantage because energy stored in a capacitor is proportional to voltage squared and fast current rise times are easier to achieve. Figure 7 shows a typical circuit using two IGBTs in a series string. Note the necessity of the following duplicate components:

1. Static voltage sharing resistors R_S due to unequal leakage currents of the two switches;
2. Dynamic voltage sharing capacitors C_S to compensate for differences in turn-on and turn-off times;
3. Resitor R_C may also be required to dampen voltage ringing or to limit capacitor in-rush current at turn-on;
4. Zener diodes Z1 to protect the IGBTs against overvoltage transients;
5. Duplicate gating circuit components R_G, Z2 and R_E.

Eight of these components can be eliminated when using only one high voltage switch! In addition, the pulse transformer is easier to wind since now there is only one secondary winding.

When one switch does not have the current handling capability, semiconductor switches are used in parallel. While both MOSFETs and IGBTs are used in parallel, both require matching to achieve satisfactory operation. The

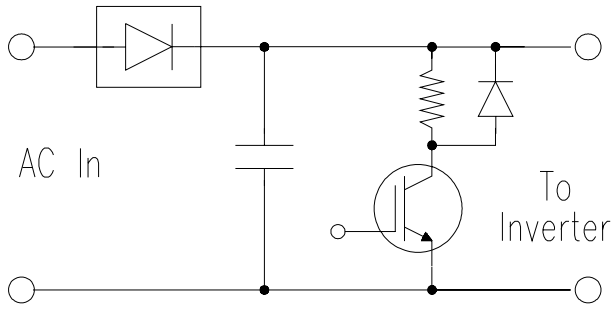


Figure 9a: Dynamic break configuration.

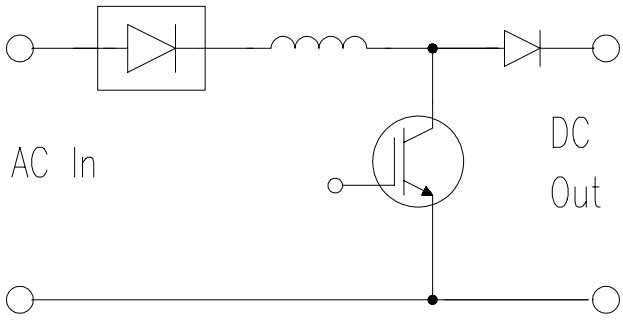


Figure 9b: Boost configuration.

BIMOSFET™ transistor family facilitates paralleling due to its positive voltage temperature coefficient of both its saturation voltage and forward voltage drop of the intrinsic diode as shown in Figure 3b..

A traditional usage of thyristors is in AC solid state switches. Two possible circuits are shown in Figures 8a and 8b. Figure 8a shows the connection diagram for two IXLH45N160 BIMOSFET™ transistors and two high voltage diodes while Figure 8b circuit uses one BIMOSFET™ transistor inside a full-wave bridge. Both circuits can be used on AC mains up to 600V(RMS) and both also provide the additional functions of precise current control and overcurrent protection. The circuit in Figure 8a can carry more current because the current is shared by the two BIMOSFET™ transistors and will be more efficient because current only flows through one diode. The circuit in Figure 8b will cost less because there is only one BIMOSFET™ transistor.

Finally Figures 9a and 9b show the usage of the BIMOSFET™ transistors in two rapidly growing applications, namely AC motor control featuring dynamic braking and boost inverters. Again due to the high voltage and fast switching capability of the IXBH40N160, one can now design these circuits to operate up to 600V(RMS) or produce output DC voltages up to 1200V.

Just as it is anticipated that the applications for BIMOSFET™ transistors will proliferate, IXYS will continue to grow the BIMOSFET™ transistor family by the additions of both higher and lower current devices with a range of switching speeds to meet the requirements of the power conversion market.

(Acknowledgement: The author wishes to recognize and thank his co-workers, Messrs. M. Arnold, T. Jankovic, A. Lindemann and O. Zschieschang, for their contributions and suggestions to make this article possible.)

Technical Application

Comparative Performance of BIMOSFETs in Fly-Back Converter Circuits

One of the typical applications for a flyback converter is the auxiliary power supply for the IGBT gate driver in an inverter. The essential requirement for a switch of a flyback converter in a drives inverter is a high breakdown voltage combined with fast switching speed. To minimize the predominant switching losses, the switch-on and -off energies have to be low. The main advantage of the BIMOSFET lies first in its lower turn- on losses and secondarily in its lower conduction losses. A comparison of the total energy losses between a MOSFET and a BIMOSFET results in ***35 % less total losses*** *for the BIMOSFET.*

Flyback Operation

The Flyback Converter is one of the most simple converter types. The minimum configuration consists of only a switch, a transformer, a diode and two capacitors as shown in fig. 1. The

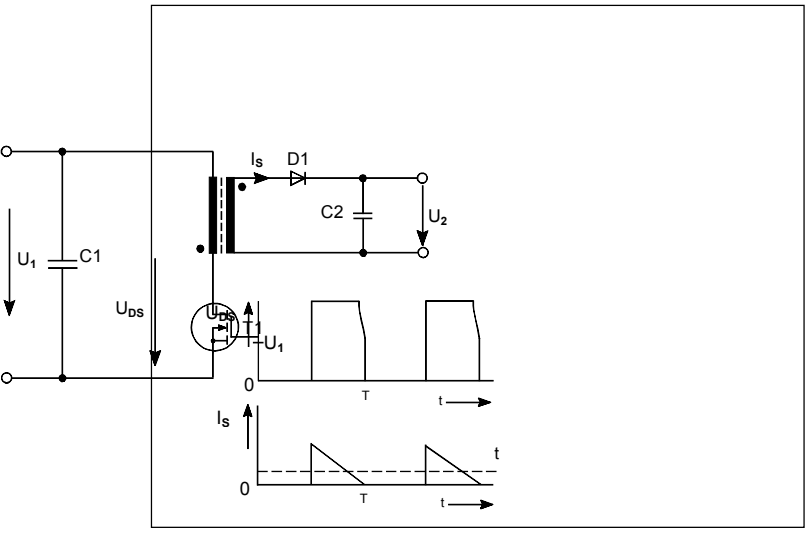


Figure 1: flyback

energy in this converter type is stored in the air gap of the ferrite core. Primary current ramps up during the on state of the switch storing magnetic energy, which is then transferred to the output by the diodes when the switch turns off. The power range for this converter type is limited to approximately 300 W.

The advantages of this circuit are the very wide input-output voltage ratio and the feasibility of adding more secondary windings to create multiple output voltages. Furthermore, it is advantageous to have galvanic insulation between primary and secondary side. The disadvantages are the high breakdown voltage required for the switch and the RFI emission generated by the air gap in the transformer. The flyback converter can not work without load or closed regulation loop as otherwise the output voltage will exceed allowable limits.

Flyback Application

One of the typical applications for a flyback converter is the auxiliary power supply for the IGBT gate driver in an inverter. This application has all the requirements, which can be fulfilled ideally by a flyback converter.

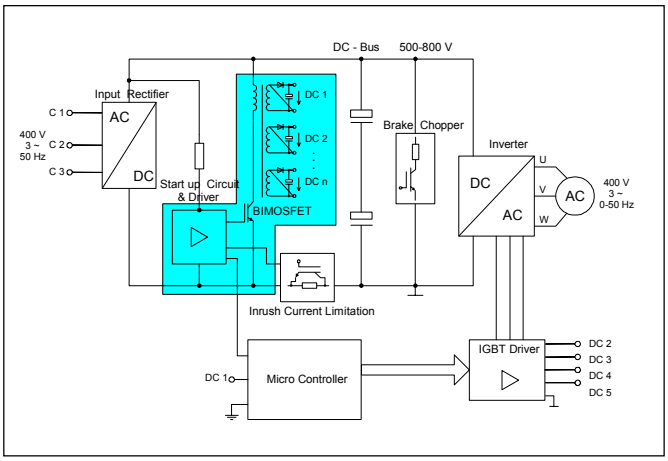


Figure 2: inverter

The shaded area in fig. 2 shows a converter with the start-up circuit as part of the drives inverter. The auxiliary power supply can be built very cost effectively with relatively few elements.

Since the input voltage for the converter is the DC-power bus, there is a wide voltage variation. During the precharge of the bus capacitors, the power supply has to work properly with very low DC-bus voltages, as well as under braking operation of the motor, when the bus voltage reaches high values up to 750 V. The output voltage can easily be regulated by varying the transistor duty cycle.

All the insulated DC- outputs can be generated by adding more separated secondary windings. For example the 5 V supply for the micro controller, ± 15 V for current sensors, a common +15V supply for the driver of the three lower IGBTs and three separate +15V supplies for the upper IGBT drivers.

Requirements for the Switch

The essential requirement for a switch of a flyback converter in a drives inverter is a high breakdown voltage. In a flyback converter the maximum voltage applied to the switch is approximately two x the input voltage. Therefore, the minimum breakdown voltage must be higher than 2 x Vin. For standard inverters for motor control used off mains of 400 V, the DC-bus voltage can reach up to 750 V in the motor braking mode of operation. Here a breakdown voltage of at least 1600 V is needed.

Flyback converters normally run with switching frequencies between 50 to 100 kHz. To minimize the predominant switching losses the switch-on and -off energies have to be low. To achieve this, a high switching speed by the switch is obvious. A common trick to avoid switch-on losses in a fly back topology is not to turn on the transistor until the current in the output diode has reached zero (discontinuous mode). There must be a deadtime until the next cycle starts. The advantage here is less transistor and diode commutation losses, which allows higher switching frequency in order to reduce the size of the transformer.

BIMOSFET™ Chip Technology

Standard high voltage IGBTs are too slow for flyback applications. The new family of high voltage BIMOSFET transistors is fulfilling these needs.

The conventional construction for both MOSFETs and IGBTs is commonly referred to as DMOS (double-diffused-metal-oxide-silicon), which consists of a layer of epitaxial silicon grown on top of a thick, low resistivity silicon substrate, as shown in Fig. 3a.

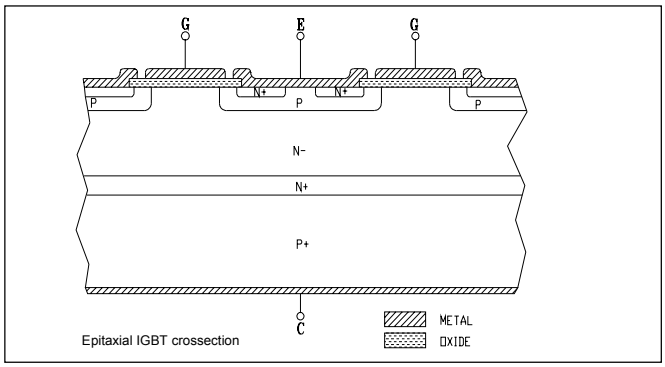


Figure 3a: Cross section

However, at voltages in excess of 1200 V, the thickness of the N-silicon layer required to suppport these blocking voltages makes it more attractive and less costly to use a non-epitaxial construction as illustrated in Fig. 3b. This type of construction is also known as “homogeneous base” or “**N**on **P**unch **T**hrough” (NPT).

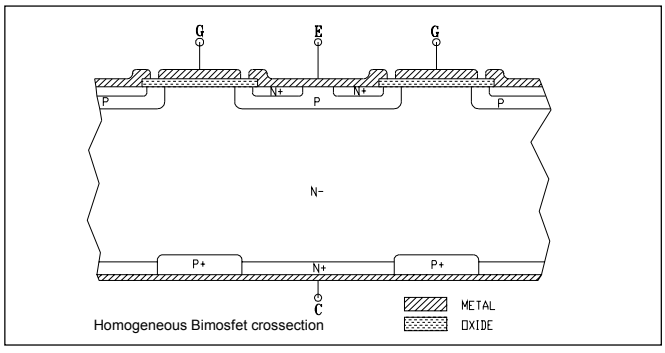


Figure 3b: Cross section

Referring to Fig. 3b, the typical pnpn structure for the IGBT has been maintained, but note that an N+ collector- short pattern has been introduced in order to reduce the current gain of the PNP transistor and consequently its turn-off switching behavior. However, now there is a “free” intrinsic diode from emitter to collector, not unlike that found in a MOSFET, which led us to coin the acronym BIMOSFET transistor. The turn-off behavior of the BIMOSFET transistor is controlled by the amount of collector shorting. In order for the diode to be usable and not cause commutating dV/dt problems, the lifetime of the minority carriers must be reduced by irradiation. The end result is a device, which can be optimized for either high frequency or low frequency switching by tailoring its collector short pattern along with suitable amounts of irradiation.

Driver requirements

Our tests have shown there is a significant influence on the losses by gate resistor and gate voltage. As a rule, we have found that a series gate resistor of less than 30 Ω has a tendency to oscillate while switching above 50 W increases mainly the turn-on losses. Therefore, the IXBH 9N160 BIMOSFET operates best at **15 V’s gate drive** and by using a **gate resistor** between **30 and 50** Ω. To achieve full conduction, a gate drive of 15 V is necessary, because the threshold voltage of 6 V is relatively high compared to MOSFETs.

Static behavior

When comparing the output curves we can see the linear characteristic for the MOSFET (fig.4a) and the bipolar behavior for the BIMOSFET (fig.4b).

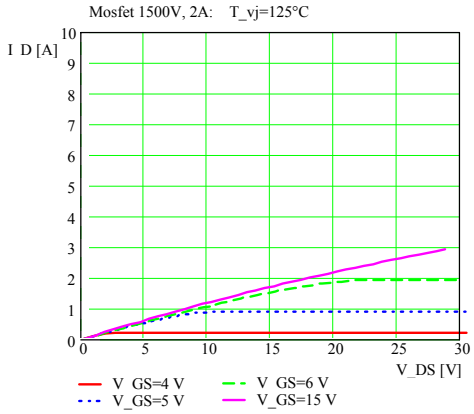


Figure 4a: output characteristics

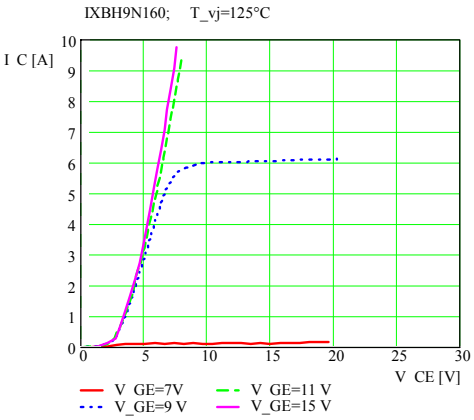


Figure 4b: output characteristics

As can be seen from figure 4a, the MOSFET can conduct 2 A with only 6 V gate drive. Comparing this to the BIMOSFET output characteristic in fig. 4b, one sees that there is no current flow with 7 V gate drive. Here lies the major difference for the BIMOSFET. We need at least 11 V to switch on properly at currents below 5 A. For higher peak currents, we need 15 V gate voltage for proper conduction. There is a significant difference in the on-state losses. At 2 A and 15 V gate drive, the MOSFET has a voltage drop of 18 V and the BIMOSFET has only 4 volt drop. This leads to 4.5 times less conduction losses. We also can see the much higher current capability of the BIMOSFET, which can easily conduct more than 10 A compared to the MOSFET, which is limited to 3 A.

Switching behavior

We have done several comparative measurements to quantify the performance of a standard high voltage MOSFET and the BIMOSFET. The figures 5a and 5b show a full switching cycle and allow the calculation of the total losses. The parameters drain current, drain voltage and gate voltage have been measured. The power dissipation and the total energy have been calculated from these data.

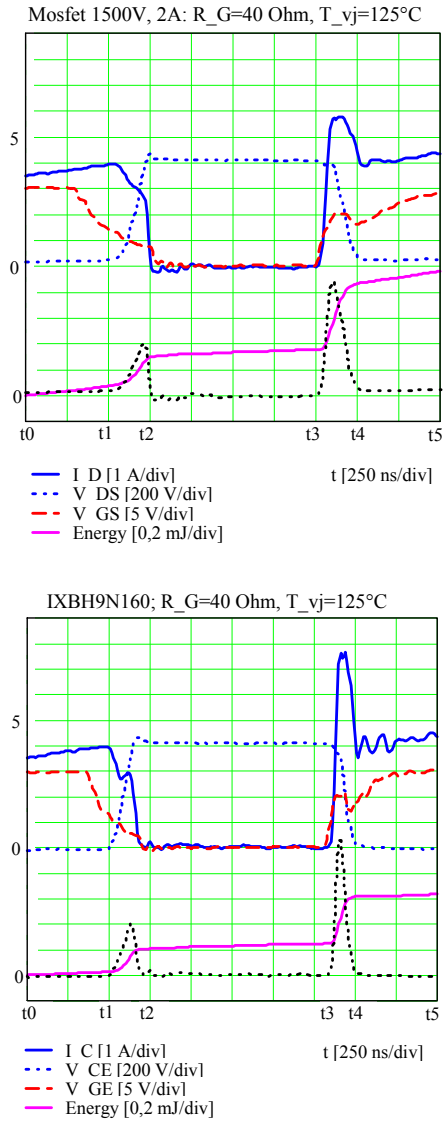


Figure 5: switching curves

The test equipment was a double pulse tester, in which the freewheeling diode is still conducting when the MOSFET is switched on. Consequently, the turn-on waveform is impacted by the diode's recovery behavior. However, the performance is comparable because the diode's influence on the MOSFET or BIMOSFET is the same.

The conditions are as follows:
Turn-off current amplitude = 4 A
Voltage = 800 V
Gate drive = 15 V, 40 Ω
Junction temperature = 125°C

The time from t0 to t1 is the end of the conduction phase. At the end of this phase we can see a rise in the energy curve (solid line below), which is caused by the higher on state losses of the MOSFET.

The next step (t1 to t2) is the turn-off. The dotted line (Ptot) below shows no significant difference in turn-off losses although they might be slightly less for the BIMOSFET.
After turn- off (t2 to t3), there is no visible tail current for the BIMOSFET. The slight increase in energy that we can see during the off-state might be a measurement error, since we have the same for the MOSFET, which definitely has no tail current.

The next phase is turn-on from t3 to t4. We easily can see that the major losses occur during turn-on. The upper solid line shows a high peak current, which is mainly caused by commutation of the diode. In comparison, the turn-on time for the MOSFET is longer than for the BIMOSFET. The peak power for the MOSFET is approximately 4 kW for 250 ns. The peak power for the BIMOSFET is 5 kW but only for a duration of 130 ns. Therefore, the total switch on energy for the MOSFET is 0.5 mJ and only 0.4 mJ for the BIMOSFET. This is 20% less for the BIMOSFET.

The last 500 ns, from t4 to t5, are the beginning of the conduction phase. The energy curve for the MOSFET shows a rise caused by the high on resistance. The BIMOSFET curve is almost flat, which is a sign for a low saturation voltage (compare fig.4b).

Product range

Type	BV_{CES} min. V	V_{CEsat} @ 25°C max. V	I_{C25} A	E_{off} @125°C typ. mJ	E_{on} @125°C typ. mJ
IXBH 9N160 **IXBH 9N140**	1600 1400	7.0	9	0.4	0.56
IXBH 15N160 **IXBH 15N140**	1600 1400	7.0	15	0.72	1.0
IXBH 20N160 **IXBH 20N140**	1600 1400	6.5	20	1.04	1.52
IXBH 40N160 **IXBH 40N140**	1600 1400	7.0	33	1.52	2.15

In summary

The main advantage of the BIMOSFET lies first in its lower turn- on losses and secondarily in its lower conduction losses. The total energy loss per pulse is shown at time t5 where we see that the MOSFET value is 0.95 mJ and for the BIMOSFET, only 0.62 mJ. This results in **35 % less total losses** for the BIMOSFET.

Reliability

General

Power semiconductors used in high power electronic equipment are exposed to different conditions compared to plastic encapsulated components applied in equipment used for communication electronics. Controlling and converting of high power simultaneously requires reliable control of both high voltage and high current. Control of electrical drives additionally results in frequent repetition of switch-on and switch-off processes that must meet special demands with respect to the internal mechanical design. While low electrical losses occur in components applied for communication electronics these can be in the order of 100 W in high power silicon semiconductor components. These really considerable losses existing during the entire operation time of a converter equipment must be dissipated to the environment by cooling surfaces. The semiconductors must be designed in the interior such as to withstand the continuously arising temperature gradients resulting from the losses. Finally, the safe electrical isolation of the electrical circuits in modules must be ensured.

Reliability, Life

According to the international standards the term quality is defined as totality of characteristics of an entity that bear on its ability to satisfy stated and implied needs. In this case entity is the power semiconductor. Reliability is the property of the semiconductor to maintain all its functions during usage. Since it is not possible to determine the long range reliability of power semiconductor components prior to production release under realistic conditions accelerated life tests must be applied which allow reliable results about the reliability of the components after a short test period. To achieve an acceleration effect the reliability tests are carried out under greater stress than in application.
According to the familiar failure rate curve (bathtub curve) we distinguish between early failures, random failures (failures with constant failure rate) and failures resulting from wear-out and fatigue.
While applying a so-called “burn-in” for integrated circuits to catch early failures prior to the final application in the equipment this does not make sense for power semiconductors because of substantial higher costs.
Provided there is no misapplication caused by the user early failures must be avoided by complete control and mastery of the manufacturing processes.
Excluding short time overload during operation random failures are determined by reproducibility and safety margins of the manufacturing parameters.
The early design phase of a product already decides about failures caused by wear-out and fatigue designing parts and processes and selecting the material.

Failure Rate, Reliability Prediction

It is difficult to find a distribution function which will allow the whole bathtub curve. However, for each section of it the Weibull distribution is applicable.

$$F(t) = 1 - \exp (- t / T)^b$$

F(t) : probability that the device fails in the interval [0,t]
T : characteristic life
b : shape parameter
t : time; number of cycles

From this equation follows the failure rate (hazard function):

$$\lambda(t) = (b / T^b) * t^{b-1}$$

The shape parameter means:

b = 1	constant failure rate	->	random failures
b < 1	decreasing failure rate	->	early failures
b > 1	increasing failure rate	->	wear-out, fatigue

a) Random failures

In terms of electrical failures usually the shape parameter b = 1 is applicable. This particular Weibull distribution then is called Exponential distribution

$$F(t) = 1 - \exp (-\lambda * t)$$

where $\lambda = 1 / MTTF$ the constant failure rate.

Failure rate often is estimated by experiment using the formula

$$\lambda = r / (n * t)$$

r : number of failures
n : sample size
t : test time
MTTF : Mean Time To Failures, time in which 62.3 % of devices failed

Because of statistical nature of this number an extended formula taking into account a confidence limit (Upper Confidence Limit [UCL] = 60 % is the common value) is used.
Moreover, it is possible to calculate reliability data by computer models. The available computer models, however, have not been developed for power semiconductors. The failure rate model according to MIL-HDBK 217 serves therefore for the time being only as rough estimate.

$$\lambda [FIT] = [(r + \Delta r) / (n * t)] * 10^9$$

Δr : depending on confidence limit and number of failures
FIT : Failures In Time, failures / 10^9 device hours

Constant failure rates allow reliability prediction by using an acceleration factor. This acceleration factor is calculated by means of the Arrhenius equation:

$$af = \exp \{ Ea * [T_2 - T_1 / (T_1 * T_2)] / k \}$$

Ea: activation energy Ea = 1eV @ HTRB, Ea = 0.4 eV @ HTGB
k : Boltzmann's constant k = 8.6 * 10^{-5} eV/K
T_1 : absolute application junction Temperature [K]
T_2 : absolute test junction Temperature [K]

Fig. 1 shows the acceleration factors (T_2 = 398 K [125°C]).

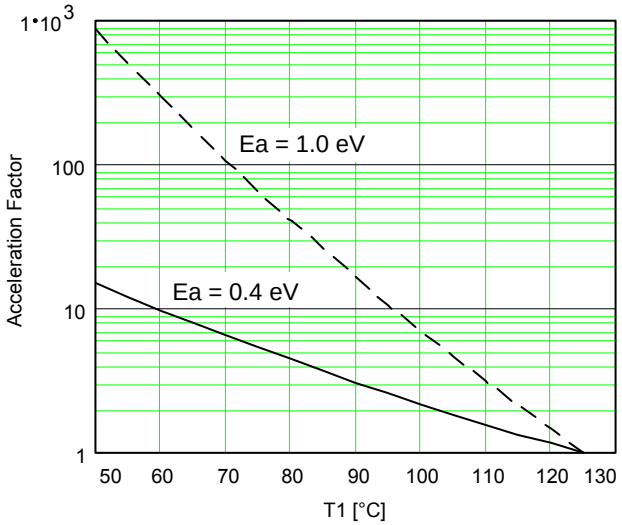


Fig. 1 Acceleration Factor

The above mentioned acceleration factor is applicable at constant temperatures mainly for HTRB and HTGB. In case of temperature differences (temperature cycle, power cycle) other formulas have to be used.
To estimate life times for different ΔT frequently the Manson-Coffin relation is used which has been established originally for metals under plasic stress [2]. If plastic strain dominates, then

$$N_f \approx 1 / (\Delta T)^2$$

Nf : number of cycles to failure
ΔT : temperature difference

An extended formula is known from literature to incorporate cycle period and maximum junction temperature [2]:

$$N_L / N_A = (f_L / f_A)^{1/3} * (\Delta T_A / \Delta T_L)^2 * \Phi(T_{max})$$

L : laboratory test
A: field application
f : cycle frequency
$\Phi(T_{max})$ ~ 1, if $T_{Amax} = T_{Lmax}$

b) Early Failures

Constant failure rate allows simple computation and prediction of life. In the regime of early failures prediction of failure rate is not practible. The failure rate is strongly time dependent.
For example an evaluation of a power cycle test on parts with early failures is given in Fig.2; (Temperature difference: 80 K, failure critera: ΔV_T = 50 mV to initial value 1.5 V @ 200 A).

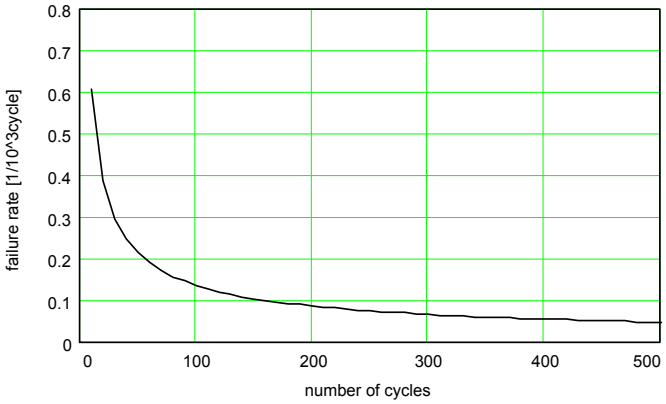


Fig. 2 Power Cycle: Early Failures, b = 0.353

c) Wear-Out

Power semiconductors rarely come up to fatigue or wear-out. Even accelerated tests take a long time to show this. Usually reliability tests are stopped at a time or number of cycles far from the fatigue.
Fig. 3 shows the result of a power cycle test that was carried out on a thyristor module to see the thermal fatigue; after six month (100 000 cycles, temperature difference 80 K, failure criteria: ΔV_T = 50 mV) the test was stopped. The Weibull analysis significantly points out wear-out.

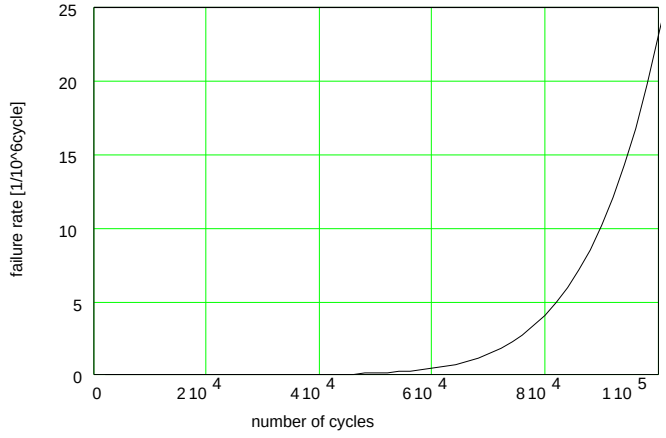


Fig. 3 Power Cycle: Wear-Out, b = 8.82

Reliability Tests

Table 1 shows the reliability tests which are performed continuously on power semiconductors and the relation to failure mode and important process parameters. Further tests are carried out on request or in particular cases, i. e. High Temperature Storage, Low Temperature Storage, HAST .
Mechanical tests (vibration,schock,acceleration) are performed on new or changed basic constructions.
HAST and mechanical tests will be performed by an outdoor test house.

Test						Failure Mode
High Temperature Reverse Bias (HTRB)		X			X	Degradation of breakdown characteristics
High Temperature Gate Bias (HTGB)				X		Rupture of gate oxide
Temperature Cycle		X	X	X		Thermal fatigue of silicon–metal and metal–metal interfaces
Power Cycle			X	X		Thermal fatigue of silicon–metal and metal–metal interfaces
Humidity Test	X	X			X	Degradation of electrical leakage characteristics

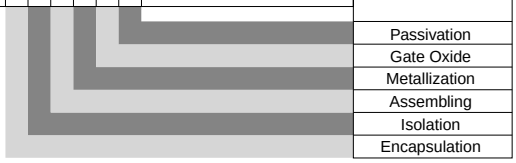


Table 1 Reliability tests,
failure mode and test sensitive process parameters

High Temperature Reverse Bias (HTRB)

If HTRB is applied on silicon chips in the devices, these chips must withstand a continuous blocking load at the PN junctions. In this case the protective functions of the passivation and encapsulation system is examined. The temperature is then adjusted such as to allow a temperature at the blocking junction of 125 °C taking in account the blocking losses. For diodes and thyristors an AC voltage is applied which is 70 % of the rated voltage. For FRED's, IGBT's and MOSFET's the applied DC voltage is 80 % of the rated voltage. The evaluation is done after 168 hrs for monitoring test and after 1000 hrs for qualification tests respectively (IEC 60747).

High Temperature Gate Bias HTGB

This test only is performed on MOSFET, HYPERFET and IGBT. In this case the gate oxide is examined and must withstand a continuous positve voltage. The applied voltage is 80 % of the rated continuous gate voltage. The temperature is adjusted to 125 °C for modules and to 150 °C for single devices (MIL-STD-750).

Temperature Cycle

The results of multiple temperature cycles ranging between the minimum and maximum storage temperatures listed in the data sheet show evidence how good different materials like plastics, metals, ceramic and silicon match and wether harmful thermomechanical stress occurs. The devices to be tested are brought into the cradle of a two-chamber temperature cycle cabinet. The cradle containing the devices moves perodically from a heat chamber to a low cooling chamber (IEC 68 -2-14, Method Na).

Power Cycle

Power cycle tests are carried out to prove the reliability of the power semiconductors after frequent switching on and off. The semiconductors to be tested are mounted on heatsinks. With the known thermal resistance of the power semiconductor and the cooling system the time of the current flow is adjusted such as to reach a junction temperature of 125 °C at each power cycle resulting in an amplitude of the chip temperature difference of 80 K (IEC 60747).

Humidity Test

A climatic test is required to determine wether the power semiconductors meet all the specifications when exposed to continuously humidity. Humidity can influence the blocking capability and attack internal connections by corrosion. This climatic test is performed on plastic encapsulated devices only. The test conditions are device depending:
module : 1000 hrs, 85 °C, 85 % r. H. (IEC 60749)
single device: 168 hrs, 125 °C, 100 % r. H.

Reliability Data

The results of reliability tests are of great importance for the user. To determine the reliability of his equipment the user needs data from the supplier with regard to failure rates of each individual part.
Results of our reliability tests are summarised in a special publication the "Reliability Report". This report is available on request.

Literature

[1] ISO 8402
Quality management and quality assurance - Vocabulary ;1995

[2] Norris, K. C., Landzberg, A. H.:
Reliability of Controlled Collapse Interconnections.
IBM J. Res. Devel., Vol. 13, page 266-271 (1969)

Technical Application

Is the lowest forward voltage drop of real schottky diodes always the best choice?

(By Dr. Günter Berndes; IXYS Semiconductor GmbH)

According to the thermionic emission model, pure Schottky barriers exhibit a forward voltage drop, which decreases linearly as the barrier height diminishes; whereas the reverse current increases exponentially as the barrier height decreases. Consequently, there exists an optimum barrier height, which can minimize the sum of forward and reverse power dissipation for a particular application.
However, discussions with the users of Schottky diodes reveal that they do not search for the minimum of forward and reverse power dissipation but always for the minimum forward voltage drop. Values of reverse current are very rarely asked for. One must know how the Schottky diode is being applied in order to objectively select the most appropriate part.

Low voltage level applications

In high power applications with low circuit voltages and using Schottky diodes with blocking voltages less than 25V, the forward power losses of the diodes still dominate in the balance of power losses. The prevailing applications are switched mode power supplies (SMPS). Here it is argued that a 4 mV decrease of the forward voltage drop results in a reduction of the forward power losses of approximately 1%. Therefore, the components created for this application have low barrier heights (less than 0.74 eV) and highly doped, thin epitaxial drift layers. This results in a device with a low forward voltage drop and high but still acceptable reverse current.

Medium and high voltage level applications

On the other hand, reverse power losses in high power applications using medium or high voltage Schottky types (V_{RRM} ranging from 45 V to 150 V) are comparable or can be even higher than the forward power losses. Nevertheless, most users don't ask for low reverse currents but again for only a low forward voltage drop.

Diode with an ideal dynamic behavior

In addition to forward and the reverse power losses, there is apparently a third quality, but one that is difficult to quantify. Nevertheless it has an impact on forward voltage drop as shown by experience.

I suppose that this quality is exhibited by the dynamic properties and switching loss of the real Schottky diode. Due to their short appearance in the range of only a few nanoseconds, they can only be measured with costly test equipment and moreover, the slight differences in their dependencies cannot be made evident.

With regard to the dynamic properties, the Schottky diode is generally considered as an ideal diode with a junction capacitance connected in parallel. Concerning the switching characteristics, the ideal diode is a pure majority-carrier component (only electrons in the n-region). After the zero crossing of the current from the forward state to the reverse state, the ideal diode fully ignores the previous conductive state and blocks reverse voltage immediately after the current crosses zero.

Fast reverse recovery pn-diodes

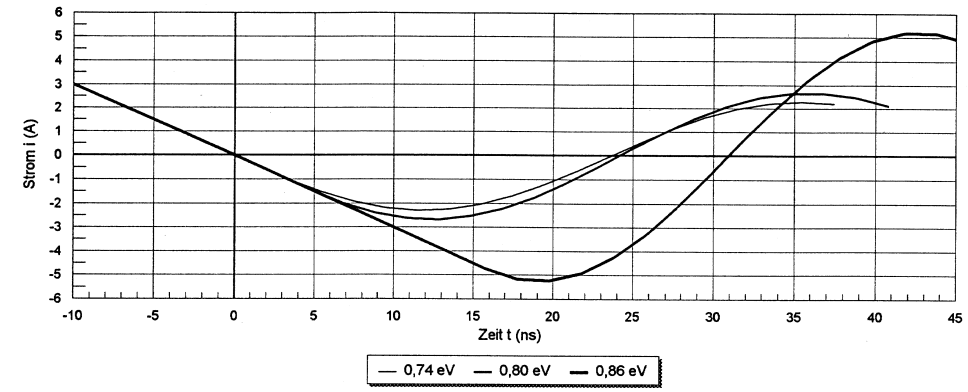
In contrast to the ideal diode, pn-diodes with minority-carrier current components still "remember" their previous on-state after forward current has decreased to zero. This is due to the injected minority carriers (holes in the n-region), which will decay exponentially with an adjusted minority carrier lifetime t or are swept out by the reverse current. The pn-diode regains its reverse blocking capability with a delay after zero crossing of current. The minority carrier lifetime can be decreased by diffusing lifetime killers (gold or platinum) into the n- region or by exposing the diode chip to radiation.

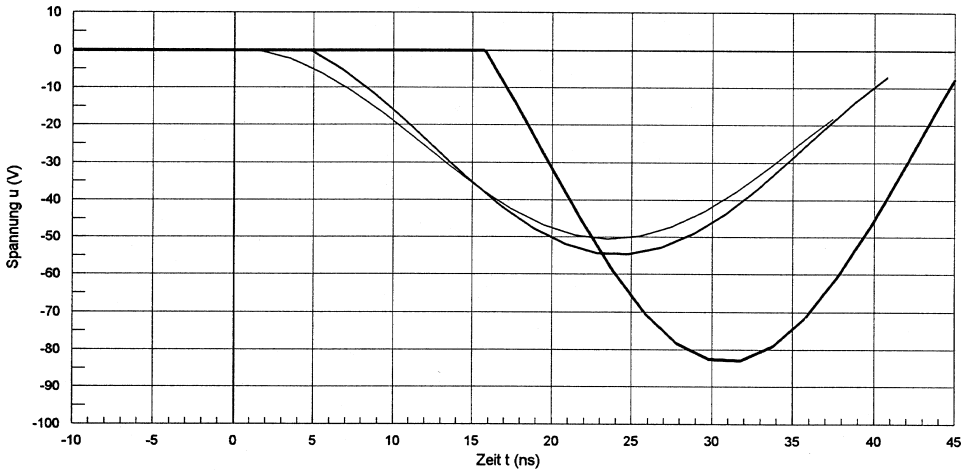
Real Schottky diodes

Real Schottky diodes also have minority-carrier injection through their barriers although it is smaller by several orders of magnitude. This phenomenon is called modulation of the epitaxial layer. The injection increases as the barrier height, voltage type, forward current density and the junction temperature increase.

Due to the above-mentioned, technical measuring difficulties, we have simulated the switch-off behavior of real Schottky diodes. In **figure 1** below, the resulting current and voltage waveforms for a Schottky diode with a type voltage of 100 V and an active area of 0.323 cm^2 are plotted versus time. The preset operating conditions are 50 A forward current, 300 A/µs during commutation, 25 V reverse bias voltage and 25°C junction temperature. Three different materials with barrier heights of 0.74, 0.8 and 0.86 eV are considered. The turn-off energies are 0.86, 1.0 and 2.3 µWs respectively.
The simulation model clearly shows that the remaining minority carriers from the conduction phase in the n-doped

Simulated reverse recovery behavior of a 100 V Schottky diode





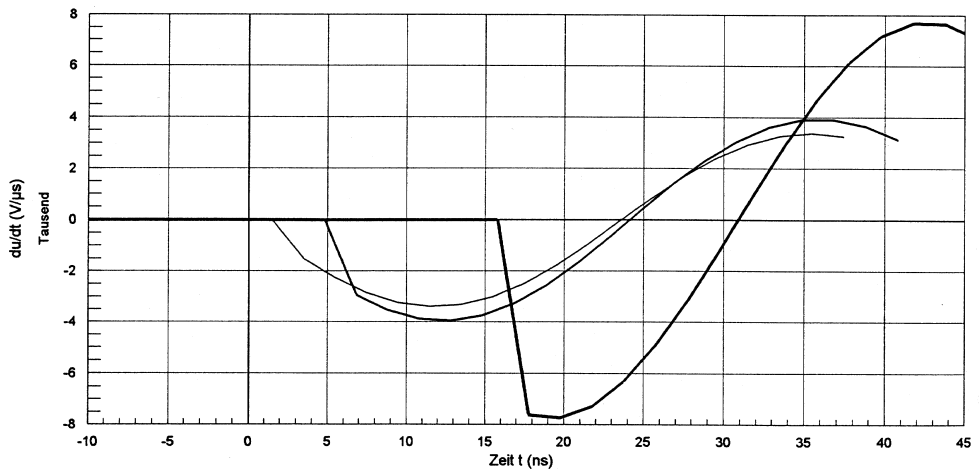


Fig. 1

epitaxial layer determine the initial conditions for the general solution of the differential equation of the LC circuit, which consists of a switch-off inductive coil, the junction capacitance and the forcing reverse voltage bias of 25 V. Due to the delayed capability of the real Schottky diode to block reverse voltage after commutation – growing with increasing barrier height -, the resonant circuit reacts with an excessive reverse current (i.e. greater than the commutation switching-off slope multiplied by the square root of LC), an excessive reverse voltage (i.e. more than twice the driving reverse voltage) and a steeply starting, excessive dv/dt (i.e. more than the driving reverse voltage divided by the square root of LC). The excess of the dynamic parameters and switching loss becomes more evident as the barrier height is increased.

The reaction at a barrier height of 0.74 eV with respect to dynamic behavior and switching loss is almost ideal for the example chosen above. Thus having the above mentioned rule in mind - the lower the barrier the lower the forward voltage drop of pure Schottky barrier - shows that the search for minimum forward voltage drop not only diminishes forward power loss but also switching loss in real Schottky diodes. It

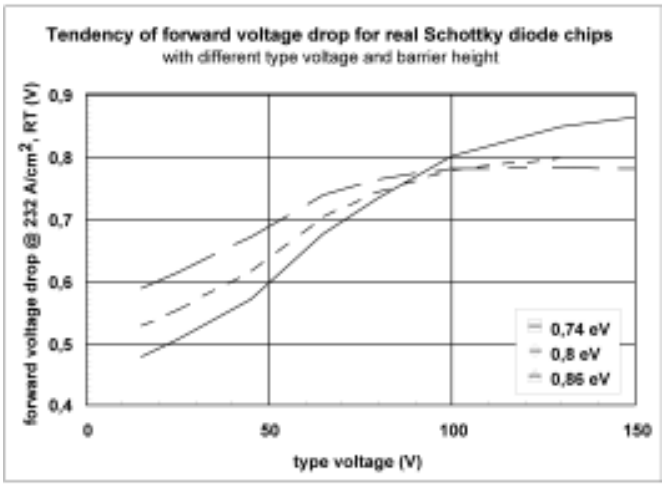


Fig. 2

explains the demand for low forward voltage drop even with high reverse current.

But this simple rule that low forward voltage drop corresponds to low switching loss does not hold for real Schottkys of type voltage above approximately 80 V. We have to take into account that forward voltage drop is the sum of drops over the actual barrier and the epitaxial drift layer. The second term becomes more pronounced with respect to the first term with increasing type voltage.

On the other hand, for increasing barrier heights and type voltage, the increased modulation in the epitaxial layer lowers the resistivity of and the forward voltage drop over the epitaxial drift layer. This lowering can become more pronounced than the increase of voltage drop over the actual barrier as figure 2 indicates. Numbers for our 100 V example at 232 A/cm2 and room temperature are: 1. diodes with the lowest forward voltage drop of 0.78 V for highest barrier 0.86 eV have worst dynamic values, and; 2. highest 0.8 V forward drop for lowest barrier 0.74 eV have best dynamic values. Thus real Schottky diodes of type voltage above 80 V with lowest forward voltage drop are not the fastest.

Application-specific adjustment of the barrier height

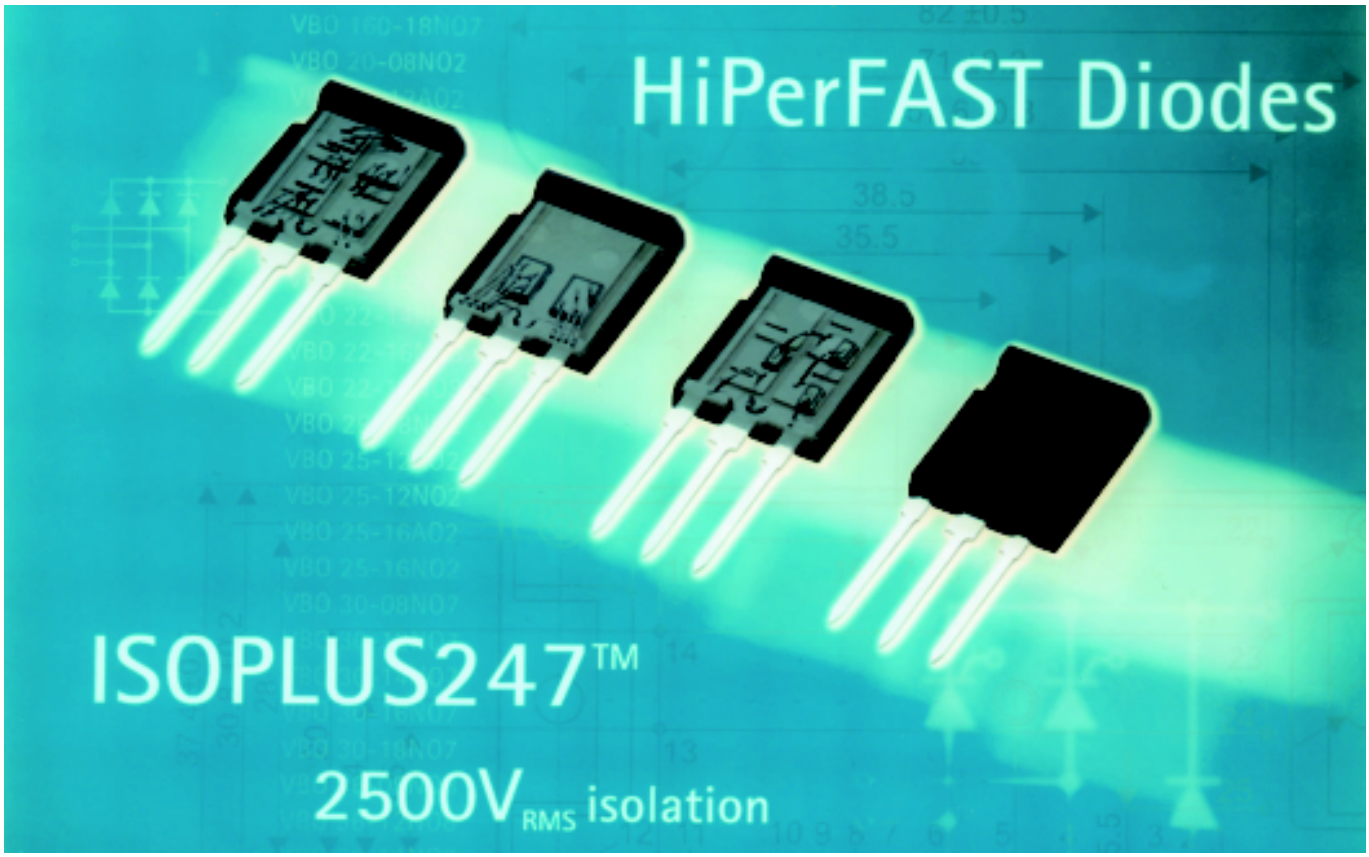
I am of the opinion that, for the circuit designer, deviations in the dynamic behavior and the corresponding switching loss from the ideal diode with a junction capacitance represent more disadvantageous behavior than a very high reverse current. In fact, the reverse current of a diode with a barrier height of 0.74 eV is about 25 times higher than that of a diode with 0.86 eV. Above a certain limit, the exponentially increasing reverse currents, typical of low barrier heights, become unacceptable. However, this depends on the respective application.

Our objective is to meet the special application requirements and the customers' needs by offering components with mixed barriers (values between 0.66 eV and 0.86 eV).

Fast, faster, fastest!

Optimised diodes for switching applications

by Udo Steinebrunner, IXYS Semiconductor GmbH



Great efforts have been made to improve power switches – MOSFETs and IGBTs – to decrease forward voltage drop, as well as to decrease turn-off energy. In switching inductive loads, the turn-on losses depend strongly of the behavior of the companion free-wheeling diode and now form the major part of over-all power losses. New developments like series connected diodes in a single package can greatly improve a given design. This article shows how to choose the optimum diode using the example of a PFC circuit.

FRANCAIS

Des efforts importante ont été faits pour améliorer les disjoncteurs MOSFET et IGBT - dons le but de réduire la chute de tension directe ainsi que l'énergie de coupure. Lors de la commutations à des charges inductives, les pertes à la mise en marche dépendent fortement du comportement de la diode adjointe de roue libre et constituent actuellement la part essentielle des pertes de courant totales. Les nouveaux développements, tels que les diodes connectées en serie dans un boitier unique, peuvent significativement améliorer une conception donnée. Cet article explique comment choisir la diode optimale sur la base d'un circuit correcteur de F.P.

DEUTSCH

Um Leistungsschalter wie MOSFETs und IGBTs zu verbessern, also die Vorwärtsspannung und die Abschaltenergie zu reduzieren, wurden grosse Anstrengungen unternommen. Beim Schalten von induktiven Lasten hängen die Einschaltverluste stark vom Verhalten der zugehörigen Freilaufdiode ab, sie spielen nun die wesentliche Rolle bei der totalen Verlustleistung. Neue Entwicklungen wie Serienschaltungen von Dioden können ein gegebenes Design erheblich verbessern. Der Artikel zeigt die Auswahl einer optimalen Diode anhand einer PFC-Schaltung.

In hard switching applications with an inductive load, the free-wheeling diode causes high losses during the turn-on transition of the power switch. Power factor correction in non resonant mode is a typical example for such hard inductive switching. A very common topology is the boost configuration (Fig. 1), using a MOSFET as the usual power switch at higher frequencies. Fig. 2 shows idealised current and voltage waveforms during the diode's turn-off and MOSFET's turn-on. These waveforms are also valid in inverter designs, where the diode and the power switch are parts of a phase leg. So the results obtained with this example can also be used for designing drive inverters, switched mode power supplies, line inverters and other similar applications.

A known method to achieve better performance for rectifiers for a given blocking voltage is to connect lower voltage diodes in series [1]. For equal voltage sharing, it is sometimes

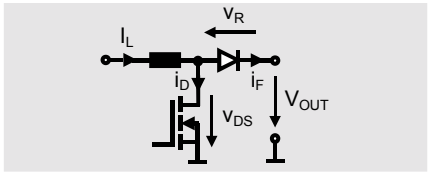


Fig. 1: *Boost converter principle, e. g. for power factor correction (PFC)*

necessary to connect RC snubber networks in parallel to each single diode, thereby making this solution rarely used. A newly developed housing makes it possible to connect two or more diodes in series within one single package. Matching and testing the dice for voltage sharing allows the user to design in these diodes without any additional snubber circuits. It now depends on the application and its switching frequency if single die or series connected diode is the better choice.

POWER LOSSES AND JUNCTION TEMPERATURE

A rectifier carrying a forward current needs a non-negligible time to change from the on-state to the blocking state. Until the reverse recovery charge Q_{rr} has not been removed from the P-N junction, the diode behaves like a short circuit – causing high current flowing not only through it self, but also through the power switch that is turning off the diode. As can be seen from Fig. 2, the maximum reverse recovery current I_{RM} of the diode is added to the load current I_L, so drain current of the MOSFET reaches the maximum $I_{RM} + I_L$. As the voltage drop for a short is zero, the switch carries not only high current but also sees the full output voltage V_{out}, resulting in enormous instantaneous power dissipation and thus turn-on

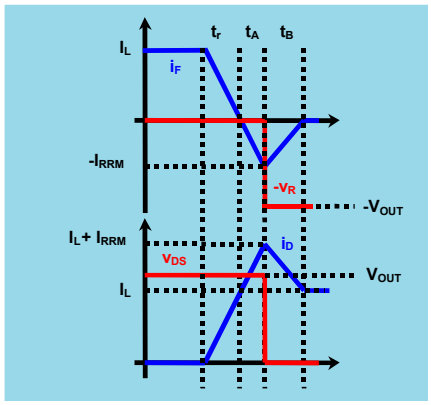


Fig. 2: *Idealised current and voltage waveforms; current commutates from diode to switch*

energy loss. Energy times frequency gives total power-loss, increasing junction-temperature of the semiconductor which in the end sets the limit for the switching frequency f_{sw}. But to reduce weight, volume and costs of passive components like inductors and capacitors (and which designer of a power supply does not want to this), it is necessary to go for higher switching frequencies f_{sw}. So over-all losses of the switch have to be reduced and the key for this is a better free-wheeling diode. At high switching frequencies, turn-off time and reverse recovery current should be as low as possible to save energy while the power switch turns on.

An estimation of switching energies can easily be derived from the curves in Fig. 2 by the use of following formulas [2]:

$$E_{off(diode)} = 0.5 \bullet I_{RM} \bullet V_{out} \bullet t_B \quad (1)$$

$$E_{on(MOSFET)} = 0.5 \bullet (I_{RM} + I_L) \bullet V_{out} \bullet (t_r + t_A) \quad (2)$$

It is obvious that turn-on losses of the switch will be higher than turn-of losses of the rectifier in this example. Turn-on energy of a diode is mostly small, turn-off and static losses of the MOSFET are independent of the diode so they are not from interest in this case.

To compare different diode types, it is also necessary to calculate their on-state and blocking losses. The first are obtained using the linear model of the output curve (Fig. 3):

$$P_{on} = V_{T0} \bullet I_{F(AV)} + r_T \bullet I_{F(RMS)}^2 \quad (3)$$

$$P_{off} = I_R \bullet V_R \bullet D$$
(Note: D = duty cycle) (4)

Dynamic losses are calculated by multiplying switching energy with switching frequency, so total diode losses become:

$$P_{tot(diode)} = P_{on} + E_{off(diode)} \bullet f_{sw} + P_{off} \quad (5)$$

To get junction temperature of the diode, power loss has to be multiplied by the thermal resistance from junction (J) to case (C):

$$T_J = P_{tot(diode)} \bullet R_{th(JC)} + T_C \quad (6)$$

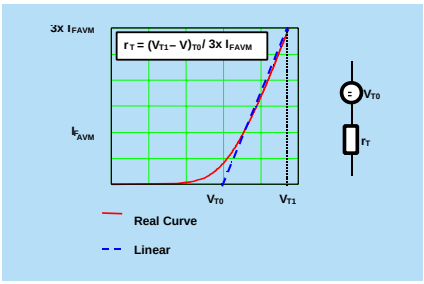


Fig. 3: *Linear model for the forward voltage drop of the output curve: deriving of V_{T0} and r_T*

A good compromise between improved reliability and optimized chip size (= optimized costs) is achieved with T_J around 125°C to 150°C. Therefore the values for the parameters in formulas (1) to (4) must be interpolated for the operating junction temperature T_J from the values given in the data sheet.

If all power losses affected by the free-wheeling diode are to derived, the following formula should be used:

$$P_{tot(diode\ affected)} = P_{on} + [E_{off(diode)} + E_{on(MOSFET)}] \bullet f_{sw} + P_{off} \quad (7)$$

Having derived all necessary formulas, it is now possible to draw some conclusions:

Diode selection depends strongly upon switching frequency. For lower frequency applications, forward voltage drop plays the major role in the diode's power loss. At higher frequencies, the switching losses become more and more important. Losses in the commutating switch will rise with frequency and dynamic behavior of the diode. To maintain low junction temperatures for increased reliability and lifetime, either power loss or thermal resistance must be decreased (or even both).

APPROACHES FOR DIODE OPTIMISATION

In addition to the well-known IXYS Fast Recovery Epitaxial Diodes (named DSEI... for single diodes and DSEK... for common cathode configuration), a new **Hi**gh **Per**formance **FRED** series has been developed called HiPerFRED™ (respectively DSEP... and DSEC...). Blocking currents have been reduced at high temperatures while dynamic parameters, like I_{RM} and t_{rr} (= $t_A + t_B$), were improved. Forward voltage drop decreases with increased T_J, giving lower static losses when the device is running at its working temperature.

Combining these diodes with the latest package development of IXYS, called ISOPLUS247™, it is possible to achieve acceptable junction temperatures even at high switching frequencies. ISOPLUS247™ is an isolated, discrete housing in which the standard copper

lead frame has been replaced by Direct-Copper-Bonded alumina, the same isolation material used in high power modules. This package meets the JEDEC standard TO-247 outline and is an UL recognised package. The ceramic isolation has an unbeatable low thermal resistance junction to heatsink while providing 2500 V_{RMS} isolation voltage from leads to backside.

ISOPLUS247™ also allows an interesting method for decreased dynamic parameters: series connection of diodes. Because the DCB-substrate can be patterned like a printed circuit board, it is easy to connect two or more chips in series in a single package. Fig. 4 shows the impact of series connection on V_F and I_{RM}. The higher the blocking voltage for the same chip size, the higher are also dynamic parameters and forward voltage drop. Connecting three 200 V devices in

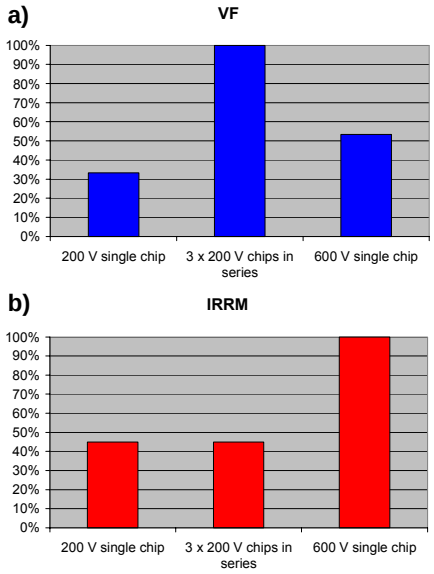


Fig. 4: *Effect of series connection on*
a) forward voltage drop and
b) reverse recovery current

series results in a 600 V blocking diode. The resulting voltage drop is increased by a factor of 3 but when compared to an actual 600 V diode, the value is only doubled (a). However, the big advantage is that the reverse recovery current is as low as of a single 200 V chip, in this case only half the value of the 600 V device (b).

Table 1: 600 V-diodes suitable for PFC and similar applications

Type	V_{RRM} [V]	I_{FAV} [A]	Total chip size	Package	Remarks
DSEP 8-06A	600	10	33%	TO-220	single chip
DSEP 9-06CR	600	9	83%	ISOPLUS247™	3 chips in series, isolated
DSEP 30-06B	600	30	100%	TO-247	single chip, high speed
Competition	600	8	-	TO-220	2 chips in series, isolated

Table 2: Static and dynamic parameters of the tested diodes

Type	V_F [V]	I_{RM} [A]	t_A [ns]	t_B [ns]
	I_F=10 A T_J=150°C	I_F=10 A, V_R=400 V -di/dt=300 A/µs, T_J=150°C		
DSEP 8-06A	1.24	15	37	43
DSEP 9-06CR	3.09	10	28	11
DSEP 30-06B	0.99	19	47	20
Competition	2.17	14	34	2

In table 1 there are three examples of diodes shown representing the above mentioned technologies [3,4]. All are rated at a blocking voltage of 600 V and are suited for the application described below. The DSEP 8-06A is a single chip diode with normal switching speed (suffix "A"). DSEP 9-06CR is a series connection of three 200 V diodes in one package which exhibits very low dynamic parameters (= "HiPer**Dyn**™FRED"). Suffix "C" corresponds to the "Lightspeed" IGBT series of IXYS, while "R" stands for the ISOPLUS247™ package. DSEP 30-06B finally is again a single chip device with improved switching speed (suffix "B"). A competitive, series-connected diode is listed last.

HOW TO CHOOSE THE OPTIMUM DIODE

A single phase PFC circuit which is fed from an input voltage of 230 V_{AC} and draws a current of 7 A_{RMS} gives a nominal input power of 1.6 kW. To simplify calculation the current is assumed to be rectangular with constant duty cycle of D=0.5 and constant amplitude of I_{peak}= 10A (RMS of rectangular waveform equals $I_{peak} \cdot \sqrt{D}$, thus giving the value mentioned above).

Static losses of the investigated diodes were calculated from formulas (3) and (4), dynamic losses of diode and turn-on losses of the switch from (1) and (2). Parameters needed for the calculations can all be found in the datasheets: V_{T0} and r_T were derived from the curve forward current vs. voltage drop as shown in Fig. 2. I_{RM} and t_{rr} were read out directly from their curves. For rough approximations, $t_A = t_B = t_{rr}/2$.

This method of getting the necessary parameters is useful for a first approximation of power losses. Having choosen suitable devices, it is recommended to measure dynamic losses within the application to prove the theoretical assumptions.

Results in Table 2 have been measured using the circuit shown in Fig. 1 under equal conditions so that now a direct comparison of the different types is possible.

With the measured values and the above calculations, the optimum diode for a given design can be found. Fig. 5 shows the total diode power losses vs. switching frequency according to equation (7) and using the values of Table 2. It can be seen that above 50 kHz, the series connected diodes lead to lowest power losses. At

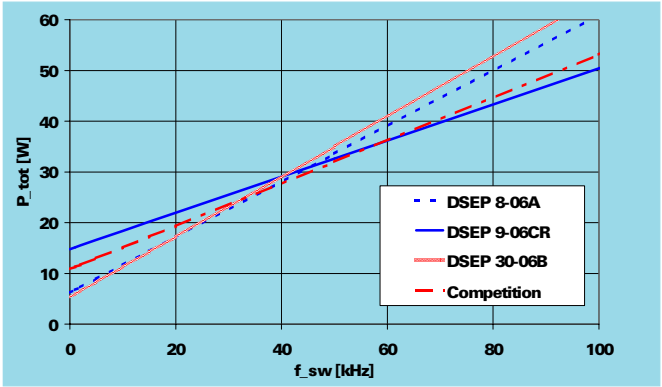


Fig. 5: *Diode affected power losses vs. switching frequency using Table 2 data*

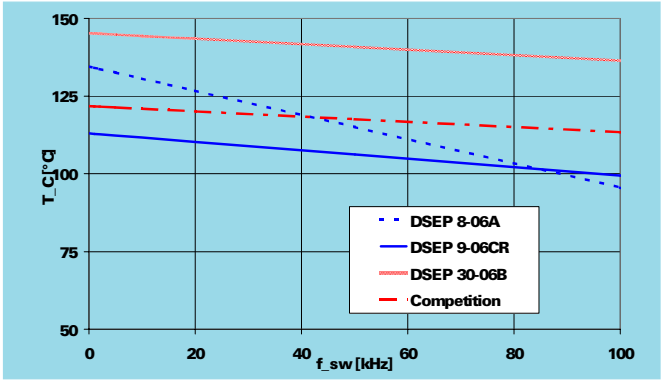


Fig. 6: *Maximum allowed case temperature vs. switching frequency using Table 2 data; T_J=150°C*

100 kHz the DSEP 9-06CR produces only 80% of the losses of the single chip diodes. So if total efficiency of the circuit is to be increased, one should use the series connected diodes.

In Fig. 6, the maximum allowed case temperature vs. switching frequency is shown calculated by formula (6), again using the values in Table 2. Junction temperature was set at 150°C, which is still well below the maximum value of 175°C for IXYS HiPerFRED™ diodes. Now the diode with largest chip size (DSEP 30-06B) requires lowest cooling effort and therefore it should be used if ambient temperatures are high or cooling is a problem. The series connected diode DSEP 9-06CR starts to outperform the smaller DSEP 8-06A single chip type above 80 kHz. Because in this diagram only diode losses appear, the cross-over point is higher than in Fig. 5; so turn-on losses of the power switch play a major rule in total diode affected losses!

Within the frequency range from 50 to 100 kHz (which is typical for most PFC applications), one has to make a decision depending upon the design goal. If the type of switch is already fixed and efficiency and cooling is no problem, the DSEP 8-06A would be best choice because it is least expensive. If the switching device has not been chosen yet, maybe a smaller part can be taken when using the series connected diodes because of reduced turn-on losses of the switch. In this case, overall costs may be lower compared to a solution with single chip diode and larger transistor. Above 100 kHz or if high system efficiency is required, there is no alternative to the series connected diodes. It may also be possible to discard active snubber networks that 'discharge' the diode junction before the main switch turns on so that there is no superimposed reverse recovery current in the main switch's drain current. Replacing the conventional rectifier with the series connected diodes with their very low reverse recovery current provides a similar effect without additional circuitry.

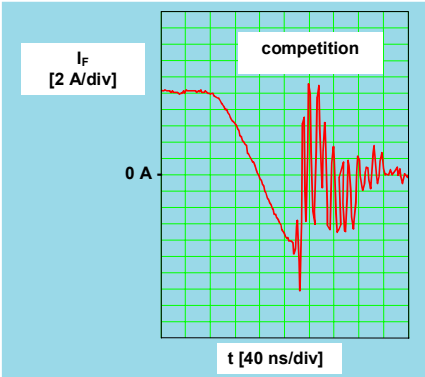


Fig. 7: *Turn-off behavior of competitive type; I_F=10 A, -di_F/dt=300 A/µs, V_R=400 V, T_J=150°C*

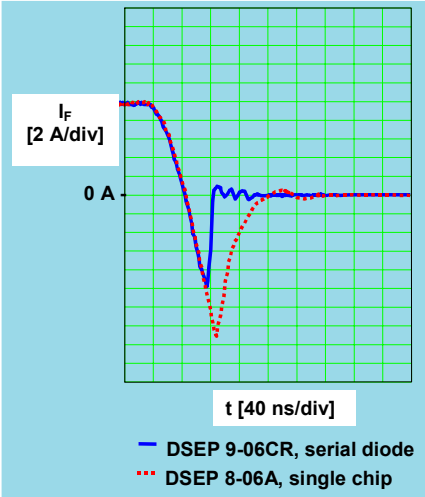


Fig. 8: *Comparison of series connected diode to single chip type; I_F=10 A, -di_F/dt=300 A/µs, V_R=400 V, T_J=150°C*

The competitive diode type requires less cooling effort than the IXYS series diode DSEP 9-06CR. This is due to its very short second portion of recovery time t_B, what leads according to formula (1) to low diode losses. The price which has to be paid for this is a very snappy turn-off behavior which might cause EMC problems as can be seen in Fig. 7. The DSEP 9-06CR is slightly slower but much softer, oscillations are negligible. Fig. 8 shows clearly its much better reverse recovery behaviour compared to the single chip diode DSEP 8-06A.

When connecting devices in series, it is normally necessary to ensure voltage sharing. This can be achieved by connecting RC-networks in parallel to each single part – resistors for static, capacitors for dynamic voltage sharing. For the above introduced, single package, series connected diode, there is no more the need for external networks. Chips built into one housing were matched so that parameter differences are kept low. 100% testing of both static and dynamic voltage sharing gives additional safety so devices can replace single chip parts without any restriction or the need for additional parts.

SUMMARY

It has been shown that, depending on switching frequency, there are optimised solutions. In the low frequency range, the single chip diodes are best because of their low static losses. In the medium frequency range, the user has to choose a suitable diode according to his main goal. If low cost is required, a single chip part is maybe the first choice but one should determine if the better performing series connected diode allows a smaller switch leading to lower overall costs. High ambient temperature or poor cooling ability leads to a large chip device with good heat transfer characteristic. High efficiency of the total system is achieved when using series connected diodes with low dynamic parameters. For this reason they are also unbeatable in the high and very high frequency range. The method described enables a designer to choose a perfect rectifier for his application.

REFERENCES

[1] B. Rivet: The Advantages of a 300 V Fast Recovery Epitaxial Diode (FRED)
Power Conversion, June 1997 Proceedings

[2] IXYS Technical Information 33: Fast Recovery Epitaxial Diodes

[3] IXYS Semiconductor Databook 2000, CD-ROM

[4] http://www.ixys.com

Fast Recovery Epitaxial Diodes (FRED)

Characteristics - Applications - Examples

During the last 10 years, power supply topology has undergone a basic change. Power supplies of all kinds are now constructed so that heavy and bulky 50/60 Hz mains transformers are no longer necessary. These transformers represented the major part of volume and weight of a traditional power supply. Today they have been replaced with smaller and lighter transfomers, whose core materials now consist of sintered ferrites instead of iron laminations and which can operate up to 250 kHz. For the same power rating, high frequency operation significantly reduces the weight and volume of the transformer. This development has been significantly influenced by new, fast switching power transistors, such as MOSFETS or IGBTs, working at high blocking voltages (V_{CES} > 600 V).

However, nearly all topologies equipped with these transistors also need ultrafast diodes to conduct the reactive load current and to rectify the AC output when DC voltage is required. The switching behavior of these diodes must be tailored to match the switching charcteristics of the transistors.

This is not only true for switch mode power supplies but also for inverter circuits. For these inverters, manufacturers have chosen PWM frequencies of about 8 kHz to create a smooth sinoidial waveform of the output current or have used a PWM frequency above 20 kHz in order to operate above the audible level. Apart from the characteristics of the transitor switches, the on-state and dynamic characteristics of the free wheeling diodes have a significant impact on the power loss, the efficiency and the degree of safety in operation of the whole equipment. They also play a decisive role when it comes to increasing the efficiency of a SMPS and to reduce the losses of an inverter, which clearly mandates that ultrafast diodes be used. The ultrafast diodes described here embrace all characteristics of modern epitaxial diodes, such as soft recovery, low reverse recovery current I_{RM} with short reverse recovery times.

[1] MOSFET = **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
[2] IGBT = **I**nsulated **G**ate **B**ipolar **T**ransistor

Technologies

The abbreviation FRED (**F**ast **R**ecovery **E**pitaxial **D**iodes) stands for a series of ultrafast diodes, which have gained wide acceptance during the last few years.

There exist several methods to control the switching characteristics of diodes and each leads to a different interdependency of forward voltage drop V_F, blocking voltage V_{RRM} and t_{rr} values. It is these interdependencies (or compromises) that differeniate the ultrafast diodes available on the market today. Fig.1 shows a qualitative relationship of forward voltage V_F and reverse recovery time t_{rr}. The most important parameters for the turn-on and turn-off behavior of a diode (Fig. 2) V_{FR}, V_F, t_{fr} and I_{RM}, t_{rr} will be influenced by different manufacturing processes. But as shown in Fig. 1, each technology must come up with a its own compromise between forward voltage and recovery time to obtain a device that will operate satisatisfac-torily.

Figure 2 shows a typical switching cycle for the diode. During forward conduction, the resistivity of the n- epitaxial layer (see Fig. 4) is decreased by excess minority charges (in this case holes) being stored there. When this forward current is commutated to another switch, the diode cannot regain its reverse blocking capability until this excess stored charge is removed, which can only be done by recombination of the stored holes with the background electrons or by reverse current flow through the diode. Since the ideal diode has zero reverse recovery

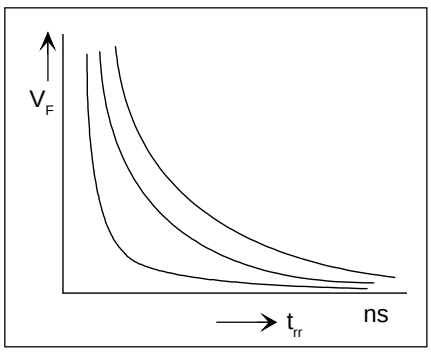


Fig. 1 Qualitative V_F - t_{rr} correlation to show this compromise for various FRED technologies

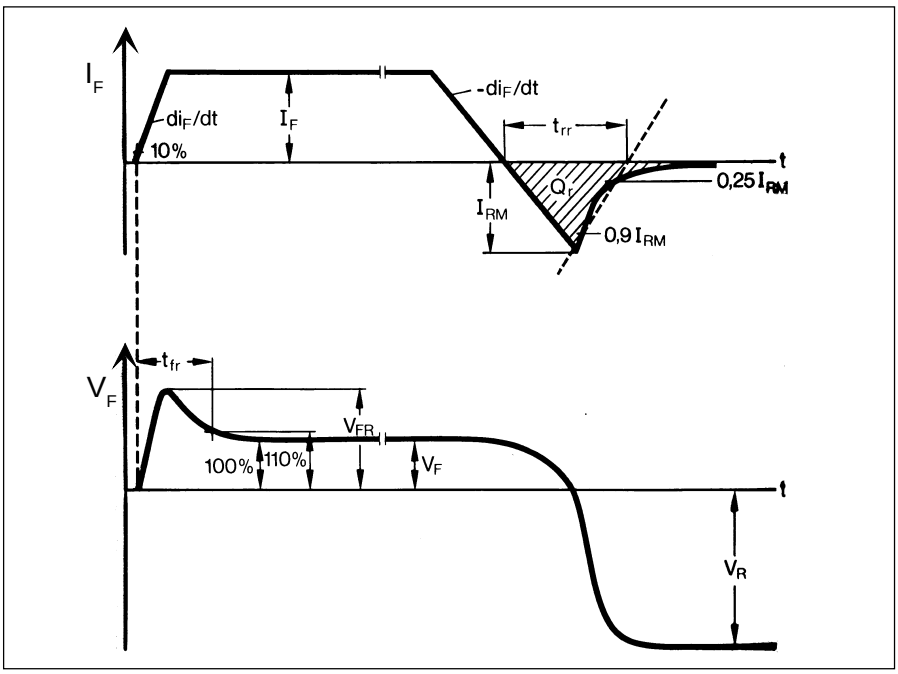


Fig. 2 Typical switching I/V waveforms for a FRED diode

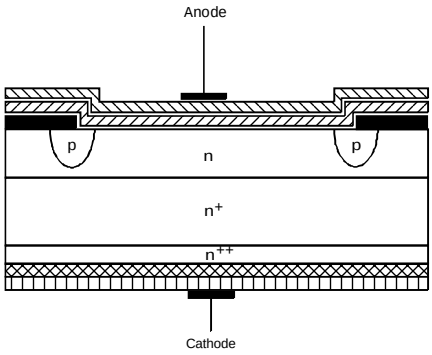


Fig. 3 Cross-sectional view of a Schotty diode

current, the recombination of stored charge must be accelerated, which is done by the introduction of recombination centers into the n- epitaxial layer. Of course, the end result will be that the stored charge both recombines and is swept out by reverse current, resulting in a short negative current pulse, called reverse recovery current. As the reverse recovery current reaches its maximun (I_{RM}), areas free of carriers develop at the pn-junction, which can then start to block voltage. The ensuing decrease of the recovery current is essentially determined by the actual distribution of the remaining carriers in the n-region. The decrease of the recovery current (di_R/dt) versus time is of special importance, because it determines the peak voltage and dv/dt transients that will occur. This will be discussed in more detail below.

As already mentioned, recombination centers are created within the diode to decrease reverse recovery current. The Schottky diode, whose cross-section is shown in Fig. 3, is a majority carrier diode, which can be switched very quickly, similar to a MOSFET. The observed reverse current is due to the charging of the metal barrier-silicon capacitance, which is independent of temperature. Up to now, Schottky diodes have only been used for applications with low reverse voltages (typically less than 60 V). However, newer types with higher blocking voltages up to 300 V and more are already available.

For applications requiring ultrafast diodes with blocking voltages in excess of 300 V, bipolar pn-junction FREDs are the only answer.

Characteristics

The most important processes to speed up the turn-off behavior of a bipolar diode are gold or platinum doping and electron irradiation. In the case of ultrafast diodes, the n-layer that supports the reverse voltage, should be made as thin as possible to minimize the forward voltage drop as well as the stored charge in the pn-junction. To obtain a wafer thickness that allows a good mechanical handling of the wafers, the epitaxial technology is the most favorable choice. This technology makes use of a relatively thick n+ doped wafer substrate for mechanical strength, on which a thin, monocrystal n-layer (the so-called epitaxial layer), is grown. The epi-layer thickness and resistivity are adjusted according to the desired blocking voltage capability.

The passivation of the pn-junction uses planar technology, which is similar to the manufacturing process of transistors. Guard rings reduce the electric field strength to prevent voltage break-down and the surface is glass-coated to ensure blocking voltage stability. To improve the turn-off behavior, either gold or platinum atoms can be diffused interstitially into the epilayer and these atoms act as trapping sites, in which the excess holes can recombine with electrons. Recombination centers can also be created by electron irradiation, which displaces silicon atoms from their normal cyrstalline lattice sites. Very high temperatures will allow the displaced silicon atoms to vibrate back into the lattice structure. Therefore, the irradiation is often followed by an annealing process to anneal out the low

Planar epitaxial diode, DWEP...

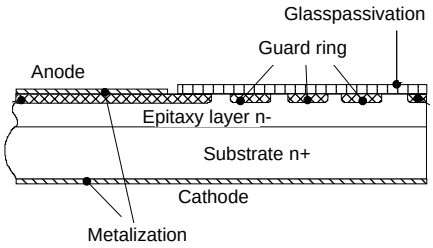


Fig. 4 Cross-sectional view of a FRED junction diode with planar passivation

temperature sensitive portion of the crystal disturbances. If the process parameters, irradiation energy and annealing temperature are properly chosen, the switching characteristic will remain stable. Table 1 shows all the essential characteristics of ultrafast diodes by process technologies.

Of course, any manufacturing process for ultrafast diodes has advantages as well as disadvantages. FRED diodes, using gold doping to control minority carrier lifetime, represent an excellent compromise between forward voltage, low peak reverse recovery currents with soft recovery. These diodes are charac-terized by a soft recovery behavior from -40°C to +150°C, showing even at very high $-di_F/dt$ (> 800 A/µs) no tendency to “snap-off.” The higher leakage current of the gold doped diode is, in compari-son to the platin doped or irradiated diode, the only disadvantage. However in most applications, the power loss caused by the leakage current is small in comparison to forward current and reverse recovery losses (Fig. 5) [1].

Table 1 Comparative advantages of ultrafast diodes by process technologies

Gold Doped	Platinum Doped	Electron Irradiation	Schottky Diodes
Soft reverse recovery	Tendency to snapp-off	Tendency to snapp-off	Much better turn-off than gold
Good V_F - t_{rr} trade-off, very short t_{rr} with much higher V_F	Good V_F - t_{rr} trade-off at nearly the same V_F as gold; higher I_{RM} for same t_{rr} than gold	V_F - t_{rr} trade-off not as good as Pt or Au doping; clearly longer t_{rr}	Very small I_{RM}, low V_F at low V_R
High I_R at high temperatures (100°C)	Low I_R	Low I_R	Very high I_R, even at room temperature, relatively low V_R

Free Wheeling Diodes

These diodes are mainly used as free wheeling diodes, connected in parallel to fast switching transistors working with an inductive load such as e.g. inductors in a boost or buck converter, transformers and motors. The majority of these circuits is controlled by pulse width modulation working at a fixed frequency. Forced by the inductive load, the current must continue to flow via a free wheeling circuit. In case the transistor is turned-on, the free wheeling path must be blocked to prevent a short circuit. The typical interaction between the power transistor and the free wheeling diode is described in the following example.

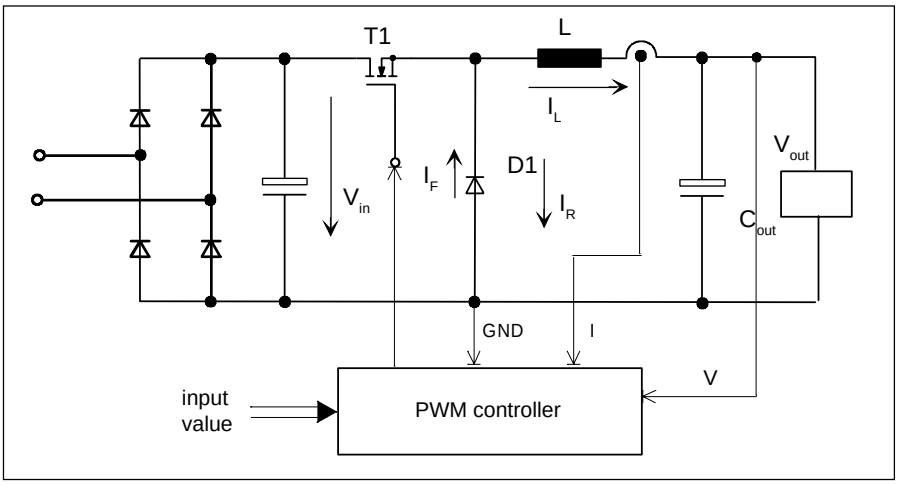


Fig. 6 Buck-converter circuit diagram

Fig. 6 shows the simplified circuit of a buck converter. This circuit provides an output voltage V_{out} which is lower than the supply voltage V_{in}. Fig. 7 shows the control signals of T1 and the voltage and current waveforms of T1 and D1. The conducting and blocking phases of the two active elements T1 and D1 can be devided as follows:

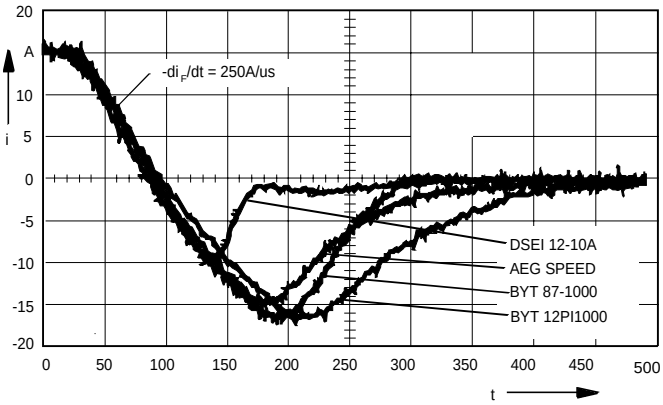


Fig. 5 Comparison of reverse recovery currents for several different FREDs [1]

At a certain time t_0 the controller switches on T1. The series circuit of L and C_{out} is connected to the supply voltage V_{in} and makes the current I_L increase linearly. This current is deter-mined by the inductor L and the output voltage V_{out}. After a certain time, fixed by the controller, T1 is switched off again. In the discontinuous mode of operation, the energy stored in L ($W = 0.5 \bullet L \bullet I_L^2$) is transferred via the free wheeling path into the capacitor C_{out}.

At a certain time t_2, T1 is switched on again and the whole precedure is repeated.

The switching action of Diode D1 is characterized by four important phases:

A. the diode blocks while T1 is in the on-state,

B. the transition from blocking to conducting mode: turn-on,

C. the diode conducts forward current while T1 is blocked,

D. the transition from conducting to blocking mode: turn-off.

A. Blocking Mode

While the MOSFET T1 is conducting, the supply voltage V_{in} appears as reverse voltage at diode D1. As with all semiconductors, a low current in the diode flows from the cathode to the anode (leakage current I_R). The leak-age current depends on the blocking voltage cabability, on the temperature of the diode chip and, above all, on the technology of the diode. Together with the applied reverse voltage the reverse power loss is:

$P_{SP} = V_{in} \bullet I_R$

B. Turn-On

With the transistor T1 switched off, the current I_L in the inductor must keep on flowing. The voltage across the diode drops down and the diode takes over the current of the inductor. The current rise time in D1 equals the current fall time in T1. The volume charge formed in the pn-junction of the diode during the blocking phase is flooded by carriers causing a change of resistance of the pn-junction during current rise time. This turn-on of the diode is accompanied by a short overvoltage in forward direction which depends on the chip temperature, on the -di$_F$/dt and again on the chip technology.

Compared to the blocking voltage, the overvoltage is very low (< 50 V) and for most applications, it is not important to the operation of the diode (waveform D1 in Fig. 7). However, this dynamic turn-on voltage of the diode does add to the peak voltage that appears across the transistor T1 and adds to its turn-off losses.

The overvoltage V_{FR} determines the turn-on losses of the diode. These turn-on losses increase linearly with the switching frequency.

C. On-State

Once the turn-on phase is over, the diode conducts the forward current I_F. There is a forward voltage drop V_F due to the threshold voltage of the pn-junction and the resistance of the semi-conductor. This voltage drop depends, as already mentioned, on the chip temperature, the forward current I_F and the process technology.

To indicate the forward voltage drop at various currents and, consequently, to calculate the on-state losses, the parameters V_{T0} and r_T often appear in datasheets.

A simplified model for the forward voltage drop shown in Fig. 8 is:

$V_F = r_T \bullet I_F + V_{T0}$

The on-state power dissipation can then be calculated accordingly:

$P_D = V_{T0} \bullet I_F + r_T \bullet I_F^2$

The calculated losses, however, are only approximate values, as V_{T0} and r_T depend a great deal on the temperature and are only given for a certain temper-ature (T_{VJM}). Since this temperature can differ from the actual operating temper-ature, the calculated losses are only valid for the given temperature.

D. Turn-Off

Apart from the on-state characteristic, the turn-off behavior is considered to be the most important parameter in determining the suitability of the diode for a high frequency application. If the current I_F is commutated to the transistor, it decreases linearly with the di/dt at which the transistor turns on the current. In the case of power MOSFETs and IGBTs, $-di_F/dt$ values of more than 1000 A/µs can easily be reached. As mentioned before, the carriers which have flooded the pn-junction during the on-state phase must be removed before the diode can start to block reverse voltage.

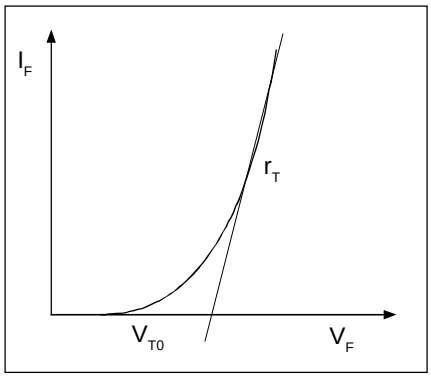


Fig. 8 Typical forward voltage drop V_F versus current its model, $V_{T0} + I_F \bullet r_T$

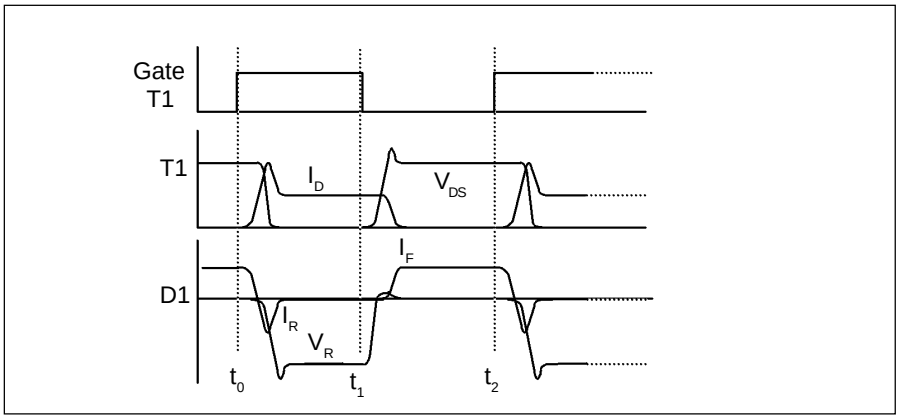


Fig. 7 Transistor gate signals, current and voltage waveforms along with the diode current and voltage waveforms for one switching cycle of the buck-converter shown in Fig. 6

What results is the reverse recovery current I_R, whose waveform depends on the chip temperature, the forward current I_F, the $-di_F/dt$ and the technology.

Fig. 9 shows how the reverse recovery current depends on the chip temperature of a gold doped (9a) and a platinum doped (9b) epitaxial diode of the same forward characteristic.

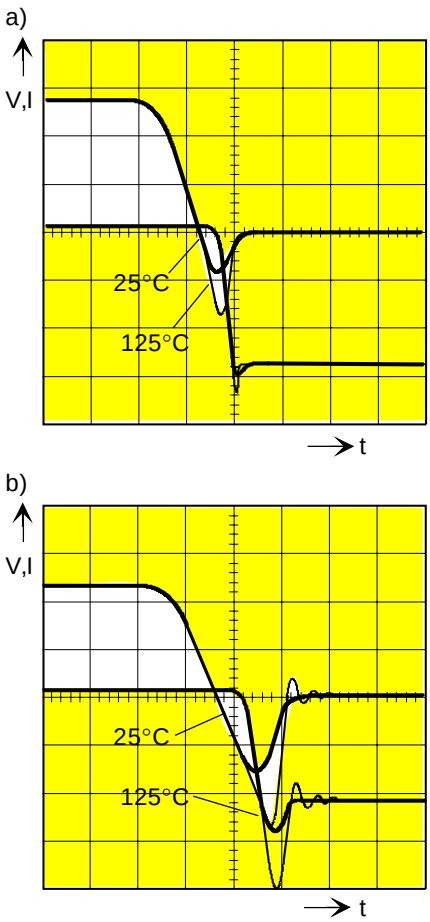


Fig. 9 Reverse recovery current and voltage for two FRED diodes at T_{VJ} = 25°C und 125°C
a) gold-doped diode
b) platinum-doped diode

The difference between the two technologies is really striking, if one compares the recovery behavior at various $-di_F/dt$ and at the same temperature.

Whereas, in the case of platinum, the decrease of the recovery current speeds up (Fig. 10b), the gold diodes with controlled minority carrier reduction keep their soft recovery behavior, even at high $-di_F/dt$ values (Fig. 10a).

The faster the decrease of the recovery current (the diode gets "snappy"), the higher the overvoltage caused by the stray inductances of the circuit lay-out. If the maximum voltage reaches the maximum blocking voltage of the transistor, snubbers must be used to guarantee the safety in operation of the equipment. Furthermore, much too high dv/dt values cause EMI/RFI problems, which complicate the shielding, if certain RFI limits have to be kept.

The reverse recovery current flowing in the diode does not only determine the turn-off losses of the diode but also adds to the turn-on losses of the transistor, which now carries the diode current.

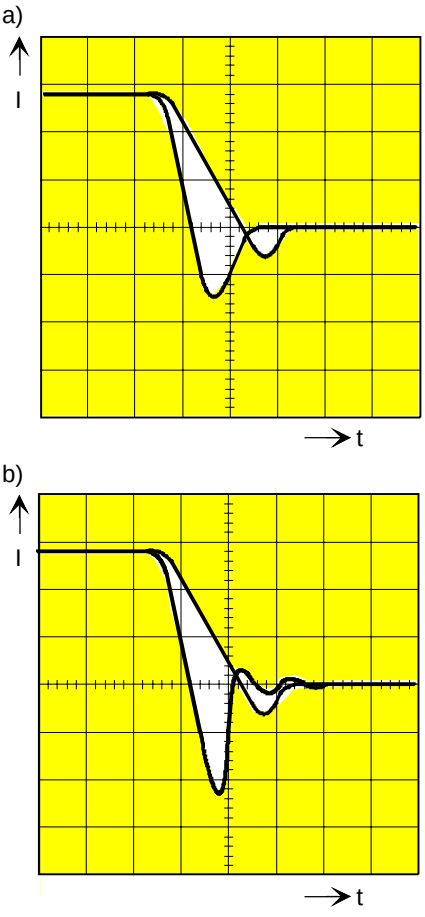


Fig. 10 Reverse recovery currents for different $-di_F/dt$ at T_J = 125°C
a) gold-doped diode
b) platinum-doped diode

The reverse recovery current must be added to the current in the inductor and the turn-on time extended by some portion of trr (Fig. 11a and b).

Figures 11a and 11b emphasize the significance of a low peak recovery current accompanied by soft recovery behavior. In the first place, the soft recovery behavior of the gold doped diodes entails a small overvoltage and a low reverse recovery current. Therefore the diode is marked by low turn-off losses. Secondly, the low reverse recovery current leads to essentially reduced turn-on losses in the transistor. Thus, the choice of the diodes decisively influences the power losses in both devices.

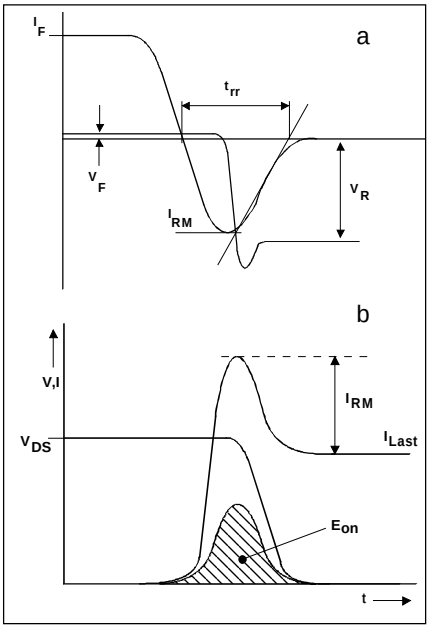


Fig. 11a Reverse recovery waveforms for a free-wheeling diode
Fig. 11b Transistor current and voltage waveforms showing the impact of reverse recovery current as it commu-tates off the free-wheeling diode

Example

The following example illustrates how to calculate the power losses of the free wheeling diode D1 in a buck-converter (Fig. 5). The epitaxial diode, type DSEI 30-10 A, is described in the slightly shortened datasheet (page D1-16), where one can also find the respective data to calculate the power losses.

Operating conditions of the buck-converter:

DC-link voltage V_{in}	600	V
Current fall time of MOSFET t_f	60	ns
Output voltage V_{out}	300	V
Switching frequency f_t	50	kHz
Inductor current I_L	15	A
Duty cycle of MOSFET d	0.5	
Max. junction temperature T_{VJ}	125	°C

A. Maximum Blocking Losses

From datasheet page 11: I_{Rmax} = 7 mA at T_{VJ} = 125°C, V_R = 800 V

$P_{SP} = V_{in} \bullet I_{Rmax} \bullet d = 600\ V \bullet 7\ mA \bullet 0.5$

P_{SP} = 2.1 W

B. Turn-on Losses

The calculation of the actual turn-on losses is much more difficult than the calculation of the blocking losses or on-state losses. There is no static operation, the current and the voltage of the diode are functions of time and can only be calculated approximately by using exponential and hyberbolic equations.

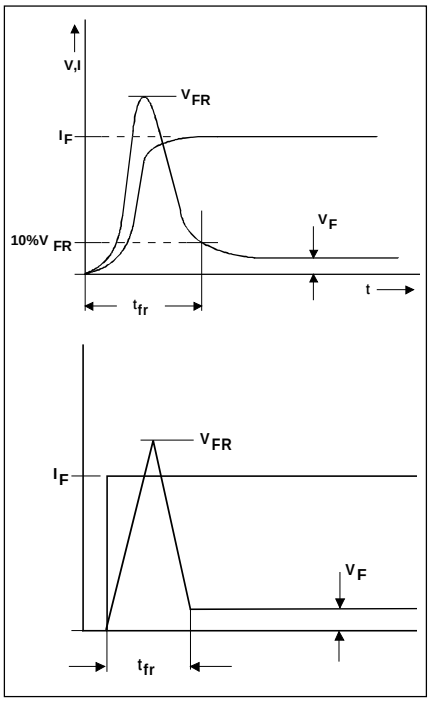


Fig. 12 Actual diode turn-on V/I waveforms and their linearized approximations to simplify turn-on power loss calculations

To estimate the diode turn-on losses, the turn-on waveform is given in a simplified form in Fig. 12. This simplification is conservative, i.e. the actual turn-on losses are smaller than the calculated ones, and makes it possible to do the calculation using the datasheet values.

The current rise time is determined by the turn-off time of the MOSFET and the load current:

$di_F/dt = I_F/t_f = 15\ A/60\ ns = 250\ A/\mu s$

The diagram in Fig. 6 of the datasheet shows the turn-on recovery time t_{fr} and the turn-on overvoltage V_{FR} for a $-di_F/dt$ = 250 A/µs : V_{FR} = 31.5 V
t_{fr} = 360 ns

To calculate the turn-on energy, the current I_F, which is assumed to be constant, is multiplied by the triangle waveform of the overvoltage V_{FR} and by the time t_{fr}:

$E_{on} = I_F \bullet V_{FR} \bullet t_{fr} \bullet 0.5 =$

$E_{on} = 15\ A \bullet 31.5\ V \bullet 360\ ns \bullet 0.5 =$

$E_{on} = 85\ \mu J$

The turn-on power losses can be calculated by multiplying the pulse energy E_{on} by the switching frequency:

$P_{on} = E_{on} \bullet f_t = 85\ \mu J \bullet 50\ kHz =$

P_{on} = 4.3 W

C. On-State Losses

The on-state forward voltage at I_F = 15 A and T_{VJ} = 125°C is shown in the diagram in Fig. 1, page 12. The on-state forward voltage at 15 A is given by the V_F curve for T_{VJ} = 100°C: V_F = 1.77 V

Thus the following on-state losses can be calculated:

$P_D = V_F \bullet I_F \bullet d = 1.77\ V \bullet 15\ A \bullet 0.5 =$

P_D = 13.3 W

If one calculates the on-state losses using the formula
$P_D \approx (V_{T0} \bullet I_F + r_T \bullet I_F^2)$ (1-d), one gets a smaller value:
V_{T0} = 1.5 V and r_T = 12.5 mΩ
$P_D \approx 1.5\ V \bullet 15\ A \bullet 0.5 + 12.5\ m\Omega \bullet 15\ A^2 \bullet 0.5^2$

$P_D \approx$ 12 W

D. Turn-off Losses

Similar to the turn-on losses, the turn-off losses can only be calculated approximately using the datasheet values. Once again, the waveforms of the voltage and of the current are simplified (Fig.13).

If one assumes the same di_F/dt as given during switch-on, the diagrams of Fig. 3 and Fig. 5 of the datasheet show: I_{RM} = 15 A, t_{rr} = 100 ns. These data are valid for T_{VJ} = 100°C and must be multiplied by a factor adjusting these data for T_{VJ} = 125°C. This factor K_f is given in the diagram of Fig. 4 of the datasheet. For T_{VJ} = 125°C the data for I_{RM} are to be multiplied by 1.1. This simplified calculation of the turn-off behavior results in a turn-off energy of:

$E_{off} = I_{RM} \bullet K_f \bullet V_R \bullet t_{rr}/2 \bullet 0.5$

$E_{off} = 15\ A \bullet 1.1 \bullet 600\ V \bullet 50\ ns \bullet 0.5 =$

$E_{off} = 248\ \mu J$

The multiplication by the switching frequency results in a turn-off power loss:

$P_{off} = E_{off} \bullet f_t = 248\ \mu J \bullet 50\ kHz$

P_{off} = 12.5 W

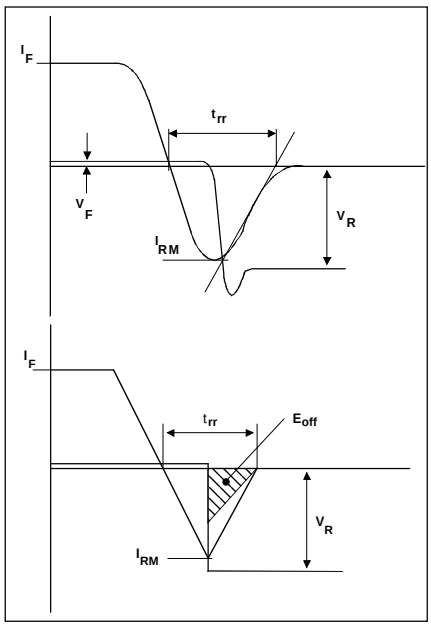


Fig. 13 Actual diode reverse recovery I/V waveforms and their linearized approximations

The total losses of the diode in the buck-converter are:

$P_{tot} = P_{SP} + P_{on} + P_D + P_{off}$

$P_{tot} = 2.1\ W + 4.3\ W + 13.3\ W + 12.4\ W$

P_{tot} = 32.1 W

Using the thermal resistance R_{thJC} = 0.9 K/W , which is shown in the data-sheet, the chip temperature is 29°C above the case temperature. Assuming a thermal resistance of R_{thCK} = 0.25 K/W and a chip temperature of less than 125°C, the maximum heatsink temperature may not exceed 88°C:

$T_{Kmax} = T_{VJM} - (R_{thJC} + R_{thCK}) \bullet P_{tot}$

$T_{Kmax} = 125°C - (0.9+0.25)\ K/W \bullet 32.1\ W =$

$T_{Kmax} = 88°C$

While this application used a buck-converter circuit as an example, the same approximations and calculations can be used for the boost-converter.

Further Applications

Rectifier Diodes

Ultrafast epitaxial diodes are used as rectifier diodes but only if the switching frequency is higher than 1 kHz and the blocking voltage exceeds 200 V. These conditions are very common in switch-mode power supplies delivering output voltages of more than 200 V, because there are no Schottky barrier diodes with the required blocking voltage capability (Fig. 14). Switch-mode power supplies generally operate with a PWM controller. Therefore the mode of operation of the epi-diode used as rectifier is very similar to that of the free wheeling diode. As the current and voltage waveforms are rectangular, the calculation of the power losses can be carried out as described in the case of the free wheeling diode.

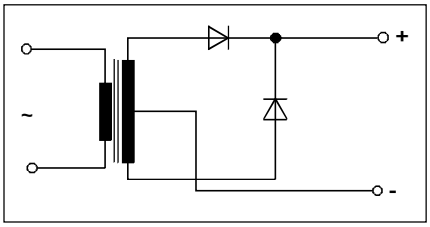


Fig. 14 Center-tapped DC output circuit with common-cathode diode connection

Snubber Diodes

"Snubber" circuits are used to protect power semiconductors from being destroyed by short overvoltage spikes. The di/dt values of more than 1000 A/µs, which can be reached with transistors (MOSFETs or IGBTs), cause overvoltages due to the parasitic stray inductances of the circuit wiring.

The equation V = L • di/dt underlines how high these overvoltages can be, even at very low stray inductances. For example, for the the case of a -di/dt of 1000 A/µs during switch-off with a stray inductance of 100 nH, the computed voltage spike is:

V = 100 nH • 1000 A/µs = 100 V

This 100 V spike, which will be added to the DC bus voltage, will require the use of a higher voltage MOSFET or IGBT. These devices not only cost more but the efficiency of the circuit will decrease due to their higher switching losses. Snubber circuits can limit the generated overvoltage transferring the energy stored in the stray inductances to a capacitor. Apart from its capaci-tance, the turn-on behavior of the diode determines the remaining overvoltage.

The diagram in Fig. 6 of the datasheet illustrates the forward recovery voltage V_{FR}, which can be expected, and the forward recovery time t_{fr} for various di/dt values.

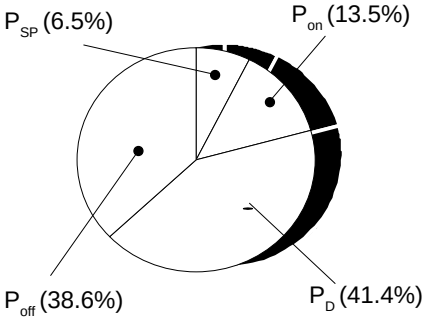


Fig. 15 Comparative losses for the free-wheeling diode in the buck-converter example

Summary

As depicted in detail, ultrafast diodes can have different characteristics depending on the manufacturing process. These characteristics should be considered to make best use of them in the various applications.
If standard FREDs in an existing circuit are replaced by DSEI diodes, the power losses of both the diode and the transistor can thus be reduced. The soft recovery behavior of all DSEI diodes also prevents the transistor from being overloaded by too high a dv/dt or overvoltage spike and also reduces EMI/RFI.

The market for ultrafast diodes is constantly expanding. Apart from their standard application as free wheeling diode in inverters, these diodes are also more and more used in snubber circuits and in rectifier circuits in switch-mode power supplies.

All FRED diodes delivered by IXYS are characterized by very low reverse recovery currents, even at high $-di_F/dt$. Simultaneaously, they show a soft decrease of the reverse recovery current, thus avoiding inductive overvoltages with very high dv/dt. These overvoltages could cause a malfunction or even the destruction of the active switching device, eg. a MOSFET, an IGBT or bipolar transistor.

The given example of the buck-converter shows, that when choosing an ultrafast diode, all operating modes taken together must be considered and not only the individual parameters.

The losses of the diode in the buck-converter can be divided as illustrated in Fig. 15. The on-state and turn-off losses make up 80 % of the total losses of the diode. The determining factors of these losses are:
$P_D \sim V_F$
$P_{off} \sim t_{rr}, I_{RM}$
IXYS offers ultrafast diodes (FRED = **F**ast **R**ecovery **E**pitaxial **D**iodes) in the TO-220, TO-247 and SOT-227B packages. These diodes are available with blocking voltages from 400 to 1200 V. Furthermore, IXYS provides FRED modules in various topologies up to 300 A and 1200 V (table 2, page 10).

FRED Modules

The FRED modules type MEO, MEE, MEA and MEK (Fig. 16) are an extension of the discrete DSEI to higher current while sharing the same diode characteristics mentioned before. They can be applied in all circuits with MOSFETs, IGBTs or bipolar Darlingtons, working at switching frequencies of more than about 1 kHz.

If the paralleling of several discrete diodes or miniBLOCs is necessary, these modules represent a possible alternative to minimize the assembly time and the size of the final equipment. Generally the FRED modules can be used as free wheeling diodes for high current IGBTs or for bipolar Darlingtons and as fast rectifiers in power supplies and welding equipments. What follows is a series of applications showing the use of FRED modules.

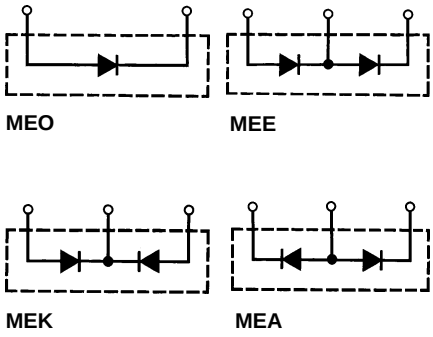


Fig. 16 Circuit diagrams for the available FRED modules

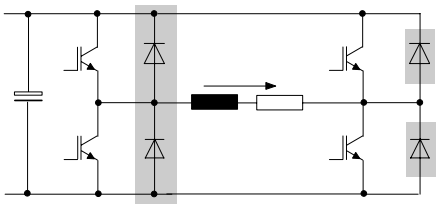


Fig. 17 MEE type or MEO type

A. Application as free wheeling diode in one or three phase inverters for drive and UPS systems, working with PWM controlling and switching frequen-cies in the kHz range (Fig. 17)

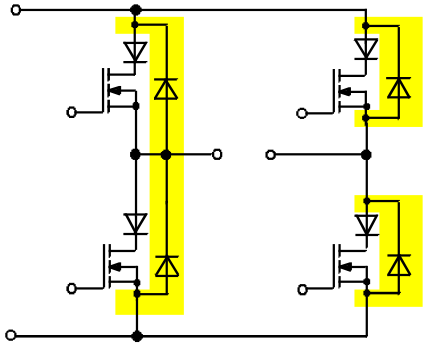


Fig. 18a MEE type or MEO type

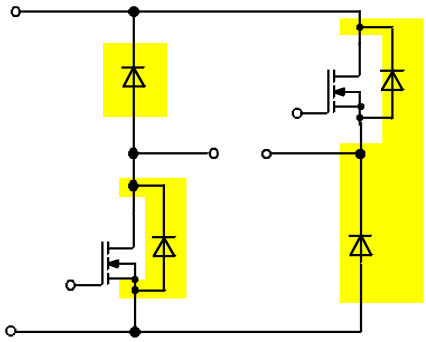


Fig. 18b MEO type or MEE type

B. Application as free wheeling diode in switch-mode power supplies and servo drives

a. symmetrical full bridge with MOSFETs and Schottky blocking di-odes (Fig. 18a)

b. assymmetrical full bridge with MOSFETs for forward converters and DC motor drives (Fig. 18b)

C. Application as rectifier in power supplies and welding equipments

Half-wave rectifier (Fig. 19a). Depending on the load current, several MEO modules can be paralleled.

Common cathode topology (Fig. 19b). Depending on the load current, several MEK modules can be paralleled.

Common anode topology (Fig. 19c). Depending on the load current, several MEA modules can be paralleled.

Full bridge rectifier (Fig.19 d). Depending on the load current, either MEE or MEO modules can be paralleled.

Full bridge rectifer for higher output voltages (Fig. 19e). Here both diodes in the MEE module are connected in series to obtain a higher/blocking voltage.

For all FRED modules the continuous DC current I_{FAVM} is given at a heatsink temperature of T_S = 65°C and a junction temperature T_{VJM} = 125°C (difference of temperature = 60°C).
When comparing these modules with types of the competition, one has to make sure that the two modules to be compared share the same difference of temperature between heatsink (case) and junction, because this is what determines the maximum allowable forward current.

Furthermore, the current ratings for the FRED modules include the blocking losses of the diode at T_{VJ} = 125°C and at a duty cycle of d = 50 %.

Parallel and Series Connection of the Modules

All FRED modules consist of several individual diode chips, which are connected in parallel internally to obtain the desired current rating of the module. In order to get a good current sharing between the diode chips, they are selected in such a way that the forward voltage drop V_F is nearly the same for all chips in parallel. This V_F selection facilitates the parallel connection as well as the series connection of several modules.

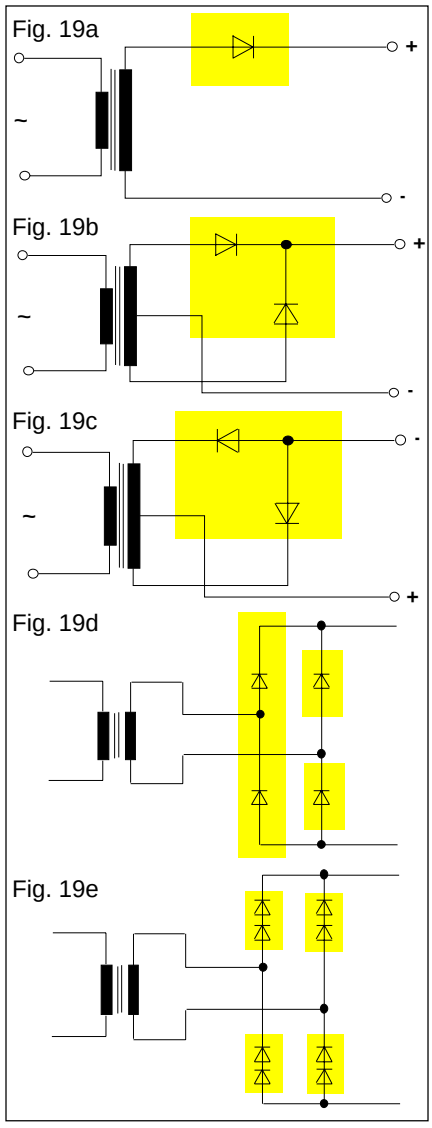


Fig. 19a-e Examples of different FRED modules as output rectfiiers in power supplies

Parallel and Series Connection of the Modules

Parallel Connection

To simplify the parallel connection of several modules, they are tested for V_F categories which are indicated on the type label. The part number is followed by a digit or letter, which stands for the V_F category of the device. Example: MEO260-12DA3 or MEK160-06DAD.

If several modules are connected in parallel to get a higher output current, only modules of the same V_F category should be used. There are, of course, exceptions to the rule: It is also possible to use two adjoining V_F categories; however, due to the saftey in operation, this should only be the exception. The current handling capability of the modules connected in parallel is calculated as follows:

$I_P \approx n \bullet I_n \bullet 0.8$
n = number of modules
I_n = current of one module (see table 3)
I_P = total current of the modules in parallel

Example: 3 modules MEO 260-12DA1 are connected in parallel:
The allowable continuous forward current I_{FAVM} at T_{VJ} = 65°C equals:
$I_P = 3 \bullet 262\ A \bullet 0.8 = 629\ A$

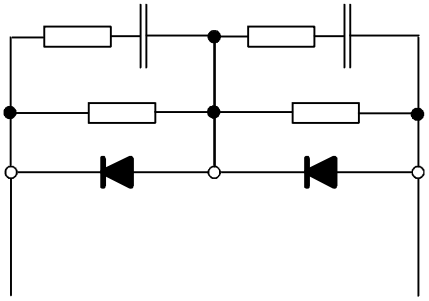


Fig. 20 Voltage sharing networks for FRED modules when its diodes are to be used in series

Series Connection

The series connection of FRED modules requires a static resistor circuit to equalize the different blocking currents of the diodes and a dynamic RC snubber circuit to equalize the different reverse recovery charges (Q_r) of the diodes. The calculation of these snubber circuits has to take into account a great number of conditions which can differ from application to application. The snubber circuits can only be optimized, if one is really familiar with these conditions.

The rough setup of these snubber circuits is illustrated in Fig. 20. What is of special interest is that, for the individual diode chips within a module, the selection in V_F categories also means that there exists a selection in I_{RM} and thus in Q_r.

A detailed databook (publication no. D94013DE) for the whole range of ultrafast diodes exists to help the design engineer to choose the right diode for his application.

Literature
[1] Heumann, K: Impact of turn-off Semiconductor devices on power electronics, EPE Journal, Vol. 1 (1991), No. 3, page 181 - 192

Input Rectifiers with Semifast Diodes for DC Link

Switching power semiconductors are used in inverter systems with DC-link. Due to high switching frequencies, harmonics and line distortion may be generated. It is important that new designs reduce these influences and fullfil the EMI filtering requirements according to i.e VDE 0871.

Input rectifiers have to charge the DC link capacitor in an inverter system with a highly constant DC voltage. If there is no request for feeding back energy to the mains, rectification of the AC voltage is mostly done by using uncontrolled single- or three phase rectifier bridges. The peak current level when loading the capacitor during switching on the system must be limited to incritical values for the input rectifier. This can be realized applying:

- NTC-resistors connected to the input rectifier. That, however, makes sense only for low power applications.
- Using a starting resistor either on the AC- or DC side which for continuous operation must be shorted to reduce losses and heat dissipation and to increase the efficiency. Very often the shortcircuit of the resistor is done by mechanical relais with a limited lifetime.
- The better way to load the DC-link capacitor is by using half controlled rectifier bridges type VVZ which are available for currents up to 175 A and voltages up to 1600 V.

When using half controlled rectifier bridges the soft start is achieved by slowly increasing the trigger angle for the bridge thyristors thus limiting the charging current for the DC link capacitor. During normal operation and after having reached the full wave control the thyristors operate like diodes.
As all cathodes of the thyristors have the same voltage potential as shown in Fig. 1a, triggering of the thyristors is easy to realize by using one impuls transformer only. Since two thyristors need a positiv triggerpuls during the reverse time it is recommended to use only triggerimpulses nearly to factor >2 of the I_{gt} -value given in the datasheet in order to avoid a high increase of the reverse current thus resulting in an increase of the blocking losses, too. Other softstart facilities using mechanical devices with a limited lifetime are not necessary.

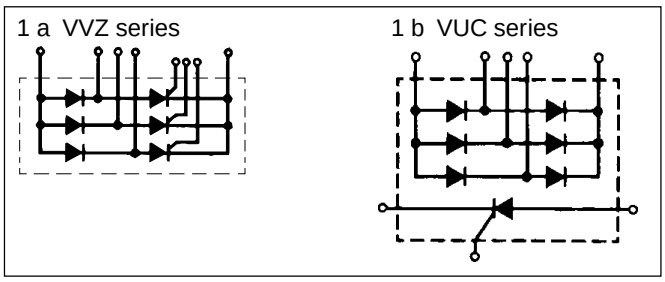


Fig. 1 Circuit of two different input rectifier bridges

For applications with a softstart resistor as mentioned above, a modul Type VUC (Fig. 1b) with a non controlled rectifier bridge including an integrated soft start thyristor is recommended. This module is available for 28 A and 39 A with voltages up to 1600 V.

The softstart will be realized with a load resistor placed in the positive outline of the input rectifier. This resistor limits the inrush current for the rectifier to uncritical values. When the DC-link resistor has reached its maximum charge the soft start thyristor in parallel to the resistor will be triggered thus shortcircuiting the resistor. Using this technology mechanically operated relais are replaced by an electronic switch with almost unlimited lifetime. The gate triggervoltage for the thyristor will be easily formed through a transistor circuit with impuls transformer using the DC link voltage. The thyristor is designed to be operated continuously with the load current as per datasheet. As the thyristor is not operated under phase control conditions, problems concerning turn-off will not occur.

The input rectifier is equipped with semifast diodes and is therefore optimized for turn-off, resulting in a lower peak recovery current compared to non-optimized and normal rectifier diodes (Fig. 2). This behaviour has a direct influence on the design of the EMI filter network with its capacitors and inductivites of which the size and costs can be reduced.

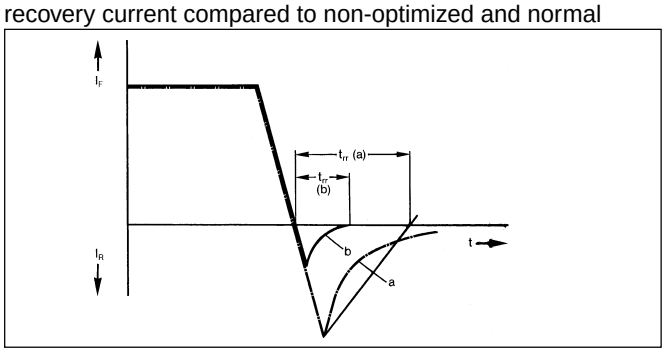


Fig. 2 Reverse revocery with standard rectifier a) and semifast rectifier b)

Fig. 3 and 4 show that turn-off optimized diodes have less snap-off behaviour compared to non turn-off optimized diodes or rectifier modules when the same EMI-filter will be used. The snapping behaviour is proportional to the peak recovery current, i.e the higher the I_{RM} rises the bigger the snapping behavour will be. These peaks always appear when the diode current commutate from one diode branche to the other branche of the rectifier bridge. During the commutation periode there always exists a short circuit for some nano-seconds. The rate of rise of the current (di/dt) in this case is only be limited by the stray inductances.

Due to the capacitor within the filter circuitry (necessary acc. to DIN 0871) the input voltage for the rectifier bridge became very “hard” thus resulting in high di/dt levels during commutation. The peak recovery current of the diode depends of the di/dt value and will be increased accordingly. To minimize this influence rectifiers should be equipped with diode chips which are optimized for short reverse delay time and small peak recovery current. The VUC modules are therefore equipped with such optimized diode chips.

Fig. 6 shows the influence of a non optimized vs. an optimized input rectifier built in a SMPS application for V_T = 208 V_{AC} (50 Hz) and I_{out} = 300 A_{AC} at V_{out} = 5.7 V. The Δ-marked line shows the voltage level vs. frequency of a non turn-off optimized VUC input rectifier module where the • - marked

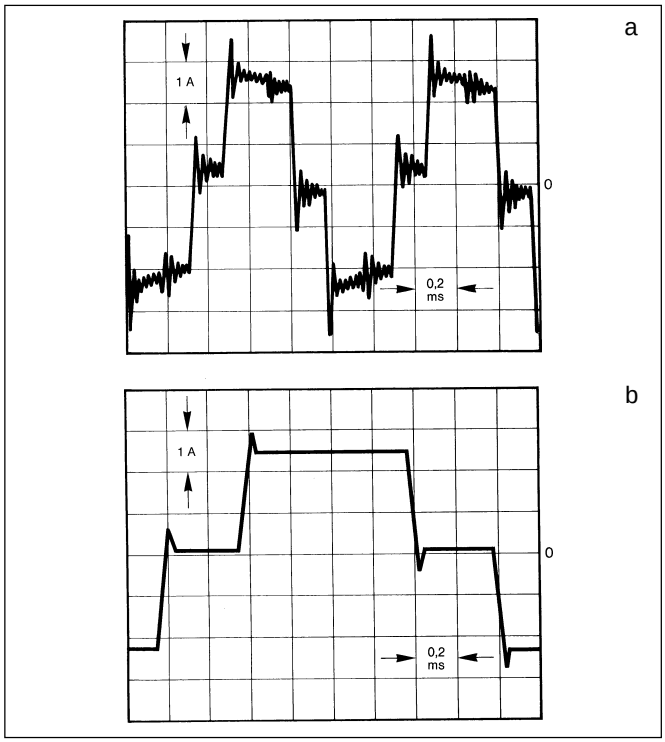


Fig. 3 a Input current with standard rectifier test point 1
b Input current with standard rectifier test point 2

line gives the results of a VUC rectifier equipped with optimized diode chips. The curves show that the noise level can be **reduced up to 15dB** when using reverse recovery optimized rectifiers. The circuit diagram for both cases is shown in Fig. 5.

The results clearly prove that the VUC module equipped with semifast diode chips shows a lower level of interference voltage thus resulting in the necessity of less filter equipment

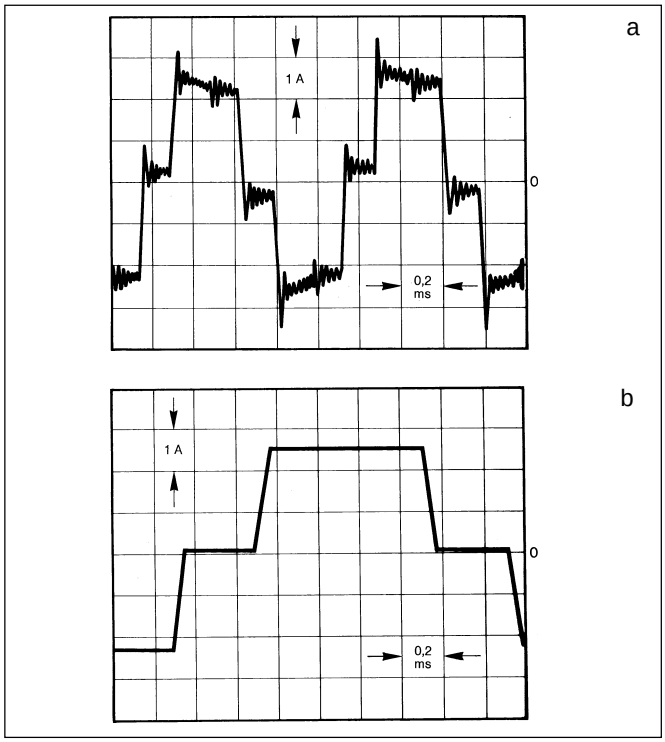


Fig. 4 a Input current with semifast rectifier test point 1
b Input current with semifast rectifier test point 2

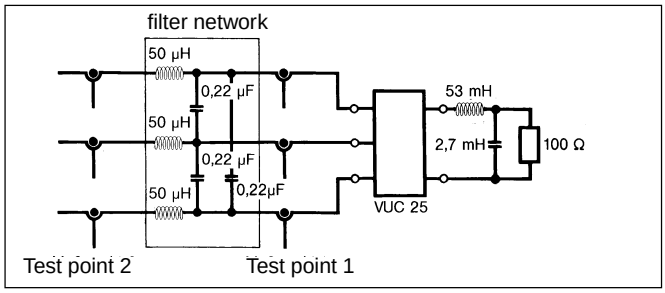


Fig. 5 Test circuit with filter network and VUC 25

compared to an input rectifier equipped with non optimized rectifier diode chips. This result will help the design engineer to design smaller, compact and less expensive power supplies systems.

Using the optimized input rectifier module type VUC with its integrated soft start thyristor or other non controlled rectifier bridges like a module type VUO 18 avoids the disadvantage

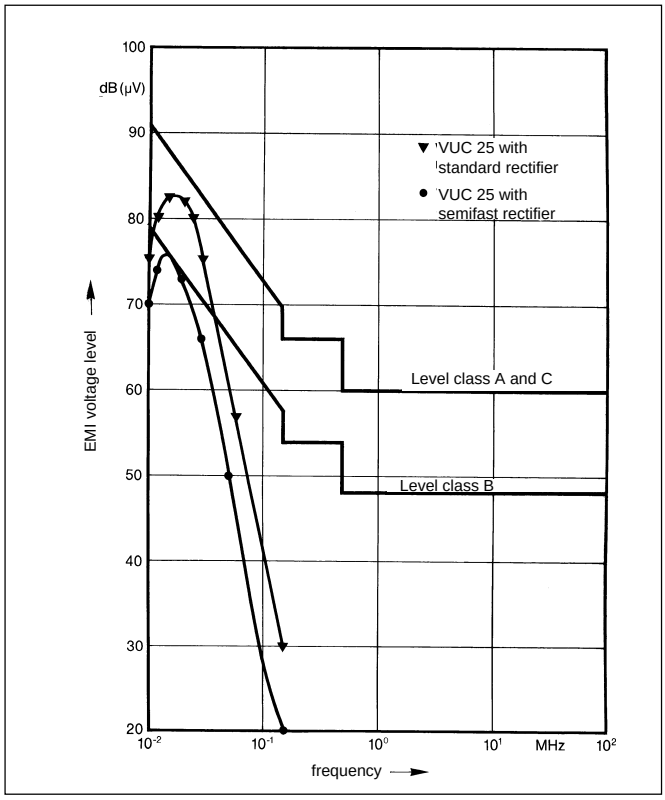


Fig. 6 EMI measurement at VDE 0871

of using many discrete components and allows to realize and produce electronic concepts at a cost effective and high quality level. IXYS is prepared to develop other rectifier bridges with semifast diodes and according to customer's request.

The noise level could again be **reduced by another 5 dB** when using rectifier bridges equipped with Fast Recovery Epitaxial Diodes (FRED) like modules type VBE (single phase bridge) or VUE (three phase bridge) which however are more expensive but may be necessary in some applications to fulfill the VDE or other standards.

New ISOPLUS247™ Power Package Features 2500V Internal Isolation

Revolutionary Approach Improves Thermal Conductance and Reliability

IXYS Corporation has introduced a new, isolated plastic encapsulated package for all types of discrete power semiconductors, one which promises to change the way power devices are attached to heatsinks. The new ISOPLUS247™ has an internally isolated mounting tab with a 2500V(RMS) isolation voltage rating. The package meets the standard JEDEC TO-247 outline and is intended for pressure mounting applications since there is no mounting screw hole. As can be seen in Figure 1, the usual copper lead frame has been replaced by a direct-copper-bonded (DCB) alumina substrate possessing both high thermal conductance and high electrical isolation (2500V).

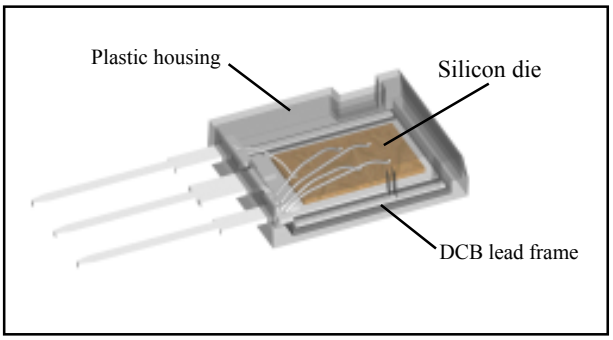


Figure 1: Cut-away view of the ISOPLUS247 package

There are multiple advantages to this isolated and hole-less packaging concept.

1. The dielectric breakdown voltage of the DCB is 6,000V although the package is only rated to 2500V(RMS) due to the creep and strike distances of the TO-247 outline;
2. The electrical insulation barrier is plastic encapsulated and therefore protected from the environment;
3. Very low, isolated thermal resistance junction-to-heatsink due to the use of DCB and only one non-soldered interface between the silicon chip and the heatsink;
4. Ease of assembly due to pressure mounting (no screws) and no additional isolation interface material required for mounting to a heatsink;
5. Increased temperature and power cycling capability because the thermal expansion coefficient of the silicon die matches that of the DCB;
6. Small chip-to-heatsink stray capacitance for reduced EMI/RFI emissions;
7. The DCB substrate can be etched like a PC board allowing for more circuit configurations than normally found in a non-isolated TO-247, e.g. epitaxial ultra-fast recovery diodes and Schottky connected common anode or in series, multiple diodes in series, MOSFET connected in series with a Schottky diode with or without an antiparallel diode.

The primary advantage of ISOPLUS247 packaging is the very low thermal resistance achievable in a rugged, high voltage, isolated mounting system. Table 1 compares the thermal resistance of a 55A/500V MOSFET chip in the ISOPLUS247 package (IXFR55N50) to the hole-less TO-247 version (IXFX55N50) when isolated with various interface material. Figure 2 shows the allowable current handling capabilities of the various mounting conditions.

Inspection of this table shows that depending upon the mounting technique, allowable output current can be increased by about 50% for the same junction temperature. Conversely, the chip can run up to 29°C cooler for the same operating conditions that translates into more reliable operation. Because there is such a potentially large decrease in junction-to-case thermal resistance, it may be possible to use a smaller chip for the same current, which would more than cover for the extra price (approximately $0.50 in production volumes) for the internal isolation.

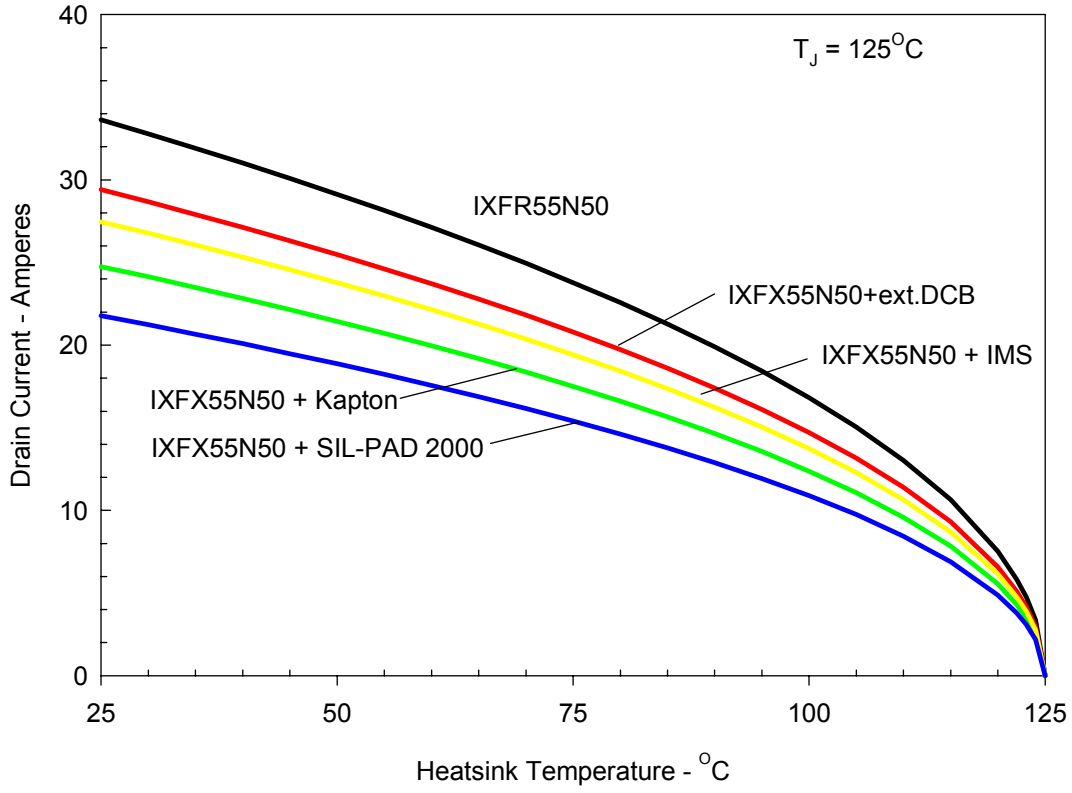
IXYS plans on introducing over 100 new part types in this revolutionary package during 1999. Initial product will consist of high power MOSFETs offering the industry's lowest on-resistance for this package outline. Future product will include IGBTs, IGBTs co-packaged with diodes, and ultra-fast and Schottky diodes.

Table: Performance Comparison of ISOPLUS247 IXFR55N50 to IXFX55N50 Mounted Using Various Interface Materials

Part Type	Isolation	Thickness	Isolation	R(th)js	Pd@ Tj=150C	Id @ Tj=150C	Tj @ Idc=15A
	Material		Voltage		Ts = 80C	Ts = 80C	Ts = 80C
		(mm)	(kV)	(K/W)	(W)	(A)	(C)
IXFR55N50	(Internal alumina DCB)	0.63	2.5	0.52	135	28.1	96
IXFX55N50	External alumina DCB	0.63	2.5	0.68	103	24.6	102
IXFX55N50	Kapton	0.05	4.5	0.96	73	20.7	112
IXFX55N50	IMS	0.13	6	0.78	90	23.0	105
IXFX55N50	SIL-PAD 2000(TM)	0.38	4	1.24	56	18.2	125
IXFX55N50	Softface(TM)	0.127	0	0.61	115	26.0	125

SIL-PAD is a trademark of Bergquist Co.

Figure 2: Graphical comparison showing the current handling capability of the ISOPLUS247 IXFR55N50 MOSFET vs the IXFX55N50 MOSFET as a function of heatsink mounting conditions.



IXYS

Technical Application

Combining the Features of Modules and Discretes in a New Power Semiconductor Package

by Andreas Lindemann IXYS Semiconductor

Abstract

A new package for power semiconductors has been developed: Power semiconductor chips are soldered onto a DCB ceramic substrate together with a lead frame with up to five pins. Subsequently chips and DCB are covered by molding compound. This packaging method combines the technologies of module and discrete assembly. Thus the resulting component provides a combination of the characteristics of both families of devices:

The new components are internally isolated from the heatsink they will be clamped onto. The pins are soldered into a printed circuit board; any circuit with an adequate number of pins can be incorporated in the package, using any kind of chip - such as MOSFETs, IGBTs, thyristors, diodes - and any topology. The pinouts are defined according to the requirements of electrical circuit design - for example avoiding current loops -, which - together with the very compact volume of the package - faciliates a low inductive design of power section.
Designing scalable power sections for a broad range of nominal power is easy due to the possibility of connecting devices in parallel. Reliability is expected to be comparable to modules' because of the matched thermal expansion coefficients of silicon chips and DCB ceramic substrate they are soldered onto.

These features described in this paper make the new family of components advantageously applicable in a variety of converters, such as for industrial and automotive drives or for power supplies.

1 Packaging Technology

The new package will be named ISOPLUS I4-PAC™ in the following. Its top and bottom view are shown in figure 1. Basically, it looks similar to conventional discrete components such as TO-247; however significant differences become obvious regarding the cross section in figure 2: The chips are not mounted on a solid metal leadframe, but on a DCB substrate [1]. It consists of a ceramic substrate with copper layers bonded onto its top and bottom side.
The bottom copper, used to transfer the operational power dissipation to the heatsink, is visible in the package's bottom view figure 1. The ceramic isolates it from the top copper layer, which may be structured corresponding to a printed circuit board as visible in figure 2. The top copper carries the chips, whose upper side is wire bonded towards the DCB pattern and the pins.

To provide electrical and mechanical protection, this subassembly is transfer molded, thus creating the typical black plastic package.

Two versions of the package with different pin distances have been successfully introduced. Their outlines are shown in figure 3. Height and length correspond to TO-247, width to TO-264 industry standard packages.
The experiences gained by IXYS' proprietary DCB production and discrete assembly, together with manufacturing the already introduced TO-247 like ISOPLUS I4-PAC™, [2] have helped to install the assembly process.

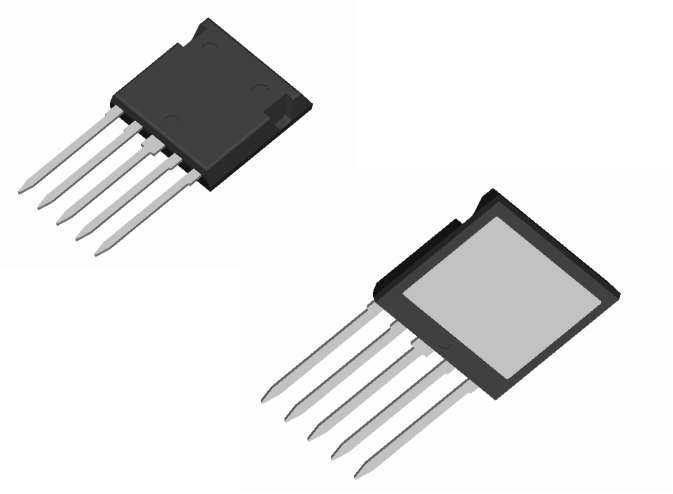


Fig. 1 Top and bottom view of five pin version

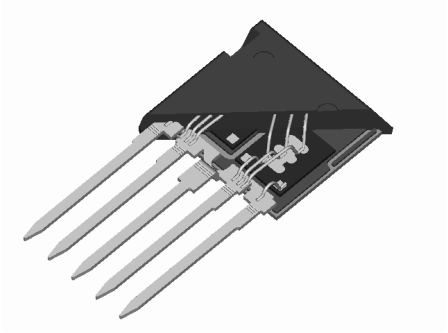


Fig. 2 Cross section of five pin version

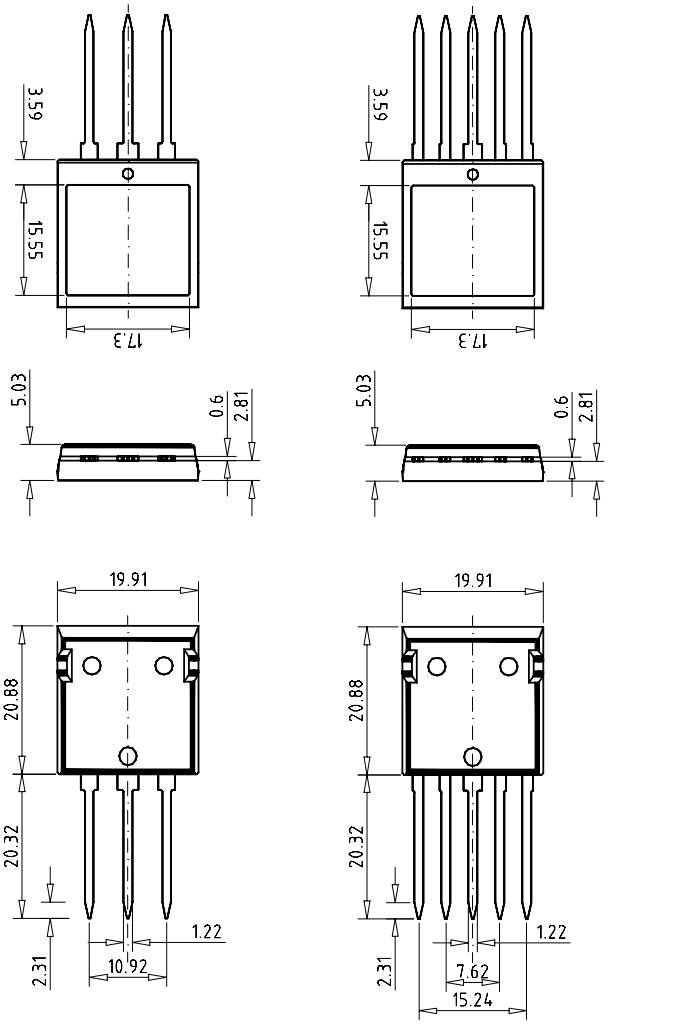


Fig. 3 Dimensional drawing of three pin (left) and five pin (right) version

The construction as described offers several benefits to the user of the components:

- A large variety of topologies with a all kinds of power semiconductor switches can be incorporated.
- The pinout can be defined in an electrically favourable way.
- The power circuit is internally isolated from the heatsink.
- A heatsink with an appropriate geometry permits to obtain a creepage distance between pins and ground of more than 6mm without additional measures.
- Standard mounting processes can be used:
  The pins are soldered into a printed circuit board.
  The package is simply directly clamped onto the heatsink with an industry standard spring [3], generally using some thermal compound to achieve a good heat transfer between the package and the sink. This mounting procedure allows considerable savings, because no external isolator is required.
- High reliability is achieved due to the corresponding thermal expansion coefficients of silicon chips and DCB substrate.

The following section 2 gives more details on several products with reference to the general features previously outlined. Section 3 shows their significance in exemplary applications.

2 Topologies, Components

This section presents some components in ISOPLUS I4-PAC™ package recently developed or currently under development. Of course there is a variety of further possibilities. Numbering of the pins as used in the following is shown in figure 4.

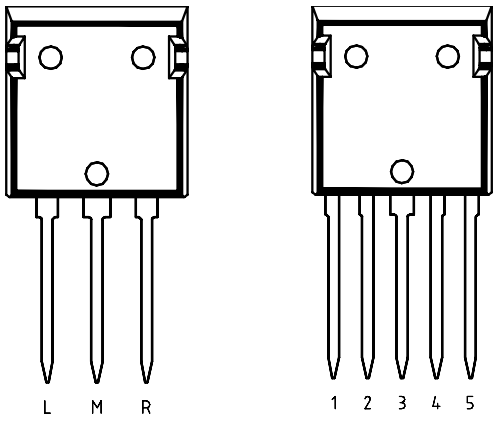


Fig. 4 pinout of three pin (left) and five pin (right) version

2.1 Single Switches

Single switches can be manufactured using all types of power semiconductors and with three different kinds of pinouts:

- The three pin package - see figure 4 (left) – will be used with the same pinout as TO-247 or TO-264 components, as a drop in replacement for the latters by isolated components with larger chips or smaller footprint respectively.
- A high voltage version will be realized based on the five pin package, omitting pins and thus enlarging the strike and creepage distances to the required length - see figures 4 (right) and 5. Please also note the position of the gate besides the source or emitter terminal, which is layout friendly and will increase noise immunity.
- A high current version will be realized with the five pin package, paralleling two pins each in the main current path - see figures 4 (right) and 6.

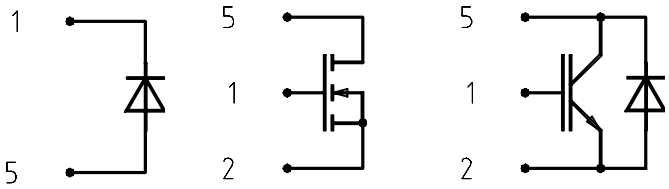


Fig. 5 high voltage single switches with diode (left), MOSFET (center) or IGBT with diode (right)

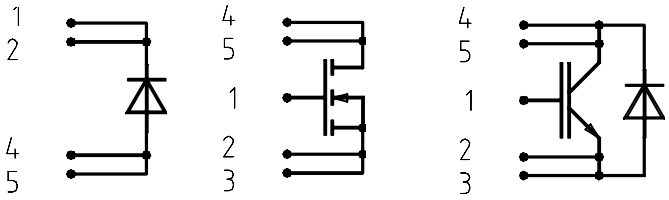


Fig. 6 high current single switches with diode (left), MOSFET (center) or IGBT with diode (right)

Table 1 gives basic ratings of exemplary single switch ISOPLUS I4-PAC™ package.

2.2 Phaselegs and Choppers

The five pin package can incorporate a complete phaseleg using MOSFETs, IGBTs with free wheeling diodes or thyristors respectively as shown in figure 7.

Please note the features

- small current loop between plus (3) and minus pin (2), thus low inductance

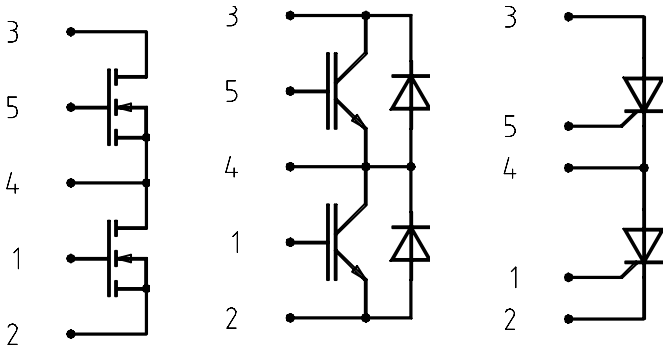


Fig. 7 Phaselegs with MOSFETs (left), IGBTs with diodes (center) or thyristors (right)

- neighbouring gate and source, emitter or cathode pins respectively (5 and 4, 1 and 2) for easy and noise immune drive

which enhance user friendlyness of these components above the market standards known from discrete components.

Of course, boost- and buck choppers can be generated based on the phaselegs, replacing one transistor by a diode. However, the possibilities even go further, because the structurability of the DCB as explained in section 1 permits to introduce a series connected and thus exceptionally fast free wheeling diode. As examples, this kind of boost and buck choppers with MOSFETs and IGBT are shown in figure 8.

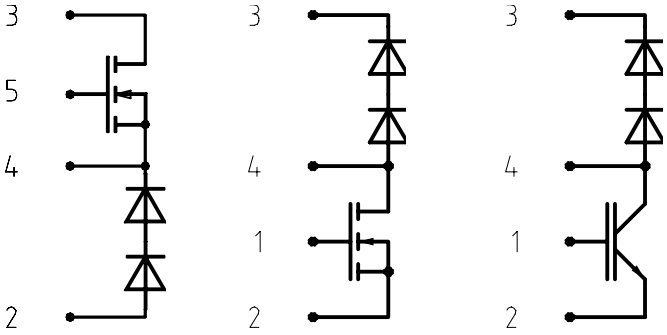


Fig. 8 Buck chopper with MOSFET (left), boost chopper with MOSFET (center) and IGBT (right), all with series connected free wheeling diodes

Please additionally note, that all bridge configurations - phaseleg, boost and buck choppers with the different types of chips - have the same pinout.

This faciliates the designers' layout work and enhances the flexibility to use printed circuit board layouts several times for different purposes.

Table 1: single switches in ISOPLUS I4-PAC™

Name	Type	Voltage rating	Current rating	Pinout, see fig. 4
IXFF24N100	MOSFET	U_{DSS} = 1000 V	I_{D90} = 17 A	G → L, D → M, S → R
IXBF9N160	BIMOSFET	U_{CES} = 1600 V	I_{C90} = 5 A	see fig. 5 (right)
IXBF40N160	BIMOSFET	U_{CES} = 1600 V	I_{C90} = 18 A	see fig. 5 (right)
IXDF30N120D1	IGBT + diode	U_{CES} = 1200V	I_{C90} = 32 A	G → L, C → M, E → R

In table 2, again basic ratings of exemplary phaseleg and chopper components in ISOPLUS I4-PAC™ package are given.

Table 2 phaselegs and choppers in ISOPLUS I4-PAC™

Name	Type	Voltage rating	Current rating	Pinout, see fig. 4
FMM75-01F	MOSFET phaseleg	U_{DSS} = 100 V	I_{D90} = 50 A	see fig. 7 (left)
FDM21-05QC	MOSFET buck	U_{DSS} = 500 V	I_{D90} = 15 A	see fig. 8 (left)
FMD21-05QC	MOSFET boost	U_{DSS} = 500 V	I_{D90} = 15 A	see fig. 8 (center)
FID35-06C	IGBT boost	U_{CES} = 600 V	I_{C90} = 25 A	see fig. 8 (right)
FCC21-08io	thyristor phaseleg	U_{RRM} = 800 V	I_{TAVM90} = 21 A	see fig. 7 (right)

Table 3 rectifiers in ISOPLUS I4-PAC™

Name	Type	Voltage rating	Current rating	Pinout, see fig. 4
FBO16-08N	single phase	U_{RRM} = 800 V	I_{FAVM90} = 16 A	see fig. 9 (left)
FUO22-08N	three phase	U_{RRM} = 800 V	I_{FAVM90} = 22 A	see fig. 9 (right)

2.3 Rectifiers

Another obviously advantageous topology in the ISOPLUS I4-PAC™ package is a single or three phase rectifier as shown in figure 9 and rated in table 3. Again an application friendly pinout has been achieved with the AC pins being separated from the DC pins.

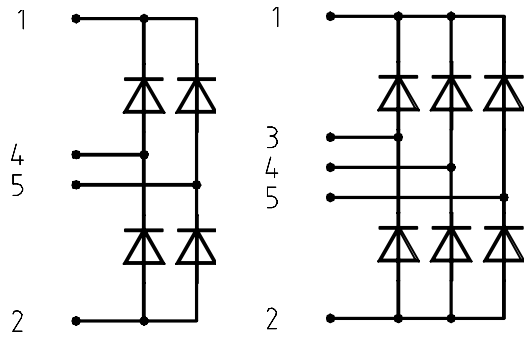


Fig. 9 single (left) and three phase rectifier (right

3 Applications

Some typical applications of ISOPLUS I4-PAC™ components with topologies and using components as desribed in section 2 are discussed in the following:

3.1 Industrial and Automotive Electrical Drives

Self commutated converters for AC drives use phaseleg configurations as shown in figure 7 (left and center). This means, that a very compact power section for an AC drive can be built, using three ISOPLUS I4-PAC™ components as listed in table 2. The power range can easily be enlarged by parallelling several components without the penalty to thus increase the low stray inductances between printed circuit board and chips, which is avoided by the phaseleg topology.

Switched reluctance drives require several boost and buck components according to figure 8 and table 2, DC drives one boost or buck chopper or a thyristor bridge according to figure 7 (right) and table 2.

Proceeding and features using ISOPLUS I4-PAC™ components will be the same as described for AC drives. In industrial drives, the inverter bridge may be complemented by a brake chopper - again see figure 8 and table 2 - and a single or three phase rectifier - see figure 9 and table 3. The advantages of this kind of converter - brake - inverter power stage using ISOPLUS I4-PAC™ components compared to standard discrete solutions are obvious - such as lower design and mounting expense, better operational behaviour and increased reliability.

Components like FMM75-01F are aiming at a different kind of electrical drives, mainly in vehicle applications: The ISOPLUS I4-PAC™ components may contribute to optimize automotive auxiliary drives with adaptable nominal power particularly for the new 42V supply and drives in battery supplied vehicles.

3.2 Power Supplies and Power Factor Correction

Figure 9 and table 3 deal with single and three phase rectifier components in ISOPLUS I4-PAC™ package; they can be used in a variety of power supplies.

A recent trend in power supply technology leads to power factor corrected rectification. This is partially due to the standards [4] [5], limiting the harmonic distortion of mains input currents, but additionally this topology offers the benefits to provide a wide input voltage range and to gain the highest amount of active power out of a plug with a given fuse. Due to the availability of ICs incorporating the control functions - such as [6] -, single phase PFC rectifiers can be built up in a simple and cost effective way. Their power section consists of a single phase rectifier in series with a boost converter [7].

While this topology can advantageously be integrated into a power semiconductor module for nominal powers above some 1kW, mainly discretes
have been used for lower power levels. However part count and again mounting effort is high for conventional discrete solutions. This can be avoided using two Isoplus ISOPLUS I4-PAC™ components - a single phase rectifier such as FBO16-08N according to figure 9 (left), table 2, and a boost chopper such as FMD21-05QC or FID35-06C according to figure 8 (center or right), table 2. The chopper consists of a MOSFET with low gate charge or a fast IGBT and two series connected

fast diodes representing the free wheeling diode with a reverse recovery behaviour outperforming single chip solutions [8] [9], which is particularly important for the switching frequencies of 50kHz to 100kHz typically used. The user friendly pinout of both components leads to a current flow avoiding wire crossings on the printed circuit board.

4 Conclusion

A new family of power semiconductor components in a recently developed package has been presented. The package combines an outline comparable to discrete components with features of multi chip modules, such as isolation from the heatsink and the capability to integrate a variety of circuits. Topologies have been suggested and power semiconductor components have been rated; typical applications have been discussed.

The features of the new packaging concept make expect a broad use of the components belonging to the new ISOPLUS I4-PAC™ product family in existing and emerging applications.

References

[1] A. Neidig: Neue Montagetechnik für Leistungsmodule; Mikroelektronik, Vol. 5, Issue 2, Fachbeilage Mikroperipherik, 1991

[2] M. Arnold, R. Locher: The Revolution in Discrete Isolation Technique; PCIM Europe, Issue 3/1999

[3] D. Grafham: Cutting-Edge Moundown Methods for Discrete Semiconductor Power Packages Boost Performance and Cut System Cost; PCIM Conference, Nürnberg 1998

[4] IEC61000-3-2: 1995; /A1: 1997; /A2: 1998

[5] IEC61000-3-4: 1998

[6] P. Todd: Boost Power Factor Corrector Design with the UC3853; Texas Instruments, 1999

[7] T. Schneider, W. Chrystowski: A New Power Stage for Boost Converters - a Perfect Match for PFC Controller ICs; PCIM Conference, Nürnberg 1993

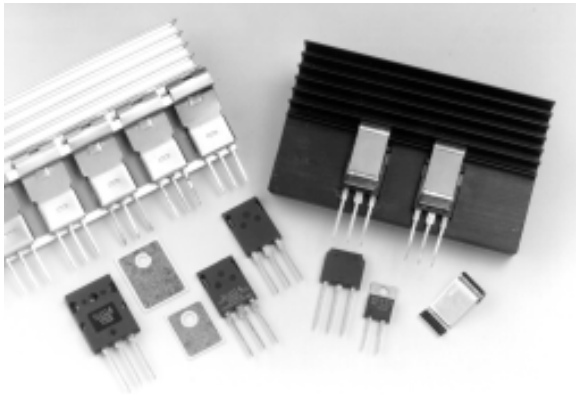
[8] J. Lutz et al.: Applikationshandbuch IGBT- und MOSFET-Leistungsmodule; Hrsg. v. P. Martin, Verlag Isle, Ilmenau, 1998

[9] B. Rivet: Dioden für Spar-PFC-Schaltungen; Design\Elektronik, März 1999

New Packages for Pressure Mounting

APPLICATION BRIEF AB-9801

Prepared by Ralph E. Locher



Introduction

The use of pressure to mount discrete power semiconductor packages to heat sinks has been rapidly growing for many reasons. When properly executed, it has proven to be a cost effective technique and has been shown that it can improve the overall performance of the discrete power semiconductor. In recognition of this trend, IXYS has brought out new discrete packages housing power MOSFETs, IGBTs and FREDs to further enhance the overall performance of the equipment using these parts. Examples of pressure mounted packages and spring clip assemblies are shown in the picture on the left.

This application brief will discuss the advantages of these new packages and their mounting considerations.

Pressure Mounting Trends

The use of spring clips and bars to secure TO-220, TO-247 and TO-264 parts to a heatsink is not new. Screwing these parts to a heatsink seems easy but suffers from the following disadvantages:

1. Their use is laborious because only one part can be mounted at a time and each screw must be accompanied by a lock or spring washer plus a flat washer to distribute the force from the screw head.
2. Torque limiting screw drivers must be used so as not to damage the silicon chip within the package or the interface pad if used.
3. Self-tapping screws should not be used due to the wide variance in applied pressure so that either the heatsink must be drilled and tapped or an additional nut will be required to secure the screw.
4. The popular discrete packages mentioned above all suffer from having only one screw hole so that the screw has a tendency to lift up the non-secured end resulting in increased case-to-sink thermal resistance R(th)cs.
5. Finally new specifications on creep and strike distances to meet the safety standards of various safety agencies increases the difficulties to using screws in mounting these packages to grounded heatsink surfaces.

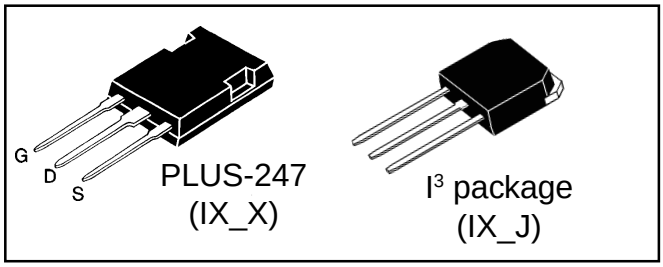
Pressure mounting presents solutions to these disadvantages as follows:

1. Elimination of the screw and associated hardware facilitates agency approval;
2. Springs apply pressure directly over the silicon chip to decrease R(th)cs;
3. Bar springs can be used to gang mount multiple devices;
4. Hardware is minimized;

New Pressure Mounted Packages

As pressure mounting comes into its own, IXYS has brought out two new packages designed to take advantage of this trend. They are: a) the PLUS247™ package, also known as the 'hole-less' TO-247 but should have been called the 'whole' TO-247; and b) the leaded TO-268 package, also known as the I^3PAK. Their package designations are the letters 'X' and 'J' respectively and are shown in the following illustration as well as in the picture above.

The major advantage of these new packages is that they allow



the semiconductor manufacturer to completely fill up the package with more silicon for maximum power efficiency. For example, in the PLUS247 package, IXYS can now offer 500V HiPerFET™ MOSFETs with an Rds(on)=0.08 Ω (IXFX55N50) or a 600V/75A rated IGBT with a companion FRED diode (IXGX50N60BU1). Likewise for the J package, one can now insert a 500V MOSFET with an Rds(on) of 0.15Ω (IXFJ32N50) in place of a pressure mounted TO-220. Indeed the driving force for the J-package was the recognition that it was the easiest, high power package to use to upgrade power conversion equipment now using TO-220 packages or other equipment with limited headroom above the PC board. Additionally it is the preferred package for high voltage since its strike distance between pins is 3.7mm (0.145"), 33% greater than the TO-247, and its creep distance has been increased to 4.5mm (0.177"), partly enhanced by a barrier ridge between each pair of pins.

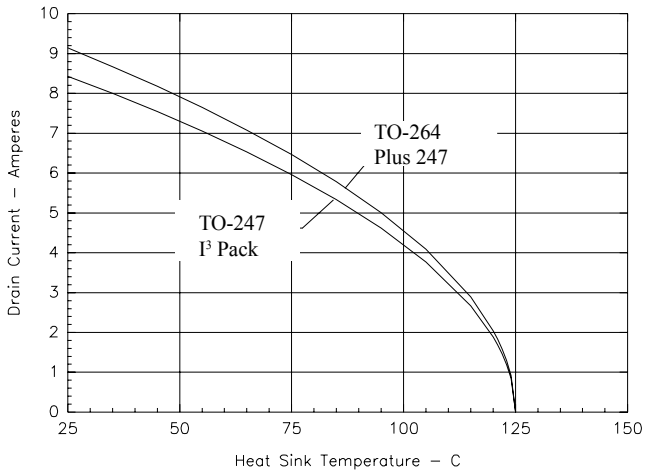


Figure 2: Comparison of allowable current ratings for a 1000V/12A rated MOSFET chip in four different packages.

All power semiconductors are limited by junction temperature so that their maximum power output is only as good as the overall thermal design of the equipment. The total thermal resistance junction-to-ambient R(th)ja can be subdivided into three components, namely the thermal resistances between junction-to-case, case-to-sink and sink-to-ambient. In equation form:

$$R(th)ja = R(th)jc + R(th)cs + R(th)sa$$

As larger and larger silicon chips have been encapsulated into discrete housings, the importance of R(th)cs has grown because it has not decreased at the same rate as R(th)jc. R(th)cs is a function of many factors, as explained in the next section, but one important contributor is the area of the heat flow path. It turns out that the PLUS247 package has the same tab area as the TO-264 package, so that they share the same value for R(th)cs of 0.15K/W. As shown in Figure 2, this results in an immediate increase of about 10% in current handling capability for the same size silicon chip housed in the standard TO-247 package. The smaller J package shares the same value as the TO-247.

Pressure Mounting Considerations

R(th)cs is a function of many factors, such as flatness and surface preparation of both the discrete package and heatsink, type of insulating washer and or thermally conductive compound, mountdown pressure and, as already mentioned, the area of the heat flow path. The best conducting contact is metal to metal but there are always air voids in a dry contact due to surface finish. Depending upon the thermal and electrical requirements of the system, the packaging engineer will choose a thermal grease and/or some form of lubricating or insulating washer to fit between the device and the heatsink to eliminate air voids.

The requirements and preparation of the mounting area on the heatsink for pressure mounted parts depends upon the selection of the thermally conducting compound or washer.

Thermal Grease

Thermal greases are effective in reducing R(th)cs where the maximum air gap between surfaces is less than 25μm (0.001”). This means that extruded aluminum heatsinks will require some surface milling for housings larger than TO-220 because the nominal flatness specification is 4μm/mm (0.004”/in). To minimize the effects of heatsink finish, the heatsink mounting surfaces should be flat within 0.001”/in and the roughness should not exceed 125 microinches.

IXYS recommends Dow Corning 340 heatsink compound or Berulub FZ1E3 (Bechem, silicone free) , which contains zinc oxide particles to reduce R(th)cs. R(th)cs of a ‘greased’ interface is typically 30-50% less than a dry joint and varies less with pressure. The grease should be rolled onto the heatsink surface to thickness of 30 - 50μm (0.001” - 0.002”). A range of 150kPa - 300kPa (20-40 PSI) is usually sufficient to ensure good thermal conduction.

Thermally Conductive Pads

Today the packaging engineer has a literal cornucopia of pads to choose from to meet his needs of isolation voltage, environmental restrictions, moisture and thermal conductance. Reference 1 has a more thorough comparison of various materials used in these pads. Mica washers coated with thermal grease on both sides provide a very low cost, good thermal conductive joint with high dielectric strength. Its major disadvantage is its brittleness and susceptibility to puncture by burrs on either the heatsink or semiconductor package. A better choice to meet high isolation voltage requirements are ceramic washers because they combine high dielectric strength with good thermal conductivity. However, they are also brittle and require thermal grease to fill in air voids between the interface layers.

IXYS manufactures its own Direct-Copper-Bonded (DCB) ceramic substrates for its multitudinous power module families of products. It has developed DCB pads for the TO-247 and TO-264 packages, which can be bought individually. Again either thermal grease or a non-insulating grease replacement material such as Q-Pad 3® from Bergquist or Thermstrate® from Power Devices. Both materials conform to the mating surfaces when exposed to modest heat and pressure to achieve relatively low thermal resistance.

There are many objections to the use of thermal greases due to their messiness, incompatibility with soldering systems, possibility of outgassing and drying out with time. There has also been much research work performed to develop ‘low pressure’ types of interface tabs, for which the power industry probably has to thank the IC industry for developing high speed digital products that require heatsinking. Consequently there is not only a very large selection of both insulating and non-insulating interface pads available on the market today from many different manufacturers but also new pads designed specifically for low pressure applications.

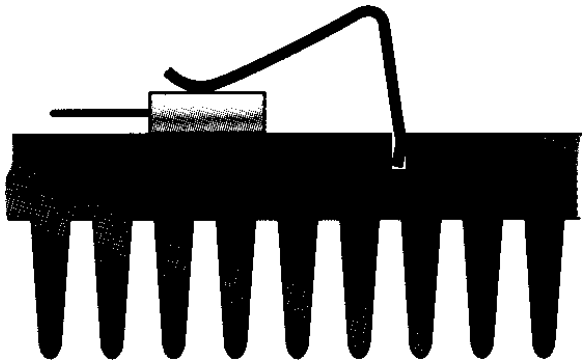
In theory the measurement of R(th)cs is simple but it has proven very difficult to duplicate measurements amongst different test labs. There are too many variables involved, including

type of package, heatsink flatness and finish, and the test environmental factors of time, pressure and temperature. Consequently today it is the exception to find graphs plotting R(th)cs vs. pressure for different washers and therefore the user must make his own side-by-side comparison of various materials in his equipment.

For low pressure mounting, Bergquist offers their Sil-pad 800-S® and 900-S®. Both Chomerics and Power Devices have pads that undergo a phase change and flow to conform to the mating surfaces. Pads with a pressure sensitive adhesive may also provide low R(th)cs at very low pressures.

Pressure Mounting Springs and Clips

As explained above, mounting pressure plays a key role in reducing R(th)cs. Mounting clips come in many different forms from the spring inserted into a slot on the heat sink (see illustration) to various U-shaped and saddle clips to spring bars to



Discrete part spring mounted to finned heatsink
(Drawing courtesy of Kunze Kuhlkorper GmbH).

hold down the semiconductor.

However, the typical spring clips today can only apply between 10 - 50N (2 - 10 lbs) of force, which equates to a range in pressure of 60kPa (8 PSI) to 300kPa (40 PSI) for the TO-220 to slightly more than one-half of this for the PLUS TO-247 package. It certainly helps that the force is centered over the semiconductor chip as illustrated in the drawing but the low pressures cited above emphasize the need to choose the appropriate thermal conducting materials.

IXYS epoxy molded packages can easily withstand pressures up to 2.27MPa (300PSI), achievable with screw mounting. The width of the spring should be about 80% of the package width and the contact area of the spring on top of the package adjusted so as not to exceed that limit.

List of Manufacturers of Thermally Conductive Materials

1. The Bergquist Co.
   5300 Edina Indeustrial Blvd.
   Minneapolis, MN 55439
   Tel: 612-835-2322
2. Power Devices, Inc.
   Thermal Interface Products Group[
   26941 Cabot Road, Bldg. 124
   Laguna Hills, CA 92643
   Tel: 714-582-6712
3. Chomerics
   6 Flagstone Drive
   Hudson, NH 03051
   Tel: 781-939-4453
4. Thermagon, Inc.
   3256 West 25th St.
   Clevaland, OH 44109
   Tel: 888-246-9050 or 216-741-7659
5. Kunze Kuhlkorper GmbH
   Postfach 1562; D-82036 Oberhaching
   Germany
   Tel: 089/613 2345

List of some Spring Clip Manufacturers

1. Thermalloy, Inc.
   PO Box 810839
   Dallas, TX 75381
   Tel: 214-243-4321

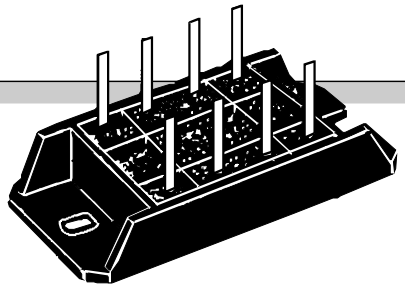
   UK office:
   Cheney Manor
   Swindon, Wiltshire SN2 2QN
   Tel: +44 1793-537861
2. Aavid Thermal Technologies
   One Kool Path
   Laconia, NH
3. EG&G Wakefield Engineering
   Components Division
   60 Audubon Road
   Wakefield, MA 01880
   Tel: 617-246-0874
4. Kunze Kuhlkorper GmbH
   Postfach 1562; D-82036 Oberhaching
   Germany
   Tel: 089/613 2345
5. Austerlitz Electronic gmbH
   Ludwig Feuerbach - Strasse 38
   90961 Nuernburg, Germany

References:

1. *A Comparison of Semiconductor Isolation Materials* by Kevin Hanson, available from the Bergquist Co.

Technical
Information 35

PFC Power Stage for Boost Converters



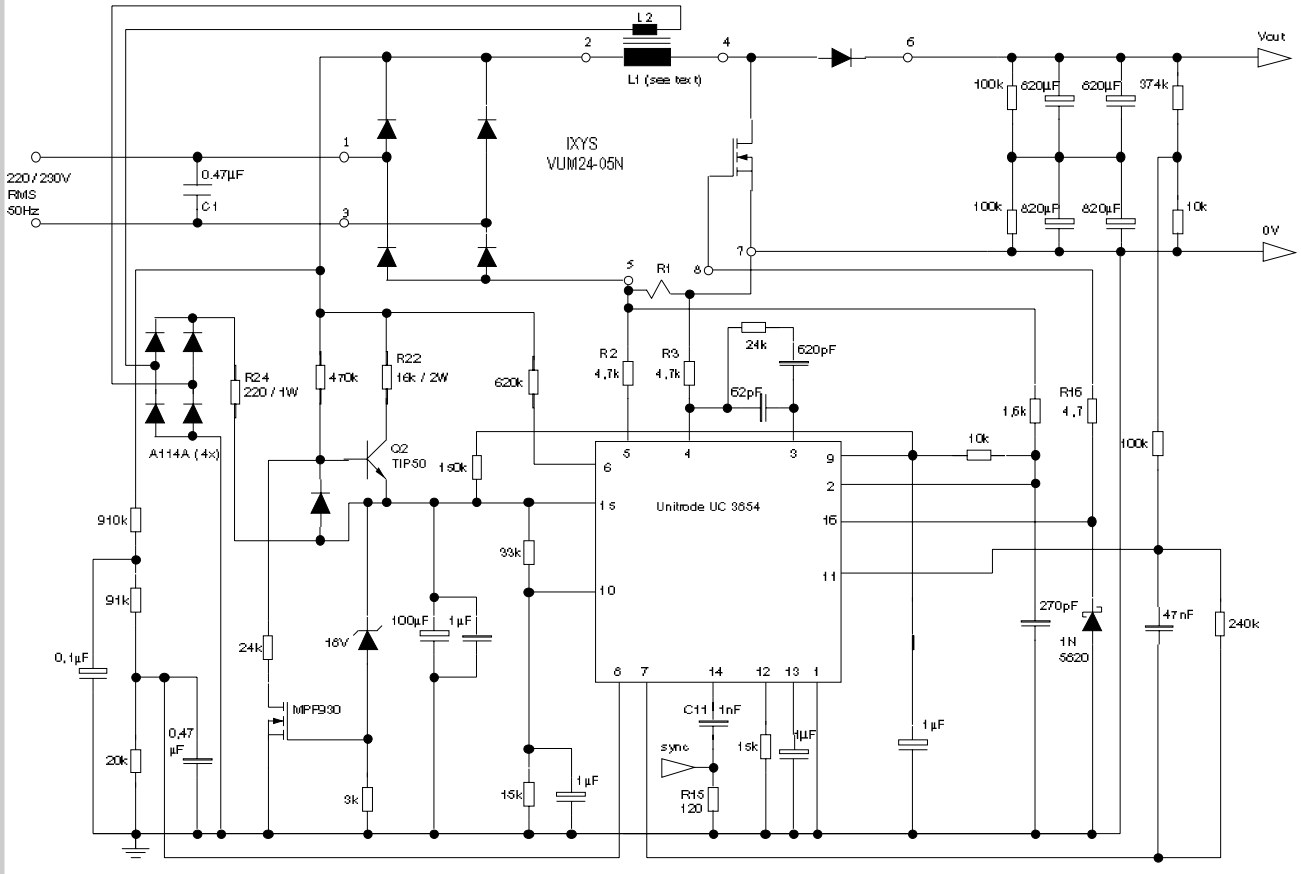


Fig. 1 Schematic of a complete 1.5 - 3 kW PFC system

The need for Power Factor Correction (PFC) - reduction of AC mains borne harmonics and improved utilization of the AC lines themselves - has been widely discussed for a number of years. Now a new power stage for boost converters is a perfect match for popular PFC Controller ICs. Permitting compact and reliable equipment designs, easy to engineer and manufacture, these products represent a real advance in the state-of-the-art of high frequency power conversion. The article describes in detail the electrical and mechanical development stages.

Introduction

The impending implementation of IEC Directive 555-2, compelling the adop-tion of such techniques in Europe, has stimulated a great flurry of design activity all over the Western World - either by Europeans who sell in their own markets, or by the Americans, Japanese and others anxious to sell goods in Europe.

Although PFC may be implemented successfully by several different power circuit architectures, including boost converters, buck converters or resonant topologies, the great bulk of design activity appears to centre around the standard boost converter configuration.

The major benefits of this topology:

- The output voltage is always higher than the peak input AC mains voltage so that energy storage is always at high voltage, enabling the use of a smaller output storage capacitors.
- The input current in a boost converter is not chopped, but is continuous with ripple at the PWM frequency. This results in lower RFI/EMI in the mains and facilitates the adoption of current mode control since the boost inductor current is the input current.
- The boost inductor protects the equipment, isolating it from high frequency mains borne transients.
- Current can be controlled over the full excursion of mains voltage and over the international voltage / frequency range.
- Semiconductor voltages are no greater than the output voltage plus switching transients.
- Easy to drive power switch, with its reference terminal (source or emitter) at 0 V potential.

Several semiconductor companies have developed and marketed specifically designed ICs that provide the necessary control and drive functions for the power stage of a boost converter implementing PFC. One of the most popular appears to be the Unitrode type UC3854. This device uses average current mode control to accomplish fixed frequency current regulation with excellent stability and low distortion. Operation is possible from 90-264 V_{RMS} without mains switching. The standards of line harmonics and distortion imposed by IEC 555-2 are handily met by a wide margin over this entire range.

Given all this activity on the IC front, it is interesting that until now no semi-conductor supplier has addressed the equally important power stage that forms an integral part of the boost converter. The power stage, consisting normally of an input rectifier bridge, a shunt power switch and the output boost diode, may of course be realized with discrete components (but then, so can the control function). However, there are significant benefits to be realized from implementing this power stage as single integrated power module.

- In a boost converter required to supply more than 1.5 kW from 220/240 V_{AC} mains, the paralleling of output switches becomes manda-tory, if TO-247 or smaller devices are used. While the paralleling of power MOSFET's is popularly considered "easy", symmetrical mechanical layouts and some degree of device matching are almost obligatory for reliable boost inverter operation. This is not always easy to accommodate when discrete components are specified. In the VUM-module, MOSFET chips from the same silicon wafer are specified for homogeneity of performance, and their internal layout on the module substrate is of course perfectly symmetrical.

The rest of this paper will describe the behaviour and quantify the perfor-mance of a boost converter consisting of an VUM 24 power module driven by a Unitrode type UC3854 PFC Controller IC. As will be seen, this design is able to operate with efficiency in the region of 95 % at power levels of 1.5 kW to 3 kW, with switching frequency of 100 kHz to minimize inductor and EMI filter size. Special gate drive enhance-ment circuitry is also described that dramatically reduces switching power losses.

Adaptation of the basic Unitrode design for 1.5-3 kW output power from 220/240 V_{AC} mains

The prototype circuit evaluated in this report was based on a Unitrode UC 3854 250 W evaluation board schema-tic adapted to drive a VUM 24 boost converter power module. The complete schematic is illustrated in Figure 1 (cover). Certain changes to the original were found to be desirable.

- The input inductor L1 in Figure 1 consisted of 55 turns of 2 mm ∅ enamelled copper wire wound on a MAGNETICS MPP Toroidal Core # 55438-AC. Over this primary was wound an additional 13 turns of 0.6 mm ∅ wire to furnish power to the auxiliary supply. Primary induc-tance L1 was measured as 918 µH, secondary inductance L2 = 68 µH. Although this inductance is far higher than that needed for 1.5 - 3 kW output at a switching frequency of 100 kHz, it was chosen such that operation at lower frequencies could be evaluated.
- Current sense resistor R_S (R1 on schematic) was of course much lower in value than the 0.25 Ω specified by Unitrode for 250 W operation. For initial runs at power levels up to 2.5 kW, a specially constructed resistor of 31.5 mΩ was used, but beyond this power level, 16.2 mΩ was found necessary to prevent unacceptable "sag" of the output voltage. The optimum choice of this resistor is well documented in the Unitrode literature.
- Associated with this resistor are the current loop resistors R2 and R3. These were increased from 3.9 kΩ to 4.7 kΩ. Once again, proper choice of these is covered in the Unitrode documentation.
- Current limit resistor R24 from the output of the auxiliary power supply bridge was found by trial and error to be optimum at 220 Ω/1 W. This relatively low value is required so that the power supply may furnish the substantial average current necessary to charge and discharge the gate capacitance of 2 size #7 MOSFET's (24 A/ 500 V) at 100 kHz.
- For the same reasons, series gate resistor R16 was reduced from 20 Ω to 4.7 Ω. This is the lowest value safe to use without the onset of potentially dangerous oscillation.
- The auxiliary power supply bridge rectifier was replaced by 4 discrete 1 A fast recovery rectifiers, since the original bridge ran **very** hot, even with Unitrode's specified R24 = 470 Ω. Because AC voltage input to this bridge is high frequency, fast recovery rectifiers are more appropriate.
- Start-up was facilitated by reducing R22 from 33 kΩ to 16 kΩ. Losses in this resistor are academic since once the circuit is running R22 is switched out by Q2.

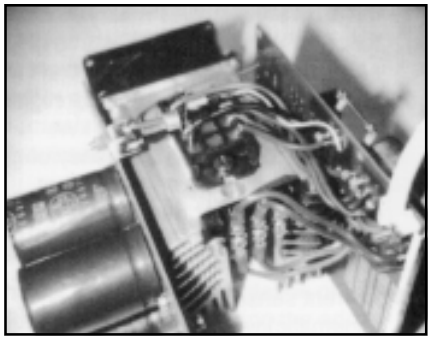


Fig. 2 VUM modul mounted on heat exchanger

Heatsink Thermal Calibration

To determine the thermal resistance of the heat exchanger on which the VUM 24 is mounte, the following procedure was adopted.

The module itself was centrally moun-ted on the machined top surface of a 10 cm x 6.5 cm x 7 cm deep aluminium semi-"sunburst" heat exchanger, itself cooled by an end-mounted 8 cm x 8 cm x 4 cm axial extractor fan (Fig. 2). The joint between the module and fin was thermally greased (Wake-field 120-2), and the module was torqued down to 2.2 Nm (M5 screws). A 1/8" ∅ hole was drilled through the heat exchanger central web at the module centre point, to accommodate the tip of a platinum resistance probe inserted from beneath.

Test current "I" shown in Figure 3 was set by adjusting V_{GS} until the VUM 24 was dissipating about 75 W. Stable operating conditions were assured by use of the existing PFC current sense resistor R_S as a negative feedback element for V_{GS} . Voltages across the FET, diode D1 and diode D2 were monitored with an accurate DC voltmeter, once equilibrium was reached after about 15 minutes.

I_{DC} = 9.10 A	V_{MOS} = 6.35 V
V_{D1} = 0.9 V	T_S = 43 °C
V_{D2} = 0.88 V	T_A = 19 °C

From these measurements, the ther-mal resistance of the heat exchanger is calculated:

ΔT = (43-19)°C = 24 K
P_{Module} = 9.1 A (6.35 V + 0.9 V + 0.88 V) = 74 W
$R_{thSA} = \Delta T/P$ = 24 K/74 W = 0.32 K/W

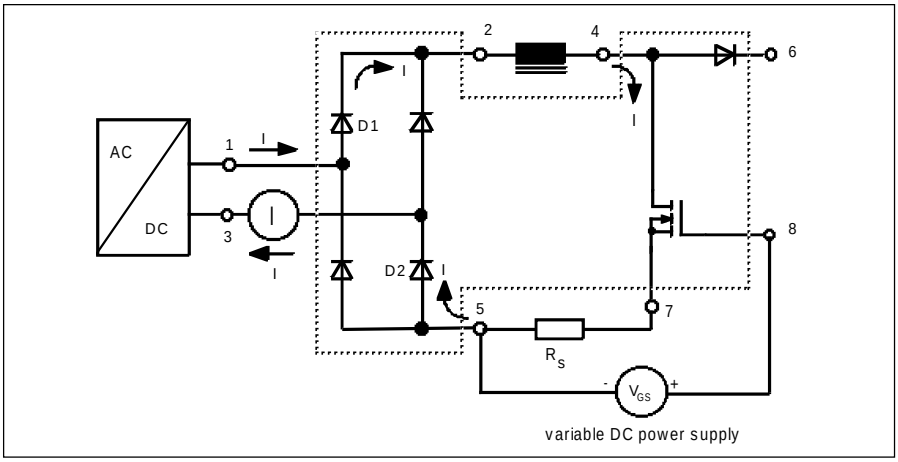


Fig. 3 Calibration circuit

Current Sense Resistor Calibration

Given that this PFC module assembly will eventually be operated at 3.5 kW input power (220 V_{RMS} x 16 A_{RMS}), the choice of an adequate current sense resistor is not easy. Conventional resistors in the 5-10 W range are bulky and not always low-inductive, so "custom-made" relatively non-inductive resistors were fabricated from 1.2 mm ∅ stainless steel welding rod. Two models were prepared (Fig. 4).

Estimation of the ohmic values of these resistors was then carried out at current levels approaching those pre-valent in the actual PFC circuit (Fig. 5).

Current was raised to approximately 10 A, voltage being monitored with a DC voltmeter.

2 cm model I = 10.08 A, V_S = 163 mV after 5 min. giving R_S = 0.163 V/10.08 A = 16.2 mΩ

4 cm model I = 10 A, V_S = 315 mV after 5 min. giving R_S = 0.315 V/10 A = 31.5 mΩ

The same technique was also employed to fabricate an AC mains current shunt.

Experience showed that use of a conventional ammeter to measure AC line current was not dependable, even although the ammeter concerned was an electronic RMS-responding DVM (Beckman # 3030). The principal problem seems to be associated with the very intense RF fields surrounding the PFC assembly, which was not shielded for these experiments. Meter readings, especially on AC current when the current is actually fed into the DVM (internal shunt), tend to be random and unpredictable, and may be

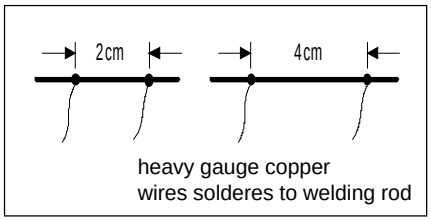


Fig. 4 Shunt models

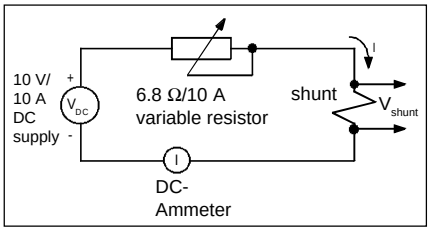


Fig. 5 Shunt calibration circuit

significantly influenced by meter placement or even the position of the human body nearby that acts as a kind of moving RF shield.

As a consequence, a current shunt was manufactured using the same welding rod as used for the PFC current sense resistors (Fig. 6).

This shunt may be used in conjunction with an RMS voltmeter (less sensitive to fields) or with an oscilloscope to visualize and measure the current directly. When

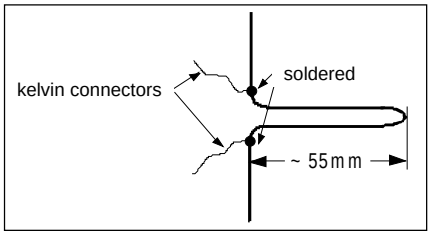


Fig. 6 AC-current shunt

fed with the SMPS/Rheostat arrangement used earlier for R_S calibration.

R_{Shunt} = 0.635 V/7 A = 0.091 Ω

For interest, its resistance was also measured at room temperature with a Marconi Wheatstone Bridge

R_{25} = 0.086 Ω

which is a 6 % difference, indicating the importance of calibration at or near normal operating temperatures.

Instrumentation

As mentioned earlier, the intense RF fields surrounding the PFC module tend to make accurate instrumentation extremely difficult. To establish a degree of confidence, several experiments were conducted. First, the same load banks as used with the PFC were run at 390 V_{RMS} 50 Hz, to establish known current levels using accurate RMS voltmeters and amme-ters. This procedure also permitted exact calculation of "hot" load resistances. Comparative data indicated that the Beckman # 3030 RMS respon-ding voltmeter can give reasonably accurate readings of RMS voltages at the PFC output, but that its ability to measure RMS output current is suspect. This meter can of course also measure DC (average) values of voltage and current without problems. Because of doubts concerning the accuracy of RMS measurements (necessary for the calculation of output power), analysis of the PFC output characteristics was undertaken with a 60 MHz oscilloscope (Tektronix # 453 A) and 50 MHz current probe (Tektronix # P6042). From this analysis, it is clear that the PFC output voltage is a DC level modulated by an extremely pure 100 Hz sine wave ripple voltage.

From this observation, knowledge of average and peak-to-peak ripple voltage permit the calculation of true RMS output and Form Factor (RMS/AVG). Theoretical relationship between RMS and average values for a pure-sine modulated DC level (Fig. 7)

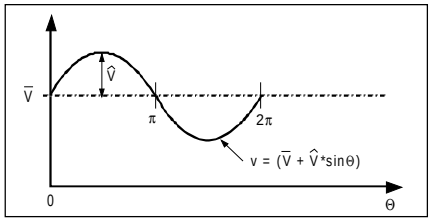


Fig. 7 Relationship between RMS and average value for a pure-sine modulated DC level

Load Configuration

Since one version of the Boost Converter power modules allow output power levels in excess of 3.5 kW (VUM 33 with semiconductor chips mounted on Aluminium Nitride Substrates), proper evaluation over the full power range presupposes a high power **variable** resistance load bank able to absorb up to 4 kW at 390 V_{DC} output. The "hybrid" load bank depicted in Fig. 8 permits full stepless control from 0 W to well over 3.5 kW at 390 V_{DC}. The variable control for the 2 x 60 W/220 V_{AC} lamps is itself a (linear mode) PFC, in that it forces the load current in the lamps to follow the voltage input! Its schematic is shown in Fig. 9. The (2 x 150 Ω) resistors must be switched in to maintain voltage sharing between the hot plate and ceramics oven, when the former is on its 1.5 kW setting.

A word of caution is in order. Although all these loads are nominally resistive, switch-off of the hot plate or oven in particular under load must be avoided at all costs, since destructive arcing is set up across the associated switch contacts due to inductance associated with the wiring.

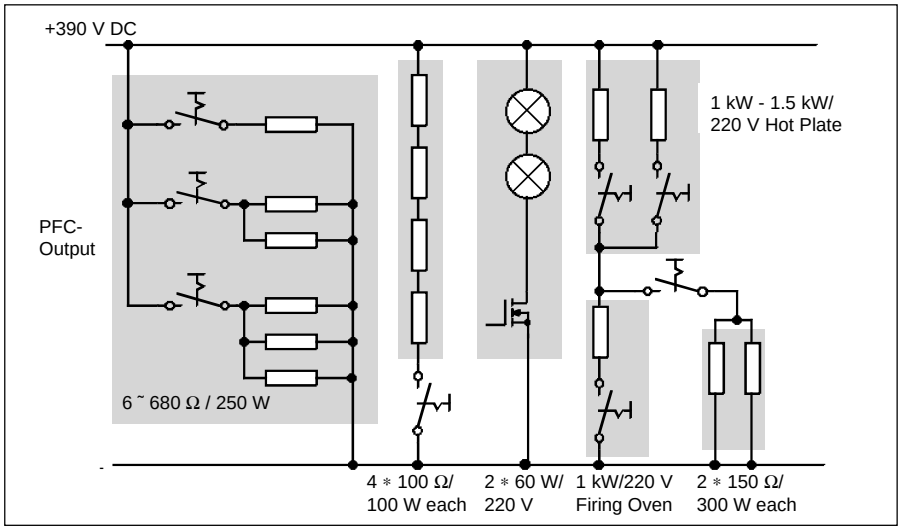


Fig. 8 Hybrid load bank

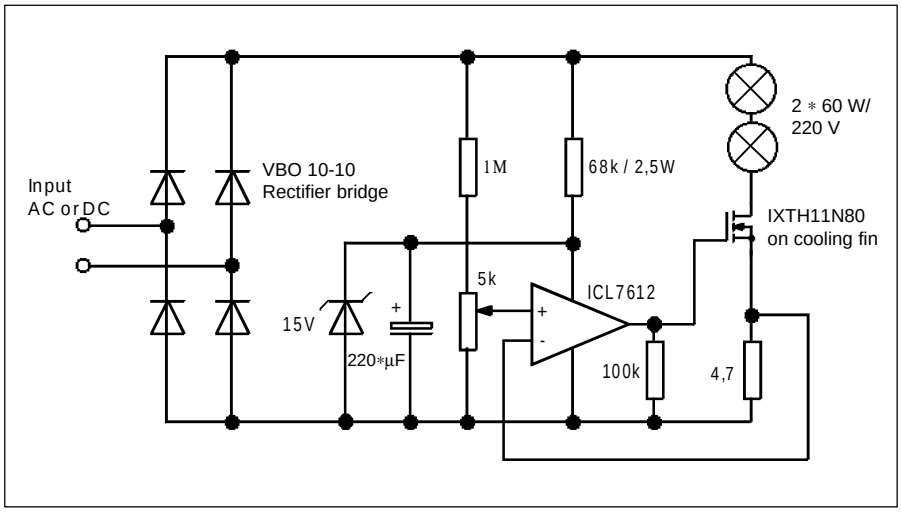


Fig. 9 Linear PFC for stepless load control

Operation of PFC unit at various power levels

The complete PFC unit, consisting of the modified Unitrode 250 W evaluation board minus its power semiconductors married to the VUM 24 Boost Converter Power Module, was operated at various power levels between 1.5 kW out to 3 kW. This was to ascertain functional behaviour, losses in the semiconductors and losses in the associated passive components and auxiliary equipment, thus establishing overall efficiency.

1. Nominal 1.5 kW out (R_S = 31.5 mΩ)

a) Input Power
Input voltage = 231 V_{RMS}
(Beckman RMS DVM)
Input current = 6.9 A_{RMS}
(Tektronix current probe)
giving Input power
P01 = (231 V x 6.9 A) = 1594 W

Note: As viewed on the oscilloscope, the input current waveform was a clean and distortion-free sine wave in phase with the mains voltage.

b) Output power
Output voltage = 360 V_{DC}
(Beckman RMS DVM) 366 V_{RMS}
Output current = 4.17 A_{RMS}
(Tektronix current probe) 4.11 A_{DC}
giving output power
(366 V x 4.17 A) = 1526 W

c) Thermal measurements
T_A = 19.8°C
(AOIP digital/Pt. Res. probe)
T_S = 36.3°C
(45 min stabilization time)
R_{thSA} = 0.32 K/W
(see calibration section)

Losses in semiconductors
$P_{SEMI} = \Delta T/R_{thSA}$ = 16.5 K/0.32 K/W = 52 W
giving losses in remainder of system
(1594-1526-52) = 16 W

These other losses include those in the sense resistor R_S, boost choke, auxiliary power supply, capacitors and cooling fan.

Overall efficiency = 1526 W/1594 W
= 96 %

2. Nominal 2.5 kW out (R_S = 31.5 mΩ)

Input voltage = 222 V_{RMS}
Input current = 12.25 A_{RMS}
giving input power =
P02 = (222 V x 12.25 A) = 2719 W
Output voltage = 335 V_{DC}
338 V_{RMS}
Output current = 7.62 A_{DC}
7.65 A_{RMS}
giving output power =
(338 V x 7.65 A) = 2585 W
T_A = 19.9°C, T_S = 52.9°C
giving ΔT = 33 K
$P_{SEMI} = \Delta T/R_{thSA}$ = 33 K/0.32 K/W = 103 W

giving losses in remainder of system
(2719-2585-103) = 31 W
Overall efficiency =
2585 W/2719 W = 95 %

Given that at P_0 = 2.5 kW nominal, the PFC output voltage had already dropped to 335 V_{DC} from its nominal open circuit level of 390 V_{DC}, it was evident that the passive control net-works associated with the IC required optimization for yet higher power out-puts. With this in mind, before making a final run at 3 kW, the current resistor R_S was reduced to 16.2 mΩ from 31.5 mΩ.

3. Nominal 3 kW out (R_S = 16.2 mΩ)

Input voltage = 226 V_{RMS}
Input current = 14 A_{RMS}
giving input power =
P03 = (226 V x 14 A) = 3164 W
Output voltage = 357 V_{DC}
361 V_{RMS}
Output current = 8.12 A_{DC}
8.2 A_{RMS}
giving output power =
(361 V x 8.20 A) = 2960 W
T_A = 30.3°C, T_S = 81.7°C
giving ΔT = 51.4 K
$P_{SEMI} = \Delta T/R_{thSA}$ = 51.4 K/0.32 K/W
= 161 W
giving losses in remainder of system
(3164-2960-161) = 43 W
Overall efficiency = 2960 W/3164 W
= 94 %

Enhanced gate drive for lower switching losses

The standard Unitrode IC drive circuit was not optimized to rapidly commutate off 2 x size # 7 large Power MOSFETs in parallel, the gate capaci-tance of these being in excess of 8.5 nF. As a consequence, during high frequency operation (f ≥ 25 kHz), significant switch-off losses are gene-rated due to the long overlap (cross over) of drain current and drain voltage. Waveforms observed under a nominal 1750 W load are shown in Fig. 10 a+b.

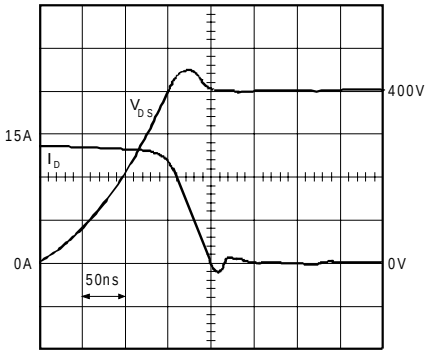


Fig. 10a Switch-off, f = 100 kHz, R_G = 4.7Ω

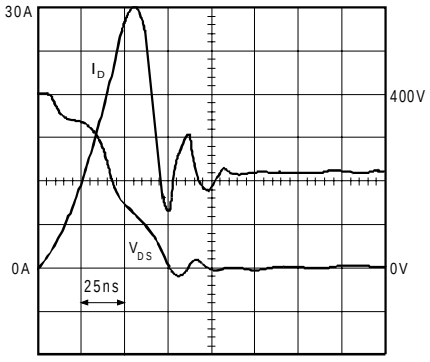


Fig. 10b Switch-on, f = 100 kHz, R_G = 4.7Ω

Note: Currents measured with a Pearson # 411 current pulse transformer connected in the MOSFET drain connection. Voltages measured with a Tektronix # 453 A, 60 MHz oscilloscope. With a 4.7 Ω resistor, turn-off at least is free of ringing, but turn-on is decidedly oscillatory.

Addition of the buffer circuit illustrated in Fig. 11 dramatically shrinks the cross over time and leads to a substantial reduction in switching losses.

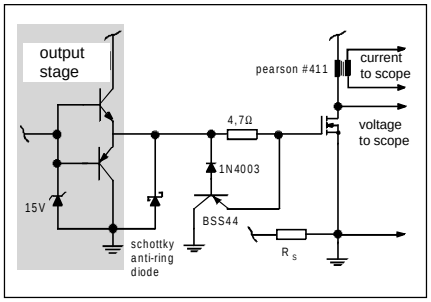


Fig. 11 Speed-up circuit

When the IC initiates turn-off, the BSS44 PNP epitaxial high speed tran-sistor conducts hard, quickly dischar-ging the MOSFET gate capacitance. The 1N4003 diode is necessary to prevent avalanching the transistor base-emitter junction during normal turn-on. The effects of this circuit are shown in Fig.12 a+b. Note that total switching time is reduced from 200 ns to 100 ns, with a minor sacrifice in overshoot voltage due to the higher di/dt.

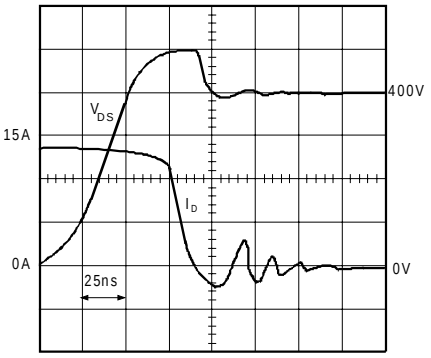


Fig. 12a Switch-off (enhanced circuit)

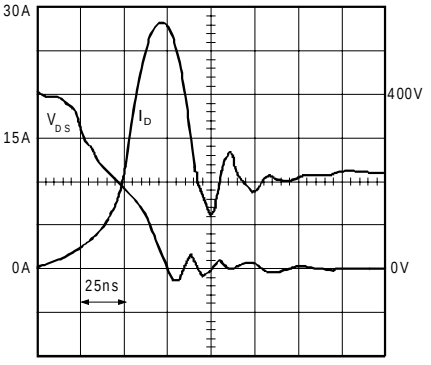


Fig. 12b Switch-on (enhanced circuit)

Although turn-on is not directly im-proved, since the 4.7 Ω series resistor is retained, there is a reduction in peak diode recovery; this is due to the lower junction temperatures resulting from less losses.

It may be asked why not substitute a complementary emitter follower for the single turn-off enhancement transistor, in an attempt to improve turn-on as well as turn-off? As already observed with a 4.7 Ω series gate resistor, significant ringing is evident and the effective elimination of all series damping resi-stance would almost certainly provoke intolerable and dangerous oscillation. So prudence dictates leaving the ori-ginal turn-on configuration undisturbed.

The benefits of reduced switching times were evaluated by running a special test on a PFC circuit temporarily fitted with discrete switching devices instead of the VUM 24 module. The reason for using discretes was to better isolate and monitor losses in the MOSFET itself, as opposed to all losses being “mixed” in one housing.

A Power MOSFET in miniBLOC-package, type IXTN 36N50 was used as the shunt switch, and a DSEI 2x30-06C miniBLOC FRED (**F**ast **R**ecovery **E**pitaxial **D**iode, 1/2 only wired up) as the boost diode. Note that this MOSFET contains identical chips to the VUM 24 and the FRED chip is also the same as in the module, so switching losses will be identical between the two versions.

Both miniBLOCs were installed on the same heat exchanger as employed for the module, the MOSFET being mounted over the temperature probe position.

Thermal resistance was determined by passing DC current through a series combination of the MOSFET and FRED using techniques similar to those used to calibrate the module version. The measured value of R_{thSA} was 0.305 K/W, this for the MOSFET primarily, since the FRED was physically somewhat remote from the temperature probe. No DC bridge was installed, DC power being furnished from an external source - an SMPS for the thermal evaluation, and a standard full wave bridge for the actual PFC runs.

Run # 1:
f = 100 kHz, standard gate drive,
P_{out} = 2590 W
T_A = 23°C, T_S = 47.6 °C after 45 min.
giving ΔT = 24.6 K
$P_{MOS/FRED} = \Delta T/R_{thSA}$ = 24.6 K/0.305 K/W = 80.7 W

Run # 2:
As run # 1, but with turn-off enhancement
T_A = 23.3 °C, T_S = 39.6°C after 45 min.
giving ΔT = 16.3 K
$P_{MOS/FRED} = \Delta T/R_{thSA}$ = 16.3 K/0.305 K/W = 53.4 W

Improvement = #1-#2/#1 =
80.7 - 53.4/80.7 = 34 % less

Since it is virtually impossible to ascertain just how much of this power is dissipated in the MOS, and how much results from the remotely mounted FRED, the absolute values of measured power are not trustworthy. The differences however are real, showing a 34 % reduction in switching losses resulting from the speed up circuit.

While this temporary set-up was operational, the opportunity was taken to re-run the equipment at a lower switching frequency, to determine the effects of switching frequency on losses, both with and without the enhancement circuit.

To halve the switching frequency, capacitor C11 on the Unitrode evalua-tion board was doubled from 1 nF to 2 nF. Measured clock frequency was 54.9 kHz.

The PFC was then run twice more, once without and once with the gate drive enhancement circuit.

Run # 3:
f = 54.9 kHz, standard gate drive,
P_0 = 2590 W
T_A = 23.2°C, T_S = 40.1°C after 45 min.
giving ΔT = 16.9 K
$P_{MOS/FRED} = \Delta T/R_{thSA}$ = 16.9 K/0.305 K/W = 55.4 W

Run # 4:
f = 54.9 kHz, enhanced gate drive,
P = 2590 W
T_A = 22.7°C, T_S = 34.4°C
giving ΔT = 11.7 K
$P_{MOS/FRED} = \Delta T/R_{thSA}$ = 11.7 K/0.305 K/W = 38.3 W

Improvement = #3-#4/#3 =
55.4 - 38.3 = 55.4 = 31 % less

It is clear from comparing Runs #1 and #2 against #3 and #4 that total switching device (MOSFETs & FRED) losses are reduced substantially through operation at lower frequencies, and in both cases the speed up circuit has a very dramatic effect. Extrapolation to even lower frequencies (just above 20 kHz, audio threshold?) should logically produce even more beneficial effects on semiconductor operation. Although this is clearly true, the "downside" is the need to increase the boost inductor size. This trade off was dramatically illustrated by the behaviour of the existing circuit (boost inductor = 918 µH, more than adequate for f_s = 100 kHz or 50 kHz) when operated at 26 kHz.

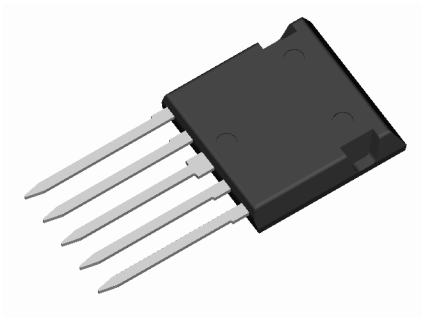
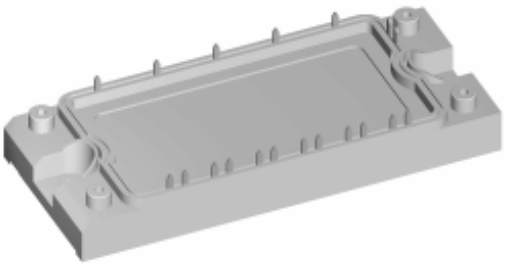
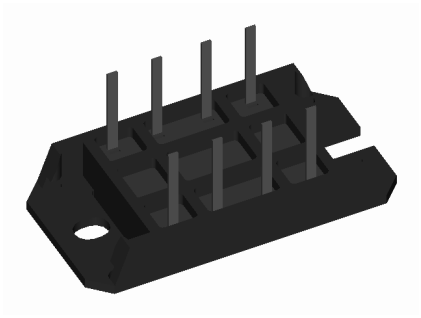
C11 was increased by adding a 3.3 nF capacitor to the original 1 nF, which reduced the clock frequency to 26 kHz. Although the circuit output remained at 2590 W with clean semiconductor switching as observed on the oscillos-cope, the 0.47 µF AC line filter capacitor C1 literally exploded after a few minutes of operation. Subsequent investigation showed that at 2590 W out, the inductor L1 saturated during mid-cycle, allowing over 50 A peak 26 kHz current spikes to flow through the 0.47 µF "filter" capacitor C1. At lower power levels, before the onset of saturation (1300 W), peak-to-peak ripple current on the 50 Hz mains was 8 A at 26 kHz. The conclusion only reinforces the laws of physics - high frequency equates to small reactive elements plus elevated semiconductor losses, where lower frequencies produce the opposite results.

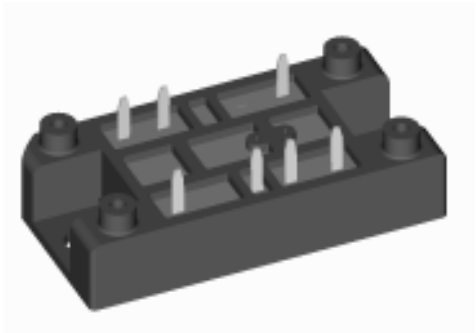
Conclusions

This new range of power stages for boost converters, type VUM 24-05 rated at 24 A/500 V and type VUM 33-05- rated at 33 A/500 V - is capable of delivering the maximum allowable power authorized from nor-mal European 220/230/240 V_{RMS} mains (16 A_{RMS} x line voltage) at efficiencies of 95 %, when driven from commercially available PFC Controller ICs like the Unitrode UC 3854. Permitting compact and reliable equipment designs, easy to engineer and manufacture, these products represent a real advance in state-of-the-art of high frequency power conversion.

Rectifiers with Power Factor Correction

by Andreas Lindemann, IXYS Semiconductor GmbH



1. Introduction

1.1 Standard Rectifiers

The topology of a standard single phase rectifier is shown in figure 1. The terminals L1 and N are connected to the grid while L+ and L- supply the inter-mediate circuit. Usually the DC voltage U_Z in the intermediate circuit is smoothed by a capacitor. To save cost, generally no further reactive components are used; this means, that only mains inductance and additional parasitic inductances have any effect. Characteristic waveforms of this circuit are shown in figure 2.

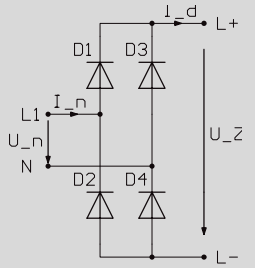


Fig. 1: *Schematic of non controlled, single phase rectifier*

This topology can be characterized as follows:

- It is simple - no control required - and rugged.
- Current flow from the grid to charge the intermediate circuit $I_d > 0$ is only possible in case the instantaneous value of the mains voltage is higher than intermediate voltage $u_n(t) > U_Z$. This leads to a short conduction period of the rectifier with the consequences that mains current I_n has high peak values, high RMS values and is harmonically distorted - see figure 2.

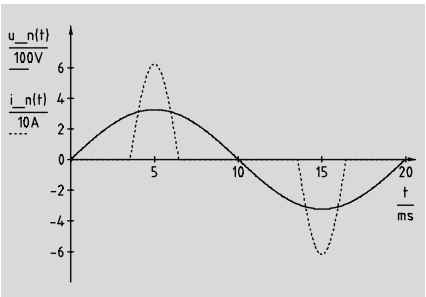


Fig. 2 *: Typical input waveforms of non controlled, single phase rectifier (P_n = 3600 W)*

- Further harmonic distortion of the mains current I_n is caused by commutation effects of the diodes using the mains inductance as commutation inductance.
- The DC voltage U_Z depends on the mains voltage U_n. Variations in mains voltage U_n thus have to be compensated in a further stage of power section, if required.
- Turning power on leads to a high mains inrush current peak I_n to charge the capacitor in intermediate circuit previously discharged.

  This may be overcome by replacing at least two of the diodes in the schematic figure 1 by thyristors, which also permits to control DC voltage. However this measure increases control complexity and its use leads to the additional generation of reactive power.

The operational behaviour of three phase rectifiers basically corresponds to these characteristics as discussed here for single phase rectifiers.
It has become obvious that the use of standard rectifier circuits leads to problems of electromagnetic compatibility (EMC) due to the harmonic distortion of the input current I_n. The recent standardization [1] [2] aims at their reduction. The limits specified may be met with a standard rectifier circuit, complemented by passive filter components towards mains. These however are rather large and expensive. Further, in EMC sensitive applications, such as power supplies for telecommunications or computers, the occurrence of harmonics in the rectifier, although filtered towards the grid, may disturb the operation of the whole circuit.

1.2 Rectifiers with Power Factor Correction

As an alternative, controlled rectifiers can be used. They can be characterized as follows:

- The occurrence of harmonics in mains current I_n is actively minimized.
- In operation, the intermediate circuit is charged during the whole mains period with sinusiodal current I_n in phase with the mains voltage U_n; this optimizes the maximum available active power through a given mains fuse.
- The voltage of DC link U_Z is controlled and thus independent of mains voltage U_n over a wide range.

  This helps to overcome possible problems of unstable supply voltage. Additionally, the rectifier is suitable for wide input voltage range: This means, that the device may be connected to any mains voltage U_n; it is not necessary to preselect the voltage range, because the controlled rectifier will keep DC voltage U_Z at the required level.
- Only few and small passive components are required.

So this type of controlled rectifiers does not only help to meet the requirements of the EMC standards, but it offers significant additional benefits.
Different types of controlled rectifiers for a variety of applications are presented in the following.

2. Single Phase Power Factor Correction

2.1 Mode of Operation

The schematic of a single phase rectifier with power factor correction in boost topology is shown in figure 3. Its operation is discussed with reference to figures 4, 5 and 6:

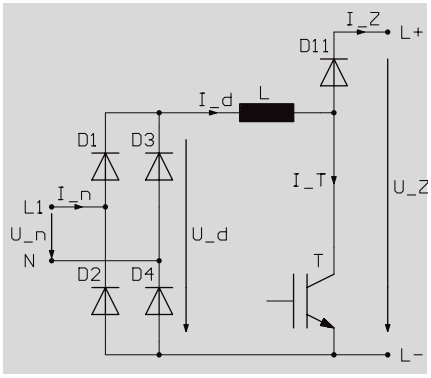


Fig. 3: *Schematic of single phase rectifier with power factor correction*

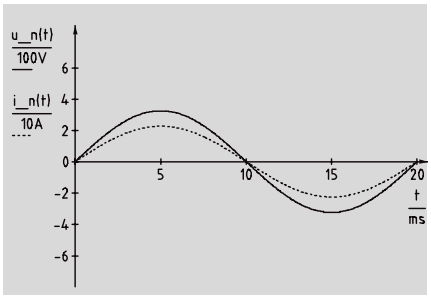


Fig. 4: *Typical input waveforms of single phase rectifier with power factor correction ($P_n = U_n \cdot I_n$ = 3600 W)*

Figure 4 depicts the waveforms of mains voltage u_n (t) (solid) and mains current i_n (t) (dotted). Due to the - ideally - sinusoidal shape of current i_n (t), there would be no harmonic content; furthermore, the phase angle zero between mains voltage u_n (t) and current i_n (t) avoids the occurrence of first harmonic reactive power. Please note the significantly lower amplitude of mains input current of the rectifier with power factor correction in figure 4 compared to the standard rectifier as in figure 2; both waveforms are displayed in the same scale and for the same rectified power.

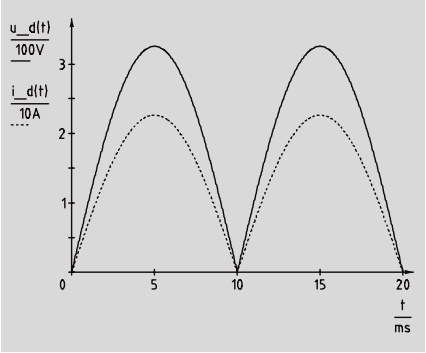


Fig. 5: *Typical rectified waveforms of single phase rectifier with power factor correction ($P_n = U_n \bullet I_n = 3600$ W)*

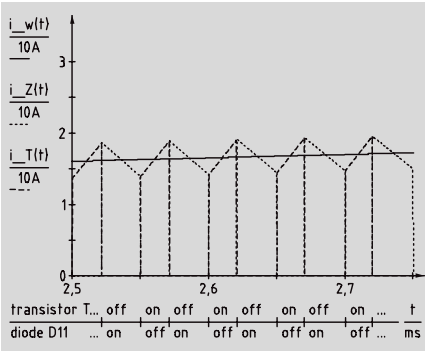


Fig. 6: *Typical boost chopper waveforms of single phase rectifier with power factor correction ($P_n = U_n \bullet I_n = 3600$ W)*

On the secondary of the rectifier bridge according to figure 3, the waveforms look as shown in figure 5: The diodes have rectified primary current and voltage as have been depicted in figure 4, thus folding the previously negative half-waves of voltage and current to the first quadrant, while their sinusoidal shape has been maintained.

Finally figure 6 depicts current waveforms taken at the chopper in a magnified time interval: The solid line represents the command variable i_w (t) for the boost chopper's input current i_d (t); the slightly rising slope corresponds to a section of the sinusoidal half-wave of the rectified input current i_d (t) according to figure 5. This desired waveform is approximated by the boost chopper, composing the sinusoidal half-waves of i_d (t) according to i_d (t) = i_T (t) + i_Z (t). The boost chopper's pulse pattern is documented below the time axis of figure 6: When the transistor *T* is turned on, it will carry a current i_T (t) according to the broken line; current rises, because the voltage u_d (t) is applied to the inductor *L* which will further magnetize. Having turned the transistor *T* off, the diode D_{11} will turn on and thus cause the inductor to demagnetize by a decreasing current i_Z (t) (dotted) into the intermediate circuit, with the voltage of intermediate circuit being larger than rectified mains voltage at any time $U_Z > u_d$ (t).
This way, the sum i_d (t) = i_T (t) + i_Z (t) represents a waveform with an average value according to the desired sinusoidal current i_w (t) and an additional triangular ripple due to boost chopper operation.

The latter's switching frequencies typically are in the range of $50\,kHz \le f_T \le 100\,kHz$, which minimizes size and cost of the inductor *L* and possible additional filter components. The control method for this kind of power factor corrected rectifiers is implemented in a variety of integrated circuits, which significantly faciliates their design - see for example [3], [4], [5], [6], [7], [8] or [9]. The following section will deal with suitable integrated power semiconductors.

2.2 Suitable Integrated Power Semiconductors}

2.2.1 General

The following aspects should be considered in choosing power semiconductor components for a power factor corrected single phase rectifier with a topology according to figure 3:

- The **rectifier diodes** D_1 to D_4 must be able to stand the inrush current peak at power on as mentioned in section 1.1, however reduced by the inductor *L*. Further, fast switching behaviour is advantageous to reduce the emission of disturbances during commutation at zero transition of mains current. Special mains rectifier diodes with fast switching behaviour are referred to as semifast diodes in the following.

- The **transistor in the boost chopper *T*** should be a fast switching device - either a high voltage MOSFET or an IGBT with optimized switching speed- to operate at the high switching frequency as mentioned in section 2.1. The use of a component with low gate charge Q_G is beneficial, because it helps to minimize the required drive power.

- The **free wheeling diode of the boost chopper** D_{11} must be optimized for high switching speed, particularly at turn off in switched mode operation. Fast recovery epitaxial diodes - FREDs - should be used; their performance can additionally be improved using a series connection of two diodes. If the free wheeling diode is correctly sized for operation at nominal power and high switching frequency, it generally stands the inrush current at power on as mentioned above.

- Several requirements refer to the **package**: The power circuit must be isolated from the heatsink for safety reasons; thus the package should provide an internal isolation. This, together with the integration of several power semicondcutors in the same package, leads to low mounting effort. The integration as mentioned is further indispensable to achieve a good operational behaviour of the chopper, particularly regarding high frequency fast switching.

Obviously, the whole rectifier with power factor correction should be considered as one system, the parts of which have to be matched to each other and to the application.

2.2.2 Component Types, their Ratings and Characteristics

In this section, several combinations of power semiconductor components constituting power factor corrected single phase rectifiers are discussed according to the approach, that the whole rectifier should be considered as one system, Consisting of several components operating together.

Different sets of power semiconductor components are listed in table 1 together with their major characteristics as explained in section 2.2.1:

- The left columns give IXYS' type designations: Either one type is mentioned, integrating all components - or two types, the first incorporating the rectifier bridge D_1 to D_4, the second the boost chopper *T* and D_{11} according to figure 3.

- The next column names the package type. All packages are isolated. The outline of Isoplus I4-Pac is shown in figure 7; this new package combines features of discrete components - it looks similar to - with features of modules - such as isolation and reliability, see [10]. Veridul module package is depicted in figure 8. Eco-Pac is a similar module, however with a smaller footprint of 30.3 mm • 47 mm.

- Features of the chips - rectifier D_1 to D_4, boost chopper transistor *T* and free wheeling diode D_{11} are outlined in the three columns on the right of table 1.

Table 1: *Features of components for single phase power factor correction*

Type designation rectifier	Type designation chopper	features package(s)	features rectifier	features transistor	features diode
VUI9-06N7		Eco-Pac module	semifast	fast IGBT	series FREDs
FBO16-08N	**FID35-06C**	Isoplus I4-Pac	standard	fast IGBT	series FREDs
FBO16-08N	**FMD21-05QC**	Isoplus I4-Pac	standard	low Q_G MOSFET	series FREDs
VUM24-05N		Veridul module	standard	MOSFET	FRED
VUM33-05N		Veridul module	standard	MOSFET	FRED

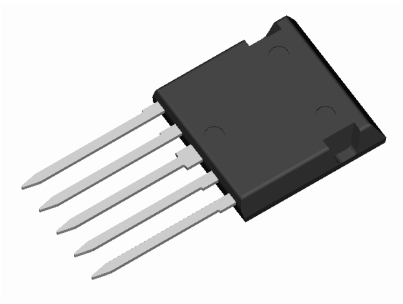


Figure 7: *Outline of Isoplus I4-Pac package: dimensions ~ 20 mm • 21 mm*

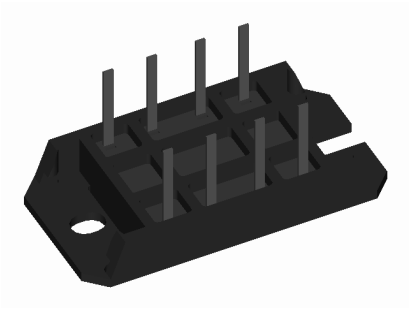


Figure 8: *Outline of Veridul package: dimensions 31.6 mm • 63 mm*

Table 2: *Typical nominal mains power P_n of components for single phase power factor correction; conditions: voltage of intermediate circuit U_Z = 400 V, switching frequency f_T = 75 kHz, case temperature T_C = 80 °C*

Type designation rectifier	Type designation chopper	P_n at U_n = 110 V	P_n at U_n = 240 V
VUI9-06N7		900 W	2100 W
FBO16-08N	**FID35-06C**	950 W	2600 W
FBO16-08N	**FMD21-05QC**	1400 W	3100 W
VUM24-05N		2200 W	2800 W
VUM33-05N		3300 W	4200 W

According to the approach to consider the whole rectifier as one system, detailed calculations have been carried out to determine the ratings of the power factor corrected single phase rectifiers as suggested. The results are shown in table 2: Under the typical operating conditions listed in the caption, the rectifier systems can take the indicated power out of mains and transfer it - reduced by the losses - to the intermediate circuit. Two power ratings are given, covering the international mains voltage range; this way, the nominal power of a rectifier system can be determined either for a fixed input voltage or for wide input voltage range.

The calculations, leading to the results as presented in table 2, use both - the characteristic values and maximum ratings of the power semiconductor components, and the knowledge of power factor corrected rectifier's mode of operation as explained in section 2.1: At given operating conditions - such as voltage of intermediate circuit U_Z, switching frequency f_T and case temperature T_C - junction temperature of the several semiconductors D_1 to D_4, T and D_{11} is calculated with the parameters mains voltage U_n and current I_n. Maximum junction temperature of any semiconductor may not be exceeded, which determines the permitted mains voltage U_n - mains current I_n operating range of the rectifier system. With these limits, nominal mains power can be calculated by $P_n = U_n \bullet I_n$.

So the calculations as described have two uses: The indications of nominal power for the whole power factor con-trolled rectifier system permit to easily select power semiconductor components for a given rectifier rating in a variety of applications. Thus rectifier design is significantly faciliated. Further the system approach helps to match the different power semiconductors to an optimum, leading to optimized components: The most economic solution will match the ratings of the single semiconductors D_1 to D_4, T and D_{11} in a way, that the $U_n \bullet I_n$ operating ranges of all parts are as congruent as possible.

3. Three Phase Power Factor Correction

There are several topologies and control methods to implement power factor correction as described in section 1.2 for three phase systems; a survey of techniques is given in [11].
Different types of three phase power factor corrected rectifiers with continuous mains current will be discussed in the following sections.

3.1 Combination of Three Single Phase Rectifiers

It is possible to connect one single phase power factor corrected rectifier as shown in figure 3 and as explained in section 2 between each of the three mains phases

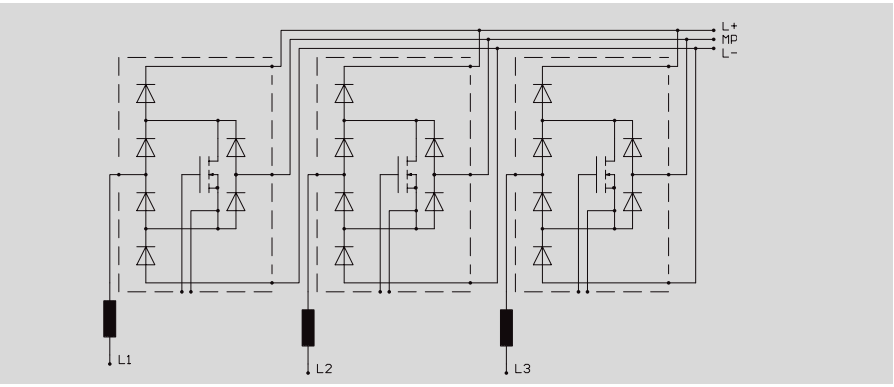


Figure 9: *Schematic of three phase rectifier with power factor correction - "Vienna" rectifier*

and the neutral conductor. However this solution is hardly used because of its drawbacks: Often no neutral conductor is available. Furthermore the rectified power is transferred to three DC links - one per phase; additional DC-DC conver-ters with galvanic isolation would be needed to make the rectifier a single DC voltage source as commonly required.

True three phase rectifier systems as outlined in the next sections prove to be better solutions.

3.2 Three Phase ''Vienna'' Rectifier

The topology of ''Vienna'' rectifier is shown in figure 9; it can be characterized as follows:

On the mains side, there is one inductor for each phase L_1, L_2, L_3. There is no need for a neutral conductor. The circuit will operate with wide input voltage range.

The output of the rectifier is an intermediate circuit with controlled DC voltage between *L+* and *L-* with center point *MP*.

There is one controllable switch per phase - MOSFETs are depicted. Together with the surrounding four diodes bridges, they operate as bidirectional switches: When turned on, they connect the respective mains phase to the DC center point via two diodes and the inductor, which makes the latter magnetize. When turned off, the inductor demagnetizes into the DC link via the free wheeling diodes connected to *L+* or *L-* respectively.

It is obvious that this operational principle is similar to the one described for the single phase power factor corrected rectifier in section 2.1. Further details about operation and control of the circuit can be found in [12], [13], [14].

In particular, the method explained in [12] permits the calculation of the power ratings of the "Vienna" rectifier analogous to the approach for the power factor corrected single phase rectifier in section 2.2.2. Basic ratings and characteristics of ''Vienna'' rectifiers built with IXYS modules are listed in table 3.

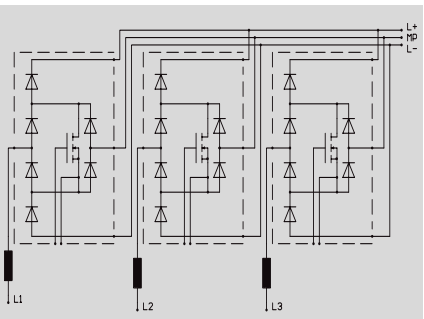


Figure 10: *Schematic of three phase full bridge*

Table 3: *Typical nominal three phase mains power P_n of components for three phase power factor correction; conditions: mains voltage $U_{\Delta n}$ = 400 V, case temperature T_C = 80 °C*

Type designation	P_n	package	options
VUM25-05	10 kW	V1-Pack	
VUM85-05A	30 kW	V2-Pack	soft start thyristor

A ''Vienna'' rectifier will use one of the indicated modules per phase. As could be expected, its range of rectified power is higher, compared to single phase rectifiers as rated in table 2. Both components in table 3 are isolated modules, where V1-Pack has the same footprint as Veridul package - see figure 8 - while V2-Pack is bigger with a footprint of *40.4 mm • 93 mm* according to the higher nominal power. The VUM85 module additionally provides a soft start thyristor to give the capability to limit the inrush current at power on, as already discussed in sections 1.1 and 2.2.1.

3.3 Three Phase Full Bridge

The last circuit to be presented is the self commutated three phase full bridge shown in figure 10. Mains would be connected via inductors to the phase outputs L_1, L_2, L_3, while *L+* and *L-* represent the constant voltage DC link. The self commutated three phase full bridge can be used as rectifier and inverter; thus it permits bidirectional energy transfer, which is useful for applications with energy recovery. However, the circuit contains twice the amount of controllable switches - six IGBTs in figure 10 - compared to the ''Vienna'' rectifier as described in section 3.2; consequently driving effort is somewhat higher. Furthermore, semiconductors with higher blocking voltages are needed. In the end, the particular requirements of the actual application will decide which solution to prefer.

Applications of this topology are wide spread in power electronics. Many control methods are known and implemented in integrated circuits. A variety of integrated power semiconductors for a wide power range is available. Without claiming completeness, table 4 lists some module types of IXYS with their most important ratings.

Table 4: *Self commutated full bridges for three phase power factor correction; breakdown voltage $U_{(Br)CEs}$ and DC ratings at case temperature T_C = 80 °C of IGBTs (I_{C80}) and diodes (I_{F80})*

Type designation	$U_{(Br)CEs}$ V	I_{C80} A	I_{F80} A
MWI30-06A7	600	30	24
MWI50-06A7	600	50	45
MWI75-06A7	600	60	85
MWI100-06A8	600	85	85
MWI150-06A8	600	125	125
MWI200-06A8	600	165	170
MWI25-12A7	1200	35	33
MWI35-12A7	1200	44	33
MWI50-12A7	1200	60	70
MWI75-12A8	1200	100	100
MWI100-12A8	1200	120	130

4. Conclusion

Power factor correction for mains rectifiers is an upcoming issue. Operating principles of single and three phase power factor corrected rectifiers have been explained. Suitable integrated power semiconductors have been presented. Power factor corrected rectifier systems using thesecomponents have been rated as a result of detailed calculations. This paper has shown that single and three phase power factor corrected rectifiers are feasible and how they can be designed.

References

[1] IEC61000-3-2: Grenzwerte für Oberschwingungsströme (Geräte-Eingangsstrom <16 A je Leiter)

[2] IEC61000-3-4: Grenzwerte für Oberschwingungsströme (Geräte-Eingangsstrom >16 A je Leiter)

[3] TDA4817 IC for High Power Factor and Active Harmonic Filtering; Siemens, 1995

[4] TDA4862 Power Factor Controller (PFC) IC for High Power Factor and Active Harmonic Filter; Siemens, 1998

[5] M. Herfurth: Power Factor Controller TDA4862 Applications; Siemens HL application note AT 2 9402 E

[6] B. Andreycak: UC3854A and UC3854B Advanced Power Factor Correction Control ICs; Unitrode Corporation, application note DN-44, 1994

[7] P. C. Todd: Boost Power Factor Corrector Design with the UC3853; Unitrode Corporation, application note U-159, 1999

[8] UC1854, UC2854, UC3854 High Power Factor Preregulator; Unitrode Corporation, 1999

[9] UC1858, UC2858, UC3858 High Efficiency, High Power Factor Preregulator; Unitrode Corporation, 1999

[10] A. Lindemann: Combining the Features of Modules and Discretes in a New Power Semiconductor Package; PCIM Conference, Nürnberg, 2000

[11] J. W. Kolar, H. Ertl: Stand der Techniknetzrückwirkungsarmer dreiphasiger Gleichrichter-schaltungen; VDE-ETG-Tage, Essen, 1995

[12] J. W. Kolar, H. Ertl, F. C. Zach: IXYS-VUM25-E - A New Isolated Power Module for Low-Cost/ Weight/Volume High Performance Three-Phase Sinusoidal Input Current Power Conditioning; Power Quality Conference, Nürnberg, 1995

[13] J. W. Kolar, U. Drofenik, F. C. Zach: DC Link Voltage Balancing of a Three-Phase/ Switch/Level PWM (Vienna) Rectifier by Modified Hysteresis Input Current Control; 29th PCIM Conference, Nürnberg, June 20-22, 1995

[14] J. W. Kolar, U. Drofenik, F. C. Zach: Space Vector Based Analysis of the Variation and Control of the Neutral Point Potential of Hysteresis Current Controlled Three-Phase/Switch/Level PWM Rectifier Systems; International Conference on Power Electronics and Drive Systems, Singapore, Feb. 21-24, 1995