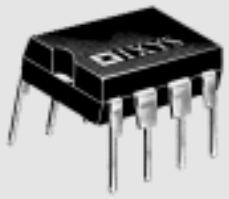
Contents



Integrated Circuits

The Smart Power ICs and Chip-sets manufactured by IXYS are designed to interface with the company's family of Power MOSFET and IGBT products in order to provide improved performance for a broad range of power conversion and motor control applications.

IXYS has focussed on two main areas:

- High/Low Side Driver Integrated Circuits which complement IXYS Power MOSFET and IGBT that offer with either open or closed loop protection of the power devices, such as the IXBD 4410 Series.
- PWM Regulator and Controller circuits optimized for specialized power supplies and motor control applications. The device satisfying this need would the IXMS 150 and IXDP 610.

Other devices included in the IXYS product range are a series of High Voltage Current Regulators, a Digital Deadtime Generator and a Negative Voltage Hot Swap Controller.

IXYS has an experienced staff of analog, digital and power designers who are teamed together to ensure accurate definition of future generations of integrated solutions to satisfy the needs for the power control, power conversion and motion control markets.

Using the advantages and compatibility of CMOS and IXYS HDMOS™ process, IXYS will continue to integrate functions for power control which are still composed discretely.

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Negative Voltage Hot Swap Controller with Active Power Filter

The IXHQ100 is a live insertion and removal circuit board power manager with a built-in power noise filter. It incorporates all the active circuitry necessary to protect circuit boards during live insertion or removal, (insertion or removal when the system power is on or active). Additionally, the IXHQ100 incorporates two new features. The first is a power active filter for improved -V_{IN} noise suppression and eliminates costly, bulky, and heavy passive power filter components. The second is an Auto-Detect circuit, which senses the loss of either Gnd or -V_{IN}, and eliminates the need for additional staggered Gnd or -V_{IN} pins and their associated detection components.

The IXHQ100 includes an on board shunt regulator to ensure wide input voltage range operation. The IXHQ100 allows continuous load current rise adjustments, presettable maximum current limits, and user variable fault indication turn off times for resetting uPs and other synchronous board level systems. For added flexibility, GSNSin pin is available to implement either circuit board insertion/removal or -V_{IN} undervoltage detection.

Features

- Live Insertion and Removal Power Manager
- Controlled Ramp-Up of Load Current.
- Autodetect of Load Open Circuit or -V_{IN} Disconnection
- Operates from –9 V to – (External MOSFET Voltage Limit) V
- Fault Indication Output (microprocessor reset).
- Board Insertion/Removal Detector Input
- Low frequency Power Active Filter
- Adjustable Circuit Breaker Interrupt Current
- V_{IN} undervoltage with GSNSin input

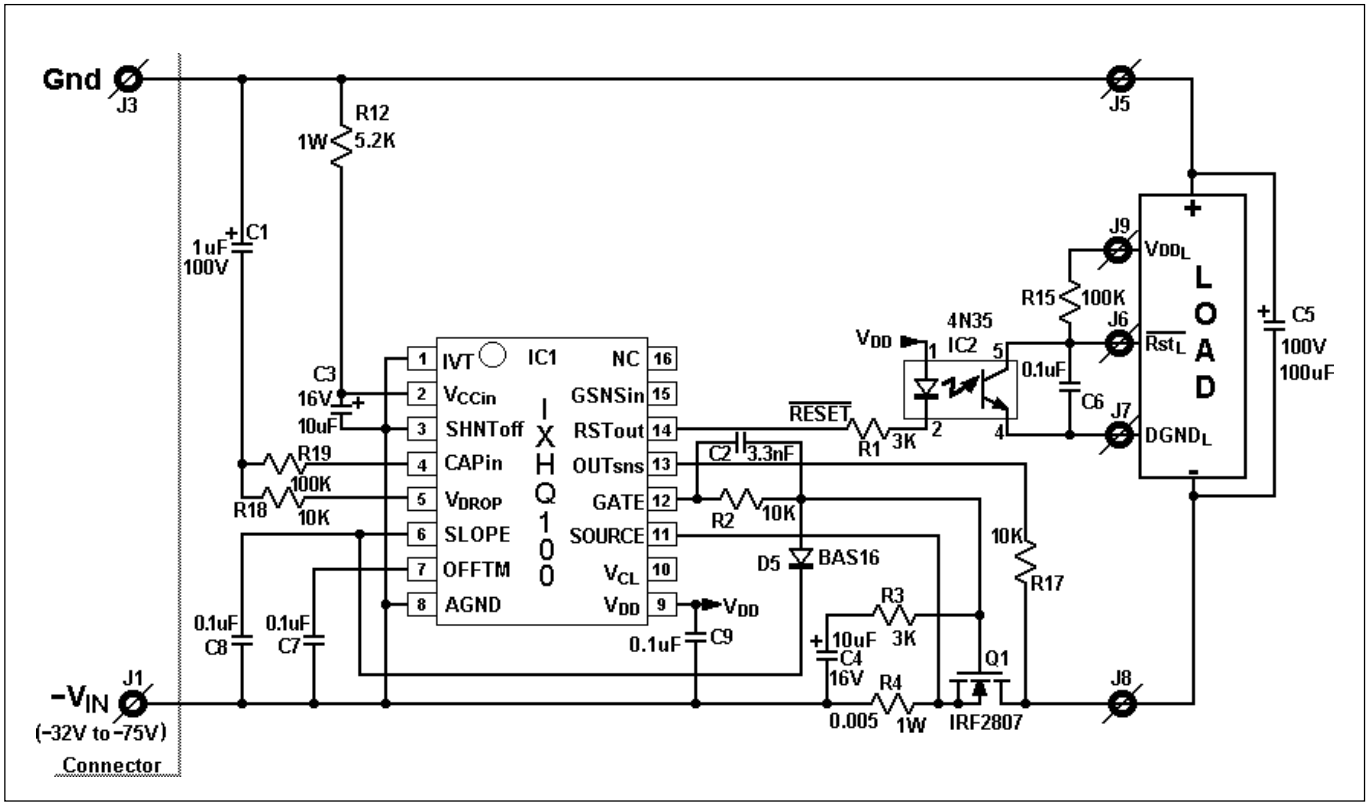
Applications

- Central Office Switching Hardware
- Circuit Boards From -48 V Distributed Power Supplies
- Circuit Board Power Manager and Noise Filter
- Circuit Board Hot Swap Protector and Manager
- Electronic Circuit Breaker

Telecommunications Application with Auto Ground Detect

Features:

- Ground detection without staggered pins
- Adjustable overcurrent protection with R4
- Floating reset output
- V_{DD} output (+5 V referred to -V_{IN})
- Active -V_{IN} filter
- Electronic circuit breaker



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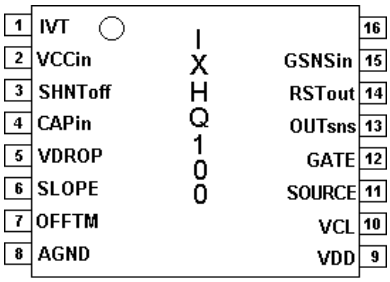
Absolute Maximum Ratings

Symbol	Definition	Max. Rating
V_{CC}-V_{AGND}	Voltage applied V_{CCin} to AGND	-0.3 V to 16 V
	All other pins except V_D	-0.3 V to V_{CCin} + 0.3 V V
I_{VDD}	V_{DD} Load Current	60 mA
T_{JM}	Maximum Junction Temperature	125 °C
T_J	Operating Temperature Range	-40 °C to 85 °C
T_{stg}	Storage Temperature Range	-65 °C to 300 °C

Pin Description



Electrical Characteristics

Unless otherwise noted, T_A = 25 °C; $-V_{IN}$= 48 V, AGND connected to $-V_{IN}$, $V_{SHUNToff}$ = 5 V, V_{CC} = 12 V, V_{GSNSin} = 12 V. All voltage measurements with respect to AGND. IXHQ100 configured as described in *Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Supply current	V_{CC}=12 V, $V_{SHUNToff}$ = V_{CC}, all outputs unloaded.		1.5	3	mA
I_{CCMAX}	Maximum shunted V_{CC} supply current	$T_{Package}$=T_{MAX} V_{CC} = 16V			60	mA
$V_{CCSHUNT}$	V_{CC} shunt regulation voltage	I_{CC} forced to 10 mA V_{SHUNT} = 0 V	12	14	16	V
$V_{THSHUNToff}$	SHUNToff input threshold voltage	V_{CC} = 15 V, monitor RST_{OUT}	0.8	1.1	2	V
$I_{SHUNToff}$	SHUNToff input bias current		-1		1	µA
V_{THIVT}	IVT input threshold voltage	V_{CC} = 12 V, monitor RST_{OUT}	6	8	10	V
Ri_{VT}	IVT input resistance		70	130	180	KΩ
V_{THGSNS}	GSNS sense input threshold voltage	V_{CC} = 12 V, monitor RST_{OUT}	4.5	6	7.5	V
I_{GSNSin}	GSNSin input bias current		-5	-2	-1	µA
I_{CAPin}	CAPin input bias current		-1		1	µA
V_{VDROP}	Active filter offset voltage		0.8	1.0	1.2	V
R_{VDROP}	V_{DROP} input resistance		70	90	110	kΩ
I_{SLOPE}	SLOPE capacitor charging current	V_{OFFTM} = 5 V, $V_{GSOURCE}$ = 0 V V_{CAPin}= 5 V	120	150	180	µA
$R_{SLOPEDCHG}$	SLOPE capacitor discharge resistance	V_{DROP} = 5 V, IVT = V_{CC} V_{SOURCE} = 0 V, V_{CAPin}= 5 V		130	200	Ω
I_{OFFTM}	OFFTM capacitor charging current	V_{DROP} = 5 V, V_{SOURCE} = 0 V V_{CAPin}= 5 V	120	150	180	µA
$R_{OFFTMCHG}$	OFFTM capacitor discharge resistance			130	200	Ω
$V_{THOFFTM}$	OFFTM input threshold voltage	OFFTM input voltage when SLOPE input voltage starts its ramp	3.8	4.2	4.5	V
V_{CL}	Overcurrent threshold bias voltage		120	150	180	mV
R_{VCL}	VCL bias resistance		4	7	10	kΩ
t_{OC}	Overcurrent detection to GATE output delay	V_{CAPin} = 0 V; V_{OUTsns} = 5 V V_{SOURCE} input is a step at t = 0s from 0 V to 200 mV		13	20	µs
dv_{GATE}/dt	GATE output slew rate	C_{SLOPE}= 100 nF	0.5	0.8	1.1	V/ms
V_{GATE}	Maximum GATE output voltage	V_{CAPin} = 0 V; R_{load} = 10 KΩ V_{OUTsns} = 5 V		10	11	V

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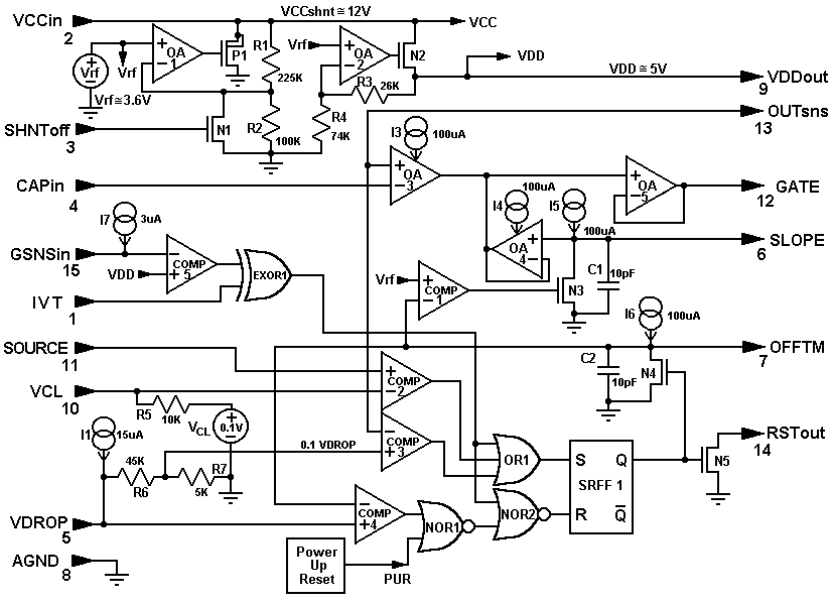
Electrical Characteristics (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{GATE}	GATE pull-up current	Gate drive on, V_{GATE} = 0 V		-15	-10	mA
I_{GATE}	GATE pull-down current	Gate drive off V_{GATE} = 10 V	10	20		mA
V_{DD}	V_{DD} regulator output Voltage	3.3K Resistive load between V_{DD} output and AGND	5	5.5	6.5	V
I_{RSTout}	RSTout drive current	V_{RSTout} =10 V during fault condition	15	30	50	mA
t_{RST}	RST pulse width		200	500	1000	ns
V_{ad}	Auto-Detect threshold	Gate drive on; ramp V_{OUTsns}; monitor RST until it pulses.	10	70	100	mV

IXHQ100 Logic Diagram



Functional Description

The IXHQ100 has three modes of operation:

1. Insertion/Removal mode

When the circuit board is inserted, the voltage across the load, V_{LOAD}, following the Power MOSFET controlled by the IXHQ100 starts at zero potential. V_{LOAD} rises at a slope determined by the value of the external capacitor placed between IXHQ100's SLOPE pin and AGND. When the circuit board is removed with V_{IN} live, the IXHQ100 first provides a RSTout low and turns off the external Power MOSFET. The RSTout low can be used by the circuitry powered by V_{LOAD} to gracefully shut down the circuit board system. If power is restored or the circuit board immediately reinserted, V_{LOAD} will start from zero potential and ramp up. With appropriate external components, GSNSin pin can work with staggered connectors to provide additional board insertion or removal detection.

2. Normal operation mode

With continuous $-V_{IN}$ applied, the IXHQ100 acts as an Active Power Filter by modulating the voltage drop across the external Power MOSFET, V_{DS}, so that any noise on $-V_{IN}$ is cancelled by V_{DS}. The direct connection of IXHQ100 AGND to $-V_{IN}$ allows the VDROP (internally set to ~750 mV) to set the ~90 % of the maximum peak noise voltage rejected by the IXHQ100. The internal VDROP setting of ~750 mV allows 1.35VPP of noise rejection.

3. Fault operation mode

When the output load current is such that the voltage drop across the current sense resistor between SOURCE and AGND exceeds VCL, (internally set to ~100 mV,) the GATE output is driven low to turn off the external Power MOSFET connected between the load and $-V_{IN}$. An external capacitor connected between OFFTM and AGND determines the off time, t_{off}, of IXHQ100 after this fault. After t_{off}, IXHQ100 will restart the turn on sequence of the external Power MOSFET with a load voltage slope determined by the size of the external capacitor connected to SLOPE. Whenever $-V_{IN}$ is interrupted or when the external circuit board disconnection is detected, RSTout will go low and the external Power MOSFET is shut off for another t_{off} period.

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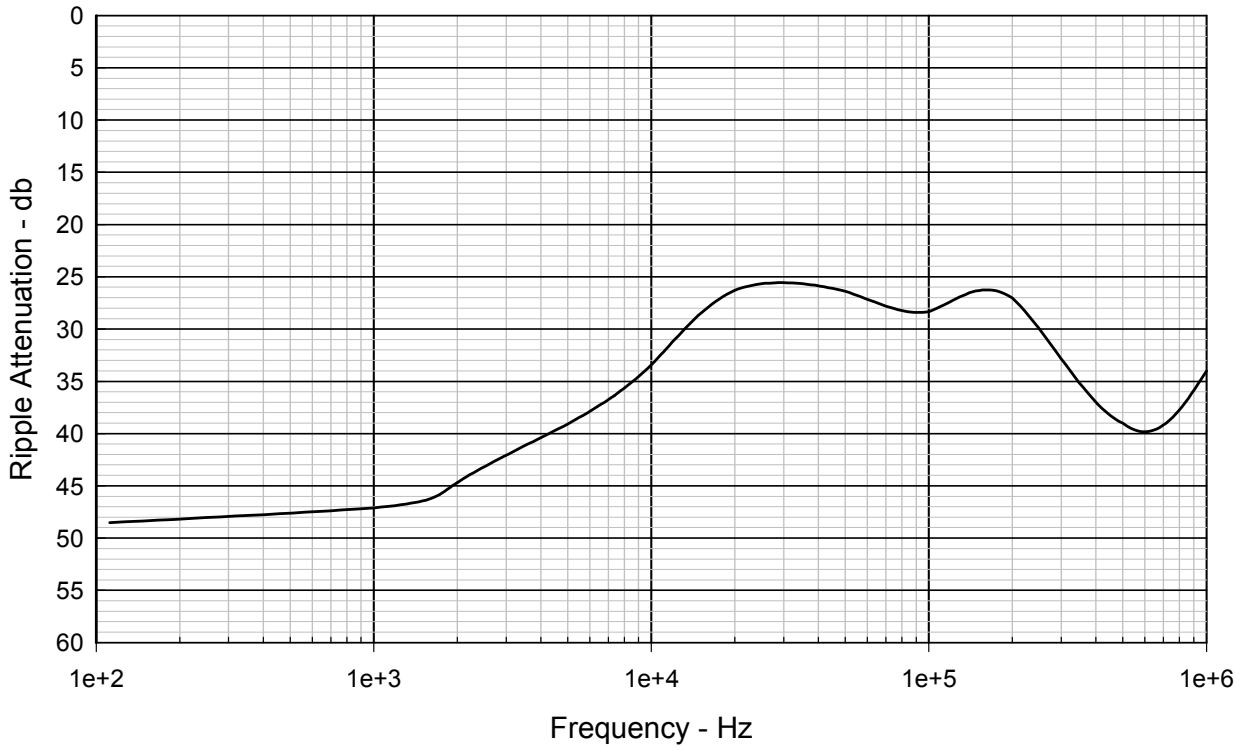
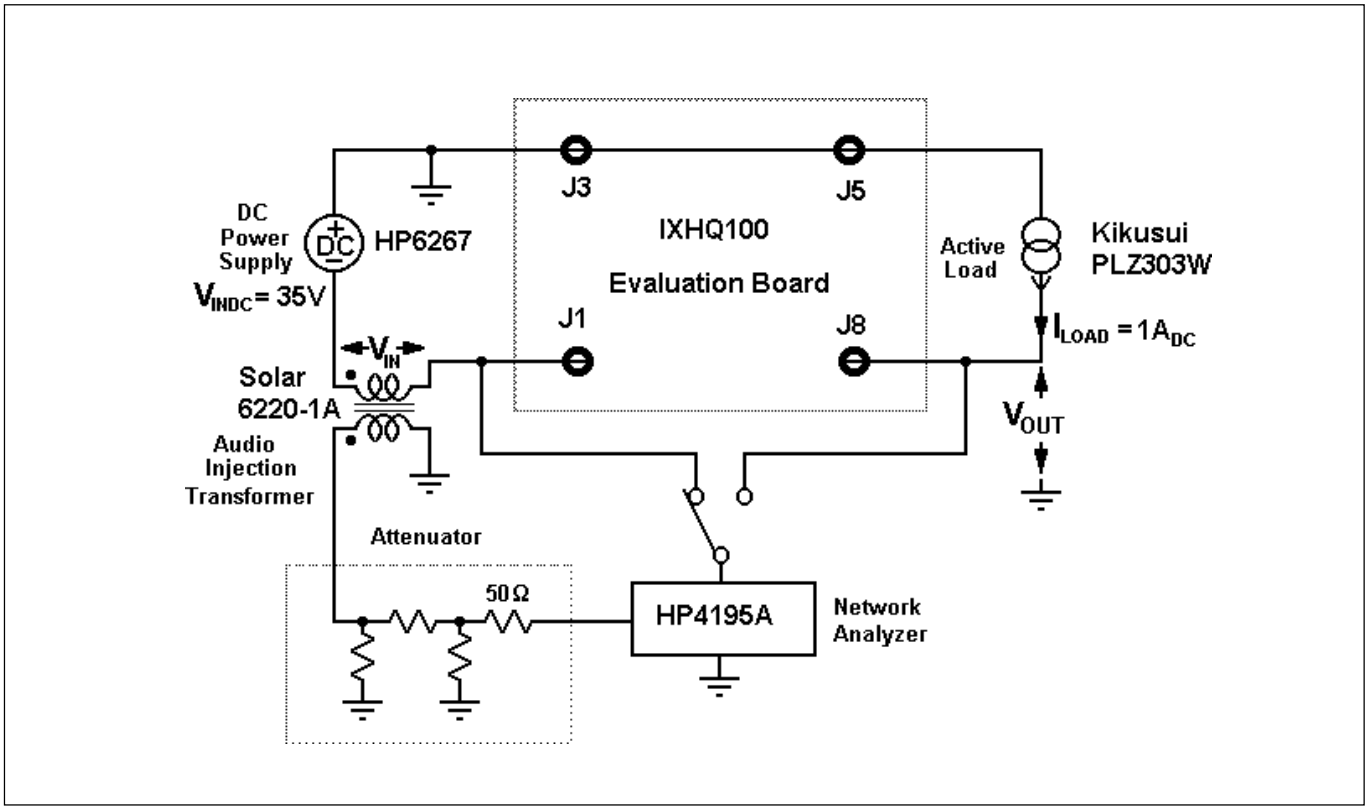
Ripple Attenuation



Test Circuit for Ripple Attentuaion



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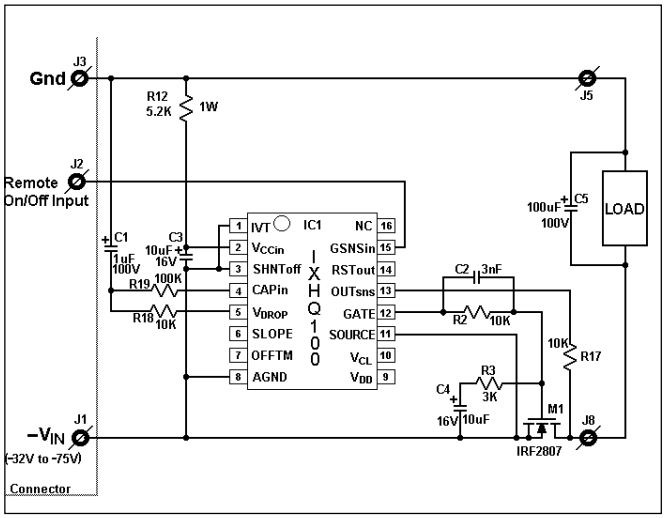
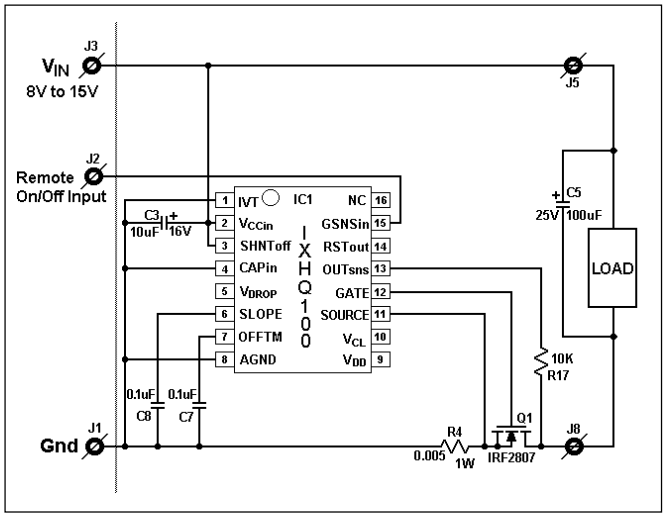
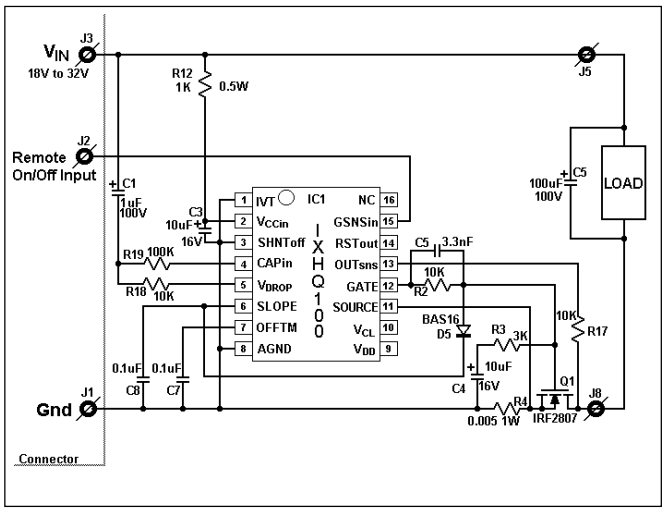
Telecommunication Application
- Active -V_{IN} filter
- Remote On/Off switch



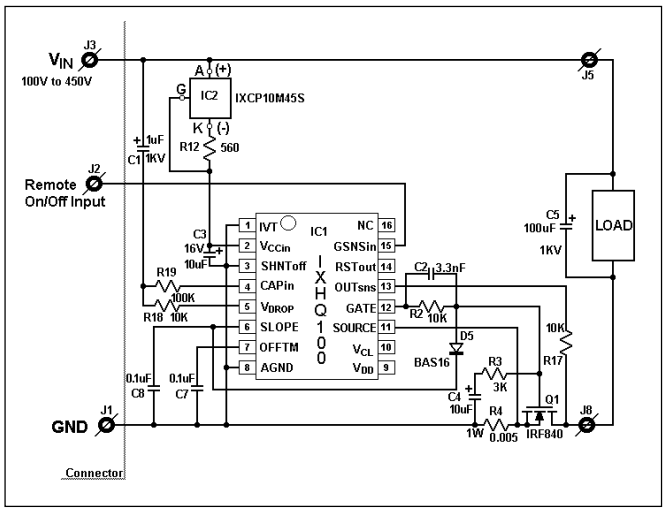
Mobile Application
- Arcless card insertion
- Remote On/Off switch
- Electronic circuit breaker



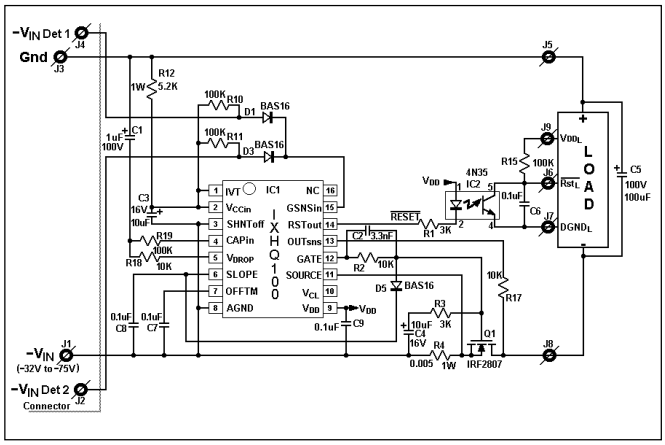
28V Application
- Arcless card insertion
- Ground noise acitve filter
- Remote On/Off switch
- Electronic circuit breaker



Avionic Application
- Arcless card insertion
- Ground noise acitve filter
- Remote On/Off switch
- Electronic circuit breaker



Telecommunication Application with -V_{IN} Detection



- -V_{IN} Detection without Staggered Pins
- Floating Reset Output
- V_{DD} Output (Referred to -V_{IN})
- Adjustable Overcurrent Protection
- Active -V_{IN} filter
- Electronic Circuit Breaker

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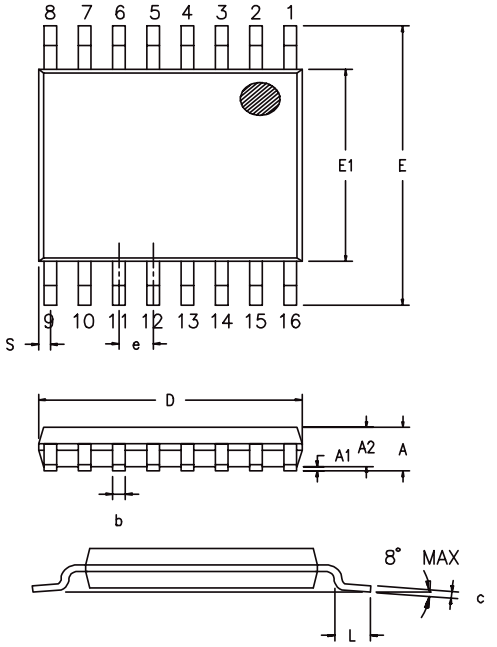
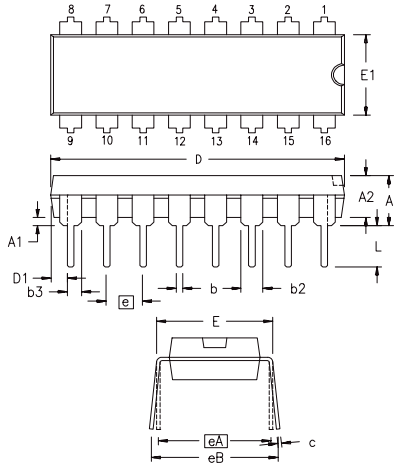
Package Outlines: 16 PIN TSSOP



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.033	.047	0.85	1.20
A1	.002	.006	0.05	0.15
A2	.031	.041	0.80	1.05
b	.007	.012	0.19	0.30
c	.003	.008	0.09	0.20
D	.193	.201	4.90	5.10
E	.252 BSC		6.40 BSC	
E1	.169	.177	4.30	4.50
e	.0256 BSC		0.65 BSC	
L	.018	.030	0.45	0.75
S	.005	.013	0.13	0.33

Package Outlines: 16 PIN PDIP

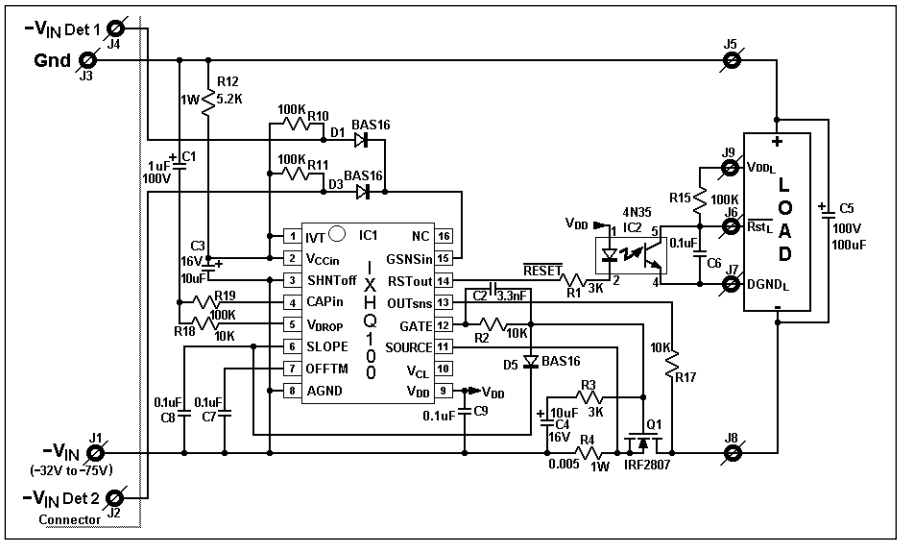


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.745	.800	18.92	20.32
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 AB AND BB.

Ordering Information

Part Number	Package Type	Grade
IXHQ100PI	14 PIN PDIP	Industrial
IXHQ100SI	14 PIN TSSOP	Industrial



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ISOSMART™ Half Bridge Driver Chipset

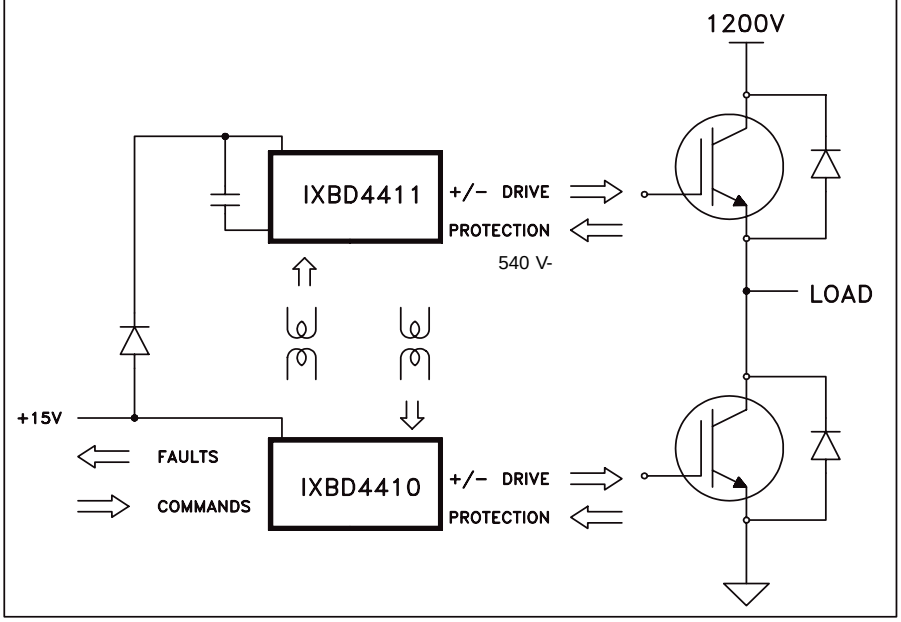
Type	Description	Package	Temperature Range
IXBD4410PI	Full-Feature Low-Side Driver	16-Pin P-DIP	-40 to +85°C
IXBD4411PI	Full-Feature High-Side Driver	16-Pin P-DIP	-40 to +85°C
IXBD4410SI	Full-Feature Low-Side Driver	16-Pin SO	-40 to +85°C
IXBD4411SI	Full-Feature High-Side Driver	16-Pin SO	-40 to +85°C

The IXBD4410/IXBD4411 ISOSMART chipset is designed to control the gates of two Power MOSFETs or Power IGBTs that are connected in a half-bridge (phase-leg) configuration for driving multiple-phase motors, or used in applications that require half-bridge power circuits. The IXBD4410/IXBD4411 is a full-feature chipset consisting of two 16-Pin DIP or SO devices interfaced and isolated by two small-signal ferrite pulse transformers. The small-signal transformers provide greater than 1200V isolation.

Even with commutating noise ambients greater than ±50 V/ns and up to 1200 V potentials, this chipset establishes error-free two-way communications between the system ground-reference IXBD4410 and the inverter output-reference IXBD4411. They incorporate undervoltage V_{DD} or V_{EE} lockout and overcurrent or desaturation shutdown to protect the IGBT or Power MOSFET devices from damage.

The chipset provides the necessary gate drive signals to fully control the grounded-source low-side power device as well as the floating-source high-side power device. Additionally, the IXBD4410/4411 chipset provides a negative-going, off-state gate drive signal for improved turn-off of IGBTs or Power MOSFETs and a system logic-compatible status fault output $\overline{FLT}$ to indicate overcurrent or desaturation, and undervoltage V_{DD} or V_{EE}. During a status fault, both chipset keep their respective gate drive outputs off; at V_{EE}.

FULL FEATURED ISOSMART™ DRIVER CHIP-SET



Features

- 1200 V or greater low-to-high side isolation.
- Drives Power Systems Operating on up to 575 V AC mains
- dv/dt immunity of greater than ±50V/ns
- Proprietary low-to-high side level translation and communication
- On-chip negative gate-drive supply to ensure Power MOSFET or IGBT turn-off and to prevent gate noise interference
- 5 V logic compatible HCMOS inputs with hysteresis
- Available in either the 16-Pin DIP or the 16-Pin wide-body, small-outline plastic package
- 20 ns switching time with 1000 pF load; 100 ns switching time with 10,000 pF load
- 100 ns propagation delay time
- 2 A peak output drive capability
- Self shut-down of output in response to over-current or short-circuit
- Under-voltage and over-voltage V_{DD} lockout protection
- Protection from cross conduction of the half bridge
- Logic compatible fault indication from both low and high-side driver

Applications

- 1- or 3-Phase Motor Controls
- Switch Mode Power Supplies (SMPS)
- Uninterruptible Power Supplies (UPS)
- Induction Heating and Welding Systems
- Switching Amplifiers
- General Power Conversion Circuits

IXYS reserves the right to change limits, test conditions and dimensions.

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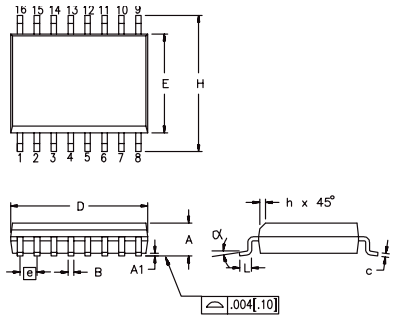
Symbol	Definition	Maximum Ratings	
V_{DD}/V_{EE}	Supply Voltage	-0.5 ... 24	V
V_{in}	Input Voltage (INH, INL)	-0.5...V_{DD} +0.5	V
I_{in}	Input Current (INL, INH, IM)	±10	A
I_o (rev)	Peak Reverse Output Current (OUT)	2	A
P_D	Maximum Power Dissipation	600	mW
T_A	Operating Ambient Temperature	-40 ... 85	°C
T_{JM}	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	-55 ... 150	°C
T_L	Lead Soldering Temperature for 10 s	300	°C

Recommended Operating Conditions

V_{DD}/V_{EE}	Supply Voltage	10 ... 20	V
V_{DD}/LG		10 ... 16.5	V
L_{Gh}/L_{Gl}	Maximum Common Mode dv/dt	±50	V/ns

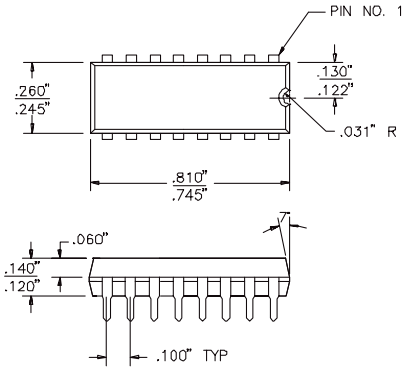
Symbol	Definition/Condition (T_A = 25°C, V_{DD} = 15 V, unless otherwise specified)	Characteristic Values min.	typ.	max.	
INL, INH Inputs (referred to LG)					
V_{t+}	Positive-Going Threshold	3.65			V
V_{t-}	Negative-Going Threshold			1	V
V_{ih}	Input Hysteresis		1		V
I_{in}	Input Leakage Current/V_{in}=V_{DD} or LG	-1		1	µA
C_{in}	Input Capacitance		10		pF
Open Drain Fault Output (referred to LG)					
V_{oh}	HI Output/R_{pu} = 10 kΩ to V_{DD}	V_{DD}-0.05			V
V_{ol}	LO Output/I_o = 4 mA		0.3	0.5	V
OUT Output (referred to LG)					
V_{oh}	HI Output/I_o = -5 mA	V_{DD}-0.05			V
V_{ol}	LO Output/I_o = 5 mA		V_{EE}+0.05		V
R_o	Output HI Res./I_o = -0.1 A		3	5	Ω
R_o	Output LO Res./I_o = 0.1 A		3	4	Ω
I_{pk}	Peak Output Current/C_L = 10 nF	1.5	2		A
IM Input (referred to KG)					
V_{t+}	Positive-Going Threshold	0.24	0.3	0.45	V
C_{in}	Input Capacitance		10		pF
R_s	Shorting Device Output Resistance	50	75	100	Ω
VEE Supply (referred to LG)					
V_{EE}	Output Voltage/I_o = 1 mA, C_o = 1 µF	-5	-6.5	-7.5	V
I_{out}	Output Current/V_{out} = 0.70 • V_{EE}	-20	-25		mA
f_{inv}	Inverting Frequency		600		kHz
V_{EEF}	Undervoltage Fault Indication	-3		-4.8	V

Dimensions in inch (1" = 25.4 mm)
16-Pin SO

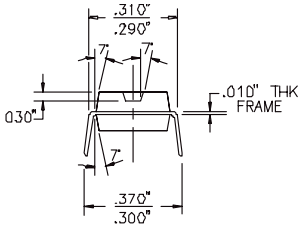


SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
B	.013	.020	.33	.51
C	.009	.013	.23	.32
D	.398	.413	10.10	10.50
E	.291	.299	7.40	7.60
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
h	.010	.029	.25	.75
L	.016	.050	.40	1.27
α	0°	8°	0°	8°

16-Pin Plastic DIP



Cross view



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Symbol	Definition/Condition		Characteristic Values (T_A = 25°C, V_{DD} = 15 V, unless otherwise specified) min.	typ.	max.	
V_{DD} Undervoltage Lockout						
V_{uv}	Drop Out		9.5	10.5	11.5	V
V_{uh}	Hysteresis		0.1	0.15	0.3	V
Quiescent Power Supply Current						
I_{DD}	V_{DD} Current/V_{in}=V_{DD} or LG, I_o = 0				20	mA
INL and INH Inputs (Fig. 1a - 1c)						
$t_{d(on)}$	Turn-on delay time; 4410	C_L =1nF		110	175	ns
t_r	Rise time;	C_L =10 nF		70	100	ns
		C_L =1 nF		15	20	ns
$t_{d(off)}$	Turn-off delay time 4410	C_L =1nF		70	150	ns
t_f	Fall time	C_L =10nF		70	150	ns
		C_L =1nF		15	20	ns
$t_{dlh(off)}$	4410/4412 Turn-on delay time vs. 4411 Turn-off delay time	C_L =1nF		60	150	ns
$t_{dlh(on)}$	4410 Turn-on delay time vs. 4411 Turn-off delay time	C_L =1nF		60	150	ns
Fault Output Delay for any Fault Conditions (4410/4411)						
t_{FLT}	$\overline{FLT}$ Delay/R_{pu} = 2 kΩ	C_L = 20 pF		200	300	ns
Overcurrent Protection Delay						
t_{oc}	Driver-Off delay time	C_L = 1 nF		200	300	ns

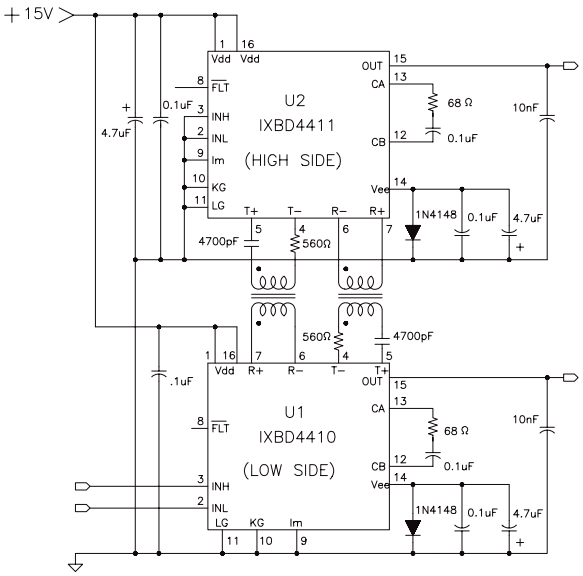

Fig. 1a: IXBD4410/4411 Switching time test circuit

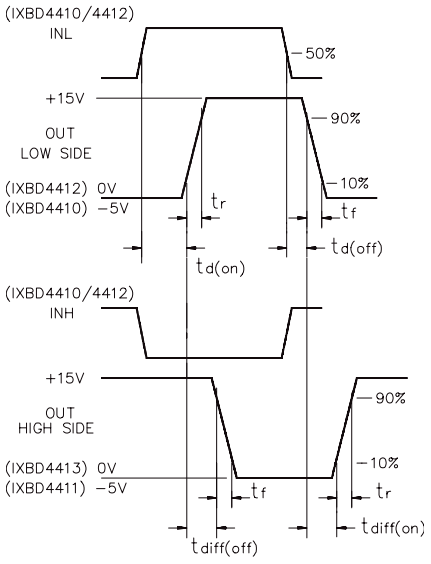

Fig. 1b: Output signal waveform

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Chipset Overview

This ISOSMART™ chipset is a pair of integrated circuits providing isolated high- and low-side drivers for phase-leg motor controls, or any other application which utilizes a half bridge, 2- or 3-phase drive configuration. They consist of two drive control inputs (INL and INH) for two Power-MOSFET/IGBT gate-drive outputs. Both inputs operate from a common ground and are activated by HCMOS compatible logic levels. The low-side output operates near input ground, while the high-side output operates from a floating ground that is nominally the source connection of the high-side phase-leg power device. Both outputs typically provide 2 A of transient current drive for fast switching of the phase-leg power device.

IXBD4410/IXBD4411
The full featured ISOSMART™ driver chipset incorporates a IXBD4410 as the low-side driver (Fig. 3) and a IXBD4411 as the high-side driver (Fig. 2). When input "INL" is set to a positive logic level, the low-side gate output goes high (turns on); when "INH" is set to a positive logic level, the high-side gate drive output goes high. The high-side IC is isolated from the low-side IC by a magnetic barrier, across which the turn on/off signal is transmitted to the high-side gate drive. The IXBD4411 fault signal is also transmitted back to the IXBD4410 driver via these transformers. This isolation only depends on the low cost communica-tions transformer, which is designed to withstand 1200 V or more.

There are two magnetic transmission channels between the low- and high-side IC's for bi-directional communication. One sends a signal from the low-side IXBD4410 IC up to the high-side IXBD4411 IC and the other sends a signal back from the high-side to the low-side IC. The signal that is sent up controls the IXBD4411 gate-drive output. The signal sent from the IXBD4411 back to the IXBD4410 indicates a high-side fault has occurred (overcurrent, or under-voltage of the high-side +power supplies). This is detected at the IXBD4410 driver and sets "FLT" pin low, to indicate the high-side fault.

The fault signal that is returned from the IXBD4411 is strictly for status only. Any gate-drive shutdown because of a high-side fault is done locally within the high-

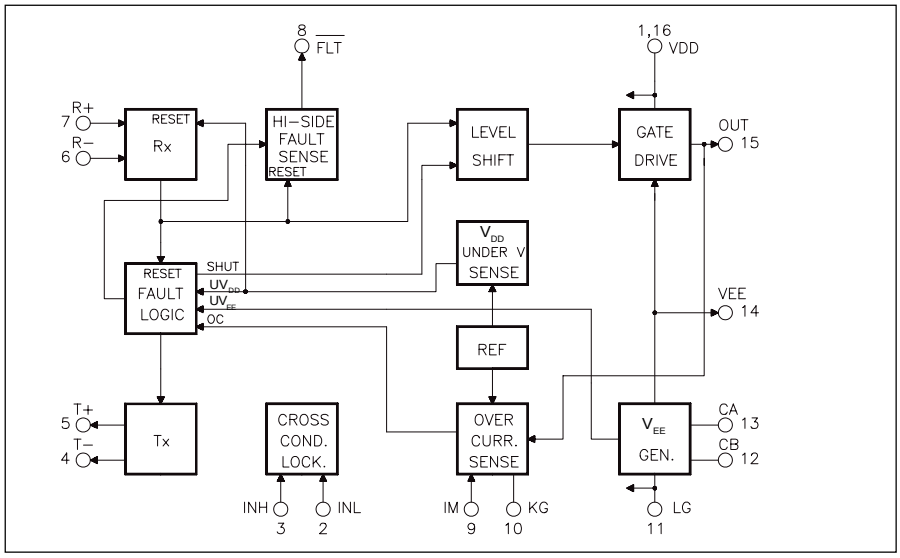

Fig. 2: IXBD4411, high-side driver block diagram

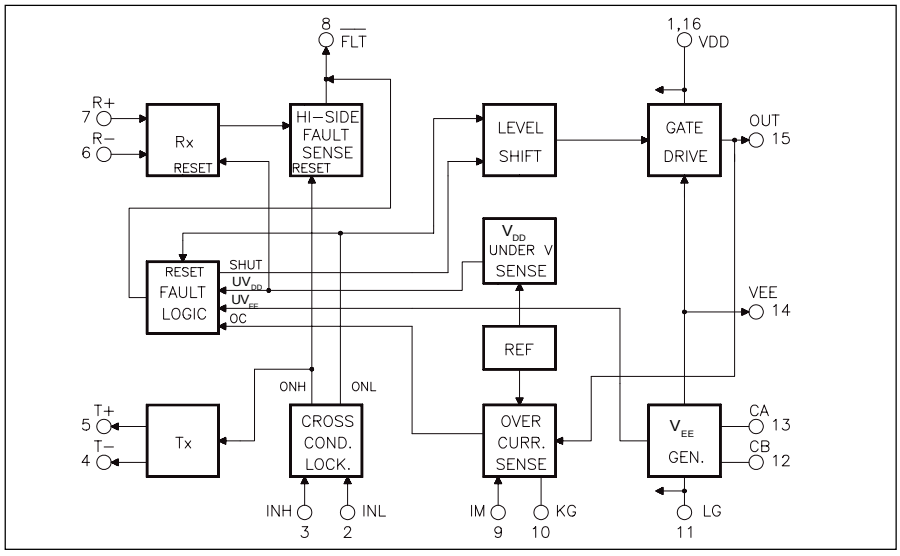

Fig. 3: IXBD4410, low-side driver block diagram

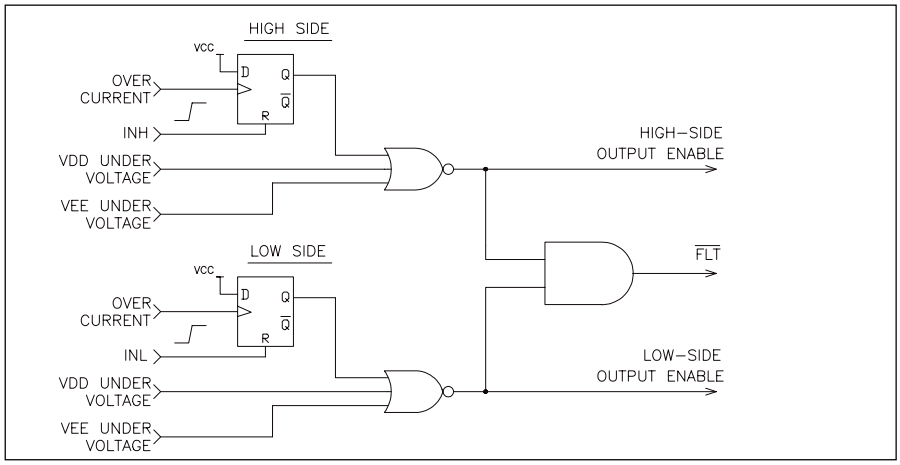

Fig. 4: Logic representation of IXBD4410 $\overline{FLT}$ signal

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side IXBD4411. The IXBD4411 gate-drive will turn-off the power device whenever an overcurrent or under voltage condition arises. The overcurrent sensing is active only while the gate driver output is "high" (on). The overcurrent fault condition is latched and is reset on the next INH gate input positive transition. The FLT (pin 8) of the IXBD4411 is not used and should be grounded.

The low-side IXBD4410 driver provides an output pin 8 (FLT) to indicate a high-side (IXBD4411) **or** a low-side (IXBD4410) fault. This output pin is an "open-drain" output. The IXBD4410 low-side driver fault indications are similar to the IXBD4411 high-side driver indications as outlined above. A "graphic" logic diagram of the chipset's FLT function is presented in Fig. 4. Note that this diagram presents the logic of this function at the "low-side" IXBD4410 driver and is not the actual circuit. It describes the combined logic of the "fault logic" and "hi-side fault sense" blocks in both the IXBD4410 and IXBD4411 as shown in Fig. 2 and 3.

The most efficient method of providing power for the high-side driver is by bootstrapping. This method is illustrated in the functional drawing on page 4 and in the application example (Fig. 6 and 9) by diode D1 and capacitor C1. Using this method, the power is drawn through a high-voltage diode onto a reservoir capacitor whenever the floating high-side ground returns to near the real ground of the low-side driver. When the high-side gate is turned on and the floating ground moves towards a higher potential, the bootstrapping diode back-biases, and the high-side driver draws its power solely from the reservoir capacitor. Power may also be provided via any isolated power supply (usually an extra secondary on the system housekeeping supply switching transformer).

Both the IXBD4410 and IXBD4411 contain on-board negative charge pumps to provide negative gate drive, which ensures turn-off of the high- or low-side power device in the presence of currents induced by power device Miller capacitance or from inductive ground transients. These charge pumps provide -5 V relative to the local driver ground when V_{DD} is at +15 V, and at rated average currents of 25 mA. The charge pump requires two external capacitors, C7 and C11 in Fig. 6. The charge pump frequency is nominally 600 kHz. The charge pump clock is turned off whenever the difference between the V_{DD} and V_{EE} supplies exceed 20 V, to prevent exceeding the breakdown rating of the IC.

Both the IXBD4410 and IXBD4411 drivers possess two local grounds each, a common logic ground, and "Kelvin" ground. The Kelvin ground and logic grounds are first connected directly to each other, and then to the Kelvin-source of the power device for accurate over-current measurement in the presence of inductive transients on the power device source terminal.

Power MOSFET or IGBT overcurrent sensing utilizes an on-chip comparator with a typical 300 mV threshold. In a typical application, the current mirror pin of the Power MOSFET or IGBT is connected to a grounded, low-value resistor, and to the overcurrent comparator input on the high- or low-side driver. The comparator will respond typically within 150 ns to an overcurrent condition to shutdown the driver output. The power switches could be protected also by desaturation detection (see Fig. 6, 7 and 9).

To assure maximum protection for the phase-leg power devices, the chipset incorporates the following Power MOSFET and IGBT protection circuits:

- Power device overcurrent or desaturation protection. The IXBD4410/4411will turn off the driven device within 150 ns of sensing an output overcurrent or desaturation condition.
- Gate-drive lockout circuitry to prevent cross conduction (simultaneous conduction of the low- and high-side phase-leg power devices), either under normal operating conditions or when a fault occurs.
- During power-up, the chipset's gate-drive outputs will be low (off), until the voltage reaches the under-voltage trip point.
- Under-voltage gate-drive lockout on the low- and/or high- side driver when-ever the respective positive power supply falls below 9.5 V typically.
- Under-voltage gate-drive lockout on the low- and high- side driver whenever the respective negative power supply rises above -3 V typically.

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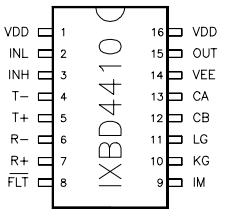
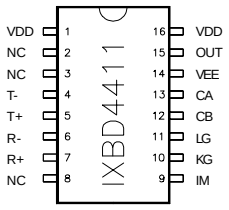
Pin Description
IXBD4410 (Low-Side Driver)



Sym. Pin Description of IXBD 4410/4411

VDD	1 16	Positive power supply.
INL **NC**	2	Logic input signal referenced to LG (logic ground). In the IXBD4410. A "high" to this pin turns on its gate drive output and resets its fault logic. A "low" to this pin turns off the gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). **N**o **C**onnection (IXBD 4411)
INH **NC**	3	Logic input signal referenced to LG (logic ground). In the IXBD4410, this signal is transmitted to the IXBD4411 "high-side" driver through pins 4 and 5 (T- and T+). A "high" to this pin turns on the IXBD4411 gate drive output and resets its fault logic. A "low" to this pin turns off the IXBD4411 gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG). **N**o **C**onnection (IXBD 4411)
T- **T+**	4 5	Transmitter output complementary drive signals. Direct drive of the low signal transformer, which is connected to the receiver of the chipset's companion device. In the IXBD4410, this signal transmits the on/off command to its companion IXBD4411. In the IXBD4411, this signal transmits the fault indication to its companion IXBD4410 driver.
R- **R+**	6 7	Receiver input complementary signal. Directly connected to the low signal transformer, which is driven by the chipset's companion device. In the IXBD4410, this input receives the fault indication from its companion IXBD4411 driver. In the IXBD4411, this input receives the on/off command from its companion IXBD4410 driver.

Pin Description
IXBD4411 (High-Side Driver)



Sym. Pin Description of IXBD 4410/4411

$\overline{\text{FLT}}$ **NC**	8	Low/high side fault output. In the IXBD4410, this output indicates a fault condition of either device of the chipset. A "high" indicates no fault, A "low" indicates that either overcurrent, V_{DD} or V_{EE} under-voltage occurred. In case of overcurrent, this output will remain active "low" until the next input cycle of the respective driver. In case of under-voltage, this output will remain "low" until the proper voltage is restored. The IXBD4411 does not have a $\overline{\text{FLT}}$ output, and its pin 8 should be tied to LG **N**o **C**onnection (IXBD 4411)
IM	9	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 70 Ω resistor. Any voltage at this pin above the threshold of .3 V typical, will turn the output (pin 15) off. This pin is used for power device overcurrent protection.
KG	10	Kelvin ground. This ground is used as Kelvin connection for overcurrent or desaturation sensing.
LG	11	Logic and power ground.
CB **CA**	12 13	Capacitor terminals for negative charge pump (V_{EE}); "+" terminal is CB (pin 12).
VEE	14	Negative supply terminal.
OUT	15	Gate drive output. In the IXBD4410 this output responds to the INL signal. A "high" at INL will turn it on ("high"), a "low" will turn it off ("low"). In the IXBD4411, this output responds to the transmitted signal from the companion IXBD4410. A "high" at INH of the IXBD4410 drives will turn it on ("high"). A "low" will turn it off ("low"). This output will turn off ("low") also in response to any fault condition.

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Application

The IXBD4410/4411 chipset devices are specifically designed as MOS-gated transistor drivers in half-bridge power converters, 1- and 3-phase motor controls, and UPS applications. The phase-leg PWM command is normally generated by previous (user provided) circuitry. It must be decomposed into two separate logic signals, one for the high-side and one for the low-side power transistors, with appropriate deadtime for each state transition. The deadtime insures non-overlapping conduction even if the turn-on and turn-off delay times of the power devices are unequal. The minimum deadtime should be greater than t_{dlh}. A separate circuit, or an IC device like the IXYS deadtime generator IXDP630, can be used to perform this function. The ISOSMART™ chipset family of devices do not generate deadtime, although there is an internal lockout that prohibits one device form being commanded "on" before the other is commanded "off". This simplifies start-up and shutdown protection circuitry, preventing logic error during power-up from turning on both high-and low-side transistors simultaneously.

Negative V_{EE} Charge Pump Circuit Design

The on-chip V_{EE} generator provided in the IXBD4410/4411 generates a negative power supply, regulated at 20 V below the positive V_{DD} rail. If V_{DD} is +10 V, V_{EE} will be -10 V. If V_{DD} is +15 V, V_{EE} will be -5 V. This negative drive potential in the off-state is either desirable or required in many instances. When switching a clamped inductive load (Fig. 5), the turn-on of Q2 will commutate the freewheeling diode around Q1. Whether this diode is intrinsic (as in a MOSFET) or extrinsic (IGBT or bipolar), its reverse recovery is critical to proper circuit operation.

At high turn-on di/dt in Q2 and near its rated voltage, the recovery of D1 can get quite "snappy" (the di/dt in the second half of the recovery process, after the diode has begun to recover its blocking capability, can get very large), creating a very high dv/dt across Q1. This dv/dt is impressed across the Miller capacitance of Q1, forcing a large current to flow out the gate terminal of the device. If this current pulse causes a

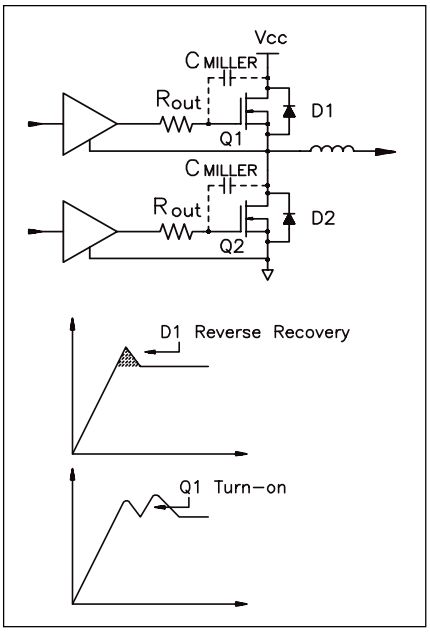

Fig. 5: Switching a clamped inductive load

high enough voltage drop across the output impedance of the gate drive circuit, R_{out}, Q1 will be turned on.

The Q1 conduction in every instance Q2 is turned on (and vice versa), aside from degrading efficiency, can lead to catastrophic failure of both power transistors. At high temperature, where the -6 to -7 mV/°C temperature coefficient of IGBT/MOSFET threshold reduces the voltage required to create a failure, this problem is even more likely to occur. In an industrial module package (e.g.: a 150 A/1200 V IGBT phase-leg module), the series inductance contributed by the long gate leads and connectors further complicate the design.

In a heavily snubbered converter, or in a power supply design with low transformer leakage inductance, the design problem is relatively simple and negative drive is seldom required. However, in a modern snubberless or lightly snubbered converter design, it is important to keep the gate drive impedance high enough during transistor turnoff to limit the reapplied dv/dt (the transistor is its own 'active' snubber). This is always important for EMI control, and in the case of IGBT may be required to achieve the necessary RBSOA. At the same time, it is mandatory to keep the off-state gate drive impedance very low to assure the transistor remain off during induced dv/dt (including diode recovery dv/dt). In some instances, it is simply not possible to satisfy both criteria with 0 V applied in the off-state. In these cases the IXBD4410/4411 with V_{EE} negative bias generator must be used.

The internal V_{EE} generator is a charge pump circuit. Referring to Fig. 6, an external charge pump capacitor is required between the CA and CB

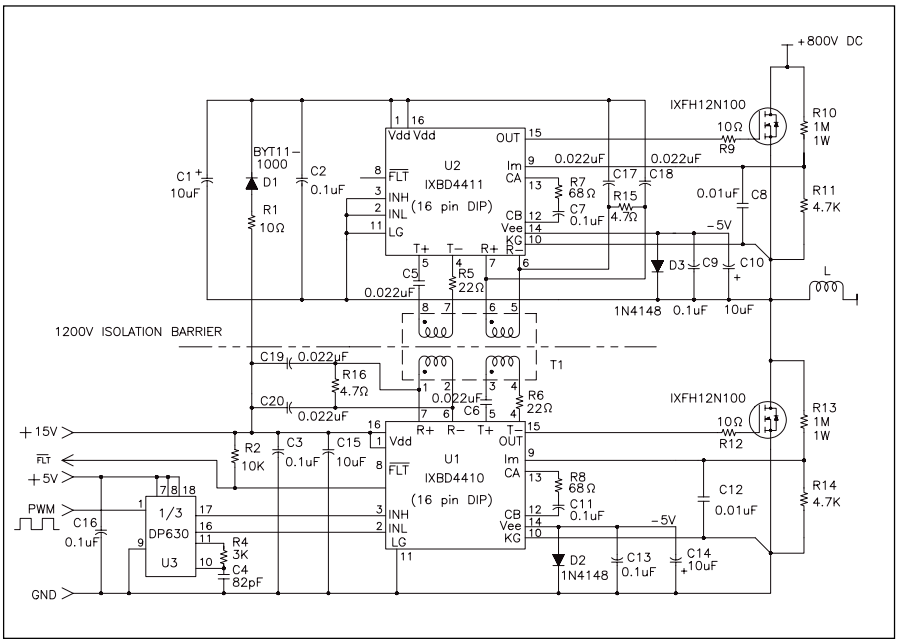

Fig. 6: IXBD4410/4411 Detailed one phase circuit with dead time generator IXDP 630

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terminals (C7, C11), and an output reservoir capacitor between V_{EE} and GND (C10, C14). A 0.1 µF charge pump capacitor (C7, C11) is recommended. The voltage regulation method used in the IXBD4410/4411 allows a 1 to 2 V ripple frequency depends on the size of the V_{EE} output reservoir capacitor (C10, C14) and the average load current. The minimum recommended output reservoir (C10, C14) is 4.7 µF tantalum, or 10 µF if aluminium electrolytic construction is chosen. Note that this reservoir capacitor is in addition to a good quality high frequency bypass capacitor (0.1 µF) that should be placed from VEE to GND (C9, C13).

A small resistor in series with the charge pump capacitor, (R7, R8) reduces the peak charging currents of the charge pump. A value or 68 Ω or greater is recommended, as illustrated in the applications example in Fig. 6.

Current Sense / Desaturation Detection Circuit

All members of the ISOSMART™ driver family provide a very flexible overcurrent/ short circuit protection capability that works with both standard three-terminal power transistors, and with 4- and 5-terminal current sensing power devices. Overcurrent detection is accomplished as illustrated in Fig. 7a (for a current mirror power device) and Fig. 7b (for a standard three terminal power transistor). Desaturation detection is accomplished with the same internal circuits by measuring the voltage across the power transistor in the on-state with an external resistor divider (Fig. 7c).

The IM input trip point V_{TIM}, typically 300 mV, is referenced to the Kelvin ground pin KG.

Current Mirror MOSFET and IGBT allow good control of peak let-through currents and excellent short circuit protection when combined with the ISOSMART™ driver family of devices. The sense resistor is chosen to develop 300 mV at the desired peak transistor current, assuming a mirror ration of 1400:1, and a trip point of 30 A is desired:

R_s = 300 mV • 1400/30 A = 14 Ω
(use 15 Ω CC).

It is important to realize that C_{oss} per unit area of the mirror cells is much larger that C_{oss} per unit area of the bulk of the chip due to periphery effects. This causes a large transient current pulse at the mirror output whenever the transistor switches (C • dv/dt currents), which can cause false overcurrent trigger. The RC filter indicated in Fig. 7a will eliminate this problem.

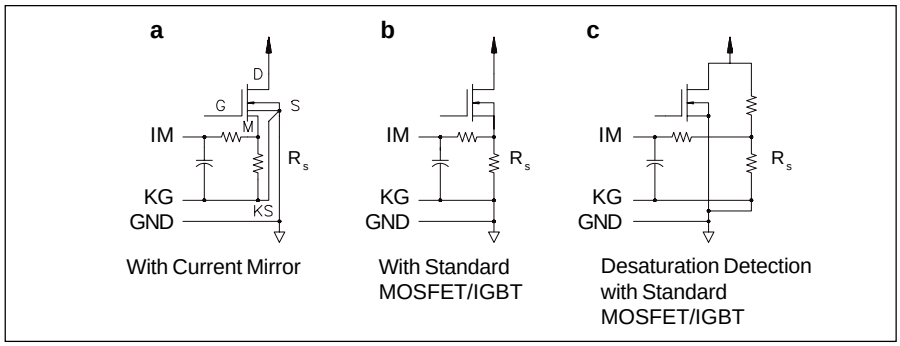

Fig. 7: Alternative overcurrent protection circuits

Standard three-terminal MOSFET and IGBT devices (in discrete as well as modern industrial single transistor and phase-leg modules) can also be protected from short circuit with the ISOSMART™ driver family devices. In discrete device designs, where the source/emitter terminal is available, overcurrent protection with an external power resistor can be implemented. The resistor is placed in series with the device emitter, with the full device current flowing through it (Fig. 7b). The sense resistor is again selected to develop 300 mV at the desired peak transistor current, assuming a trip point of 30 A is desired:

R_s = 300 mV / 30 A = 10 mΩ
(use 10 mΩ, noninductive current sense resistor).

It is important to recognize that "noninductive" is a relative term, especially when applied to current sense resistor construction and characterization. There is always significant series inductance inserted with the sense resistor, and L • di/dt voltage transients can cause false overcurrent trigger.

The RC filter indicated in Figure 7b will eliminate this problem. Choosing the RC pole at the current sense resistor RL zero should exactly compensate for series inductance. Because the exact value is not normally known (and can vary depending on PC layout and component lead dress) this is not normally a good idea. Usually, the RC time constant should be two to ten times longer than the suspected RL time constant.

Desaturation detection as in Figure 7c is probably the most common method of short circuit protection in use today. While not strictly an "overcurrent" detector, if the power transistor gain, and consequently short circuit let-through current, is well controlled (as with modern MOSFET and IGBT) this methodology offers very effective protection.

The IXBD4410/4411 half-bridge circuits in Fig. 6 uses desaturation detection. In Fig. 6, the voltage across the two power MOSFET devices (or IGBTs) are monitored by two sets of voltage-divider networks, R10 and R11 for the high-side gate driver, and R13 and R14 for the low-side gate driver. The dividers are set to trip the IM input comparators when either Power MOSFET device V_{DS} exceeds a reasonable value, perhaps 50 V (usually a value of 10 % of the nominal DC bus voltage works well). R10 or R13 are chosen to tolerate the applied steady state DC bus voltage at an acceptable power dissipation. Dielectric withstand capability, power handling, temperature rise, and PC board creep and strike spacings, must all be carefully considered in the design of the voltage-divider networks.

In the off-state, the voltage across the Power MOSFET device may go as high as the DC bus potential. To keep this normal condition from setting the internal fault flip-flop of the IXBD4410 or the IXBD4411, an internal CMOS switch is turned on and placed across IM and KG pins shorting them together. This effectively discharges C8 or C12 in Fig. 6 and maintains zero potential with respect to KG at IM.

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When the command arrives to switch on the Power MOSFET device, the CMOS switch shorting IM to KG is turned off. The driven Power MOSFET device is switched on approximately 100 ns to 1 µs later, and with typical load conditions, its drain-to-source potential, V_{DS}, may take an additional 10 µs of delay to collapse to the normal on-state voltage level. To prevent false triggering due to this, C8 or C12 in parallel combination with R10 and R11, or R13 and R14, delays the IM input signal. During this turn-on interval, the voltage across C8 or C12 will rise until the Power MOSFET device finally comes on and pulls the voltage across C8 or C12 back down. If the MOSFET device load circuit is shorted, its V_{DS} voltage cannot collapse at turn-on. In this case, the voltage across C8 or C12 rises rapidly until it reaches 300 mV, tripping the fault flip-flop and shutting down the driver output. At the same time, C8 or C12 must be kept small enough that the added delay does not slow down the detection of a short circuit event so much that the Power MOSFET device fails before the driver realizes that it is in trouble. The desaturation detection circuit in Fig. 9 functions identically to the one in Fig. 6 as just described. Current limit or desaturation detection is latched, and reset on a cycle-by-cycle basis with the rising edge of the respective input command.

Three Phase Motor Controls

Fig. 8 is a block diagram of a typical 3-phase PWM voltage-source inverter motor control. The power circuit consists of six power switching transistors with freewheeling diodes around each of them. The control function may be performed digitally by a microprocessor, microcontroller, DSP chip, or user custom IC; or it may be performed by a PC board full of random logic and analog circuits. In any of these cases, the PWM command for all six power transistors is generated in one circuit, and this circuit is usually referred to system ground potential - the bottom terminal of the power bridge.

The ISOSMART™ family of drivers is the interface between the world of control logic and the world of power, 5 V input logic commands precisely control actions at high voltage and current (1200 V and 100 A in a typical application). Fig. 6 is a detailed schematic of one phase of three

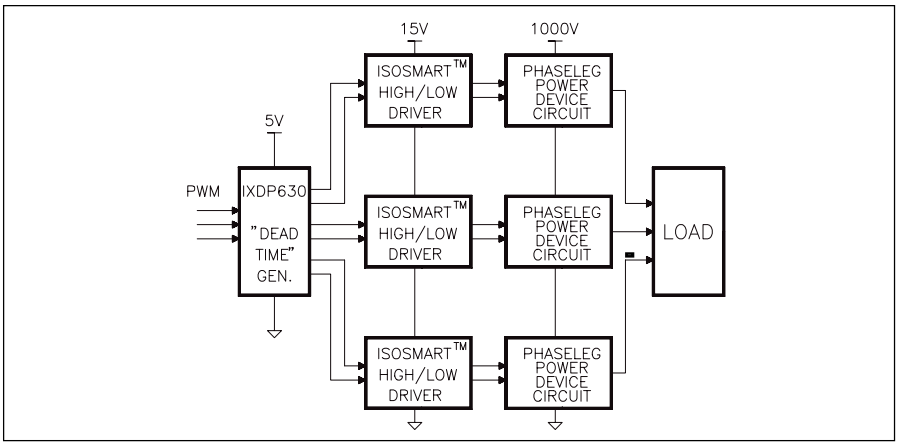

Fig. 8: Typical 3-phase motor control system block diagram

3-phase motor control, showing the interconnection of the IXBD4410/4411 and its associated circuitry.

PCB Layout Considerations

The IXBD4410/4411 is intended to be used in high voltage, high speed, high dv/dt applications.

To ensure proper operation, great care must be taken in laying out the printed circuit board. The layout critical areas include the communication links, current sense, gate drive, and supply bypassing.

The communication path should be as short as possible. Added inductance disturbs the frequency response of the signal path, and these distortions may cause false triggering in the receiver. The transformer should be placed between the two ICs with the orientation of one IC reversed (Fig. 10).

Capacitance between the high- and low-side should be minimized. No signal trace should run underneath the communication path, and high- and low-side traces should be separated on the PCB. The dv/dt of the high-side during power stage switching may cause false logic transitions in low-side circuits due to capacitive coupling.

The low signal pulse transformer provides the isolation between high-and

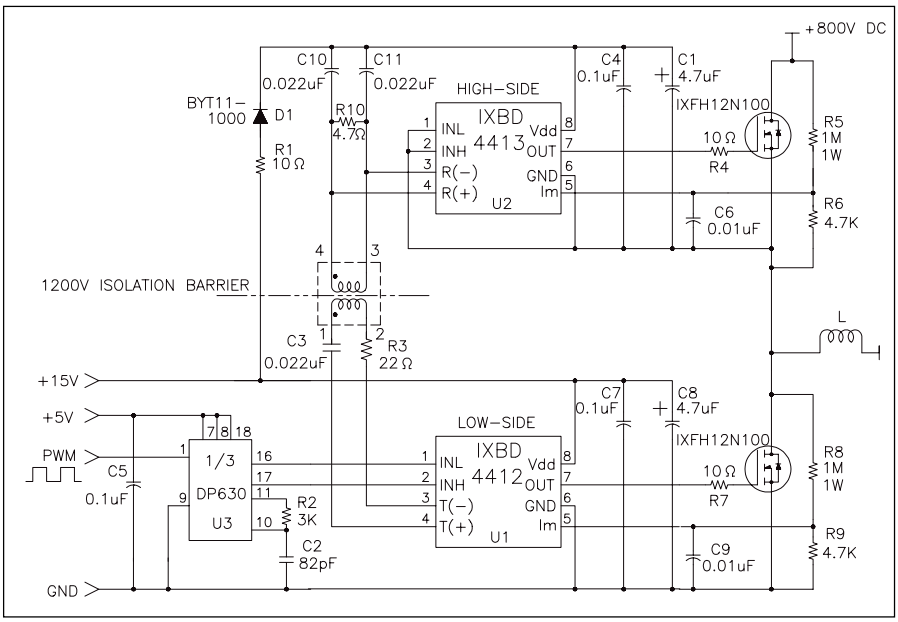

Fig. 9: Lower cost IXBD4412/4413 single phase circuit with deadtime generator IXDP630

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low-side circuits. For 460 V~ line operation, a spacing of 4 mm is recommended between low- and high-side circuits, and a transformer HIPOT specification of at least 1500 V~ is required. This creep spacing is usually adequate to control leakage currents on the PCB with up to 1200 V~ applied after 10 to 15 years of accumulated dust and particulates in a standard industrial environment. In other environments, or at other line voltages, this spacing should be appropriately modified.

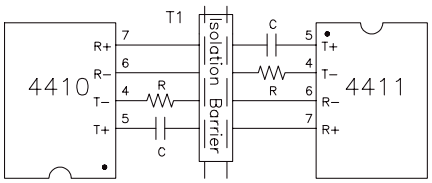

Fig. 10: Suggested IC Orientation

The current sense/desaturation detect input is noise sensitive. The 300 mV trip point is referred to the KG (Kelvin ground) pin, and the applied signal must be kept as clean as possible, A filter is recommended, preferably a monolithic ceramic capacitor placed as close to the IC as possible directly between IM and KG. To preserve maximum noise immunity, the KG pin should first be connected directly to the LG pin, and the pair then sent directly to the power transistor source/emitter terminal, or (if a desaturation detection circuit is used) to the bottom of the divider resistor chain.

All supply pins must be bypassed with a low impedance capacitor (preferably monolithic ceramic construction) with minimum lead length. The output driver stage draws 2 A (typical) currents during transitions at di/dt values in excess of 100 A/µs. Supply line inductance will cause supply and ground bounce on the chip that can cause problems (logic oscillations and, in severe cases, possible latch-up failure) without proper bypassing. These bypass elements are in addition to the reservoir capacitors required for the negative Vee supply and the high-side bootstrapped supply if these features are used.

Power Circuit Noise Considerations

In a typical transistor inverter, the output MOSFET may switch on or off with di/dt >500 A/µs. Referring to Fig.11 and assuming that the MOSFET source terminal has a one inch path on the PCB to system ground, a voltage as high as V = 27 nH • 500 A/µs = 13.5 V can be developed. If the MOSFET switched 25 A, the transient will last as long as (25/500) µs or 50 ns, which is more than the typical 6 or 7 ns propagations or of a 74HC series gate.

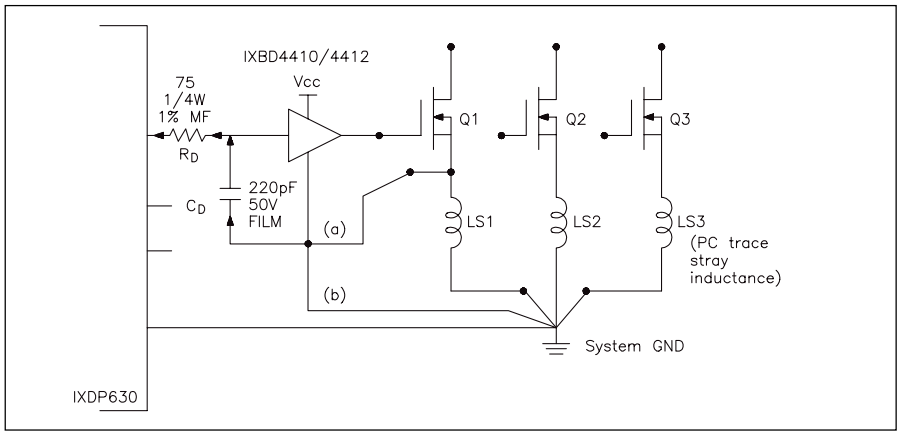

Fig. 11: Potential layout problems that create functional problems

Fig. 11 illustrates an example layout problem. The power circuit consists of three power transistors (MOSFETs in this example). With the ISOSMART™ gate driver chipset grounded as in option (b) in Fig. 11, the communication path from the IXDP630 will operate without errors. The PC trace induced voltages are not common with the digital path, so the input of the gate driver will not see or respond to them.

Unfortunately, the MOSFET will not operate properly. The voltage induced across LS1 when Q1 is turned on, acts as source degeneration, modifying the turn-on behavior of the MOSFET. If LS1= 27 nH, and V_{CC} is 15 V (assuming the gate plateau of the MOSFET is 6 V), the di/dt at turn-on will be regulated by the driver/MOSFET/LS1 loop to about 200 A/µs; quite a surprise when your circuit requires 500 A/µs to operate correctly.

It is possible to make use of this behavior to create a turn-on or turn-off di/dt limiter (perhaps to snub the upper free wheeling diode reverse recovery). While possible, this is normally not desirable or practical where two or more transistors are controlled. Equalizing the parasitic impedances of three traces while positioning the transistors next to their heat sink and meeting UL/VDE voltage spacings is just too difficult.

Grounding the gate driver as in option (a) in Fig. 11 solves the MOSFET turn on problem by eliminating LS1 from the source feedback loop. Now, unfortunately, the gate driver will oscillate every time it is turned on or off. As the IXDP630 output goes "high", the gate drive output follows (after its propagation delay) and the MOSFET starts to conduct. The voltage transient induced across LS1 (V = LS1 • di/dt) raises the local ground (point a) until it exceeds V_{oh} (630) - V_{il} and the driver (after its propagation delay) turns the MOSFET off. Now the MOSFET current falls, V(LS1) drops, point (a) drops to system ground (or slightly below), and the driver detects a "1" at its input. After its propagation delay, it again turns the MOSFET on, continuing the oscillation for one more cycle.

To eliminate this problem, a ground level transformation circuit must be added, that rejects this common mode transient. The simplest is a de-coupling circuit, also illustrated in Fig. 11. The capacitor voltage on C_d remains constant while the transient voltage is dropped across R_d and the driver detects no input transition, eliminating the oscillation. This circuit does add significantly to turn-on and turn-off delay time, and cannot be used if the transient lasts longer than the allowable delays. Delay times must be considered in selection of system dead time.

The most complex (and most effective) method of eliminating the effects of transients between grounds is isolation. Optocouplers and pulse transformers are the most commonly used isolation techniques, and work very well in this

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case. The IXDP630/631 has been specifically designed to directly drive a high speed optocoupler like the Hewlett Packard HCPL22XX family or the General Instrument 740L60XX optologic family. These optos are especially well suited to motor control and power conversion equipment due to their very high common mode dv/dt rejection capabilities.

Transformer Considerations

The transformer is the communication link and isolation barrier between the high- and low-side ICs. The high-side gate and fault signals are transmitted through the transformer while maintaining the proper isolation. The transmitter signal is in the form of a square wave, but the receiver responds only to the logic edges. This allows for much smaller transformer designs, since a 10 kHz switching frequency does not require a 10 kHz pulse transformer.

The recommended transformer for this ISOSMART™ driver chipset is fabricated using a very small ferrite shield bead (see Fig. 12), onto which a six-turn primary and a two-turn secondary winding of 36 AWG magnet wire are made. The two windings are segment wound to achieve primary-to-secondary isolation of up to 2500 V~. The six-turn primaries are connected to the respective IXBD4410/4411 transmitter outputs and the two-turn secondaries are connected to their respective receiver inputs.

The nominal electrical specifications of the transformer are as follows:

- Open circuit inductance (100 kHz; 20 mV): 3 µH
- Interwinding capacitance: 2 pF
- Primary leakage inductance: 0.1 µH
- Turns ratio: 6:2
- Primary-to-secondary isolation (1 min): 1500 V~
- Core permeability (μ_i): 125

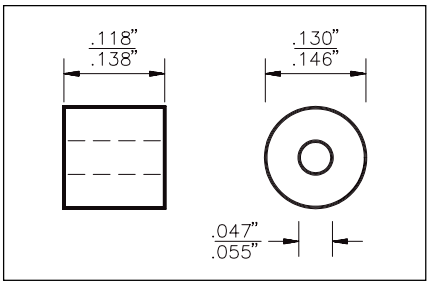

Fig. 12: Ferrite bead dimensions

The recommended ferrite bead is Fair Rite Products part number 2661000101, which is manufactured by:

Fair-Rite Products Corp.
Wallkill, NY
Phone: (800) 836-0427
Web site: www.fair-rite.com

As seen in the application drawings (Fig. 6, 9 and 13) a coupling capacitor (22 nF) and a damping resistor (22 Ω) are added in series with the primary side of the transformer. The capacitor will control the small amount of energy needed to transfer the signal to the companion driver. The resistor will control the damping of the signal and limit the peak transmitter output current. The receiver is designed to operate over a wide common mode input range. To reduce noise pickup, the receiver has ±250 mV of input hysteresis.

If the signal is being distorted at the transmitter, the transmitter is probably running into current limit. A decrease in the coupling capacitance or an increase in the damping resistance should solve this problem. The receiver operates over a wide input range. The minimum amplitude for one side of the receiver is about 1 V and a maximum of about 3 V. It is critical that there be no overshoot on the transformer secondary wave-form. Each signal should be slightly over-damped. If significant overshoot exists, the received signal may be logically inverted. An increase of the damping resistor will solve this problem.

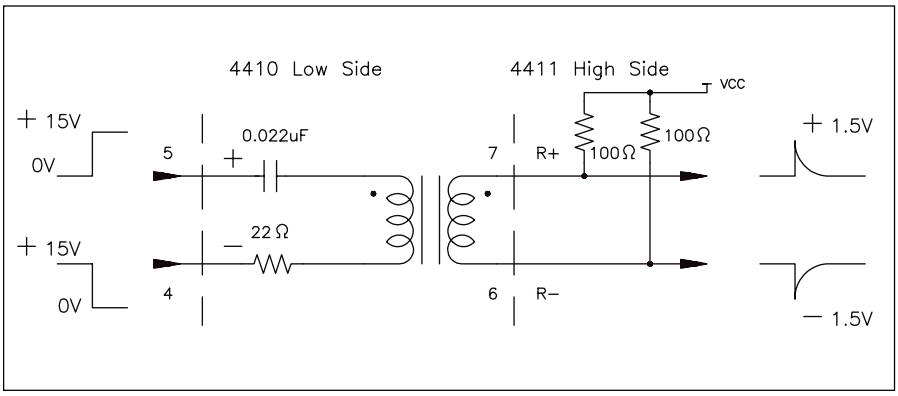

Fig. 13: Transmitter/Receiver Waveforms

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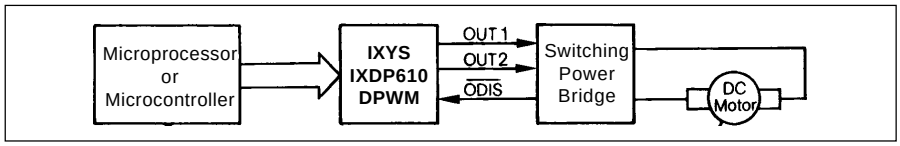
Bus compatible Digital PWM Controller, IXDP 610

Features

- Microcomputer bus compatible
- Two complementary outputs for direct control of switching power bridge
- Dynamically programmable pulse width ranges from 0 to 100 %
- Two modules of operation: 7-bit or 8-bit resolution
- Switching frequency range up to 300 kHz
- Programmable Dead-time Counter prevents switching overlap
- Cycle-by-cycle disable input to protect against over-current,over-temperture, etc.
- Outputs may be disabled under software control
- Special locking bit prevents damage to the power stage in the event of a software failure

Basis system Configuration



The IXDP 610 Digital Pulse Width Modulator (DPWM) is a programmable CMOS LSI device which accepts digital pulse width data from a microprocessor and generates two complementary non-overlapping pulse width modulated signals for direct digital control of a switching power bridge. The DPWM is designed to be operated under the direct control of a microprocessor and interfaces easily with most standard microprocessor and microcomputer buses. The PWM waveform generated by the IXDP 610 results from comparing the output of the Pulse Width Counter to the number stored in the Pulse Width Latch. A programmable "dead-time" is incorporated into the PWM waveform. The Dead-time Logic disables both outputs on each transition of the Comparator output for the required dead-time interval. The output stage provides complementary PWM output signals capable of sinking and sourcing 20 mA at TTL voltage levels. The Output Disable Logic can be activated either by software or hardware. The facilitates cycle-by-cycle current-limit, short-circuit, overtemperature, and desaturation protection schemas. The IXDP 610 is capable of operating at PWM frequencies from zero to 300 kHz, the dead-time is programmable from zero to 14 clock cycles (0 to 11 % of the PWM cycle), which allows operation with fast power MOSFETs, MOSIGBTs, and bipolar power transistors. A trade-off between PWM frequency and reso-lution is provided by selecting the counter resolution to be 7-bit or 8-bit. The 20 mA output drive makes the IXDP 610 capable of directly driving opto isolators and Smart-power devices. The fast response to pulse width commands is achieved by instantaneous change of the outputs to correspond to the new command. This eliminates the one-cycle delay usually associated with digital PWM implementations.

Type	Package	Temperature Range °C
IXDP 610 PI	18-Pin Plastic DIP	-40 to 85

Digital Deadtime Generator, IXDP 630 / 631

Features

- 5 Volt HCMOS logic implementation maintains low power at high speed
- Schmitt trigger inputs and CMOS logic levels improve noise immunity
- Simultaneously injects equal deadtime in up to three output phases
- Replaces 10-12 standard SSI/MSI logic devices
- Allows a wide range of PWM modulation strategies
- Directly drives high speed optocouplers

This 5 Volt HCMOS integrated circuit is intended primarily for application in three-phase sinusoidally commutated brushless motor, induction motor, AC servomotor or UPS PWM modulator control systems. It injects the required deadtime to convert a single phase leg PWM command the two separate logic signals required to drive the upper and lower semiconductor switches in a PWM inverter. It also provides facilities for output disable, fast overcurrent, and fault condition shutdown.
In the IXDP 630 the dead time is set by controlling frequency of the internal oscillator using an external R.C. network. In the IXDP 631 the dead time is achieved by use of an external crystal oscillator. An alternative programming means for both the IXDP 630/631 is by an externally provided clock signal.
Because of its flexibility, the IXDP 630/631 is easily utilized in a variety of brushed DC, trapezoidally commutated brushless DC, hybrid and VR step, or other more exotic PWM motor drive power and control circuit designs.

Type	Configuration	Package	Temperature Range °C
IXDP 630 PI	RC Oscillator	18-Pin Plastic DIP	-40 to 85
IXDP 631 PI	Crystal Oscillator	18-Pin Plastic DIP	-40 to 85

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High Voltage Current Regulators

IXC Series

V_{AK} = 450/350 V
$I_{A(P)}$ = 2 - 100 mA
R_{DYN} = 9 - 900 kΩ

Preliminary Data Sheet

The IXYS IXC series of high voltage current regulators consists of non-switchable, 2-terminal, AC and DC current regulators.

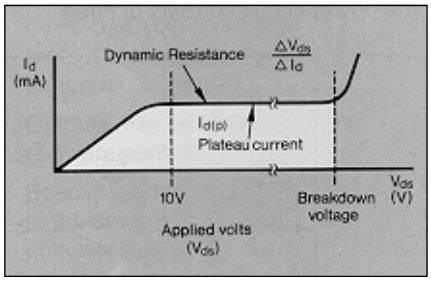


Fig. 1 Current Regulator Output Characteristics

Non-switchable regulators

This is a family of extremely stable, high voltage current regulators with the typical output characteristic shown in Figure 1. The temperature stability is based on a threshold compensation technique and uses IXYS' most recently developed high voltage process. The complete family will be capable of providing other intermediate current levels which can be programmed on-chip during the manufacturing phase.

Specific applications are current sourcing in PABX applications, telephone line terminations, surge protection and voltage supply protection. Two devices in a back-to-back configuration will give bidirectional operation. Specific bidirectional applications would be series surge protection and soft start-up applications from AC mains.

AC non-switchable regulators

This family consists of two DC current regulators connected internally in series to regulate the current to a specified value in both directions. Its output characteristics in quadrants 1 and 3 are the same as shown in Figure 1 so that the current regulation is also the same in both directions.

Current Regulator Nomenclature

Parts can be ordered by using the following nomenclature:

IXCY10M45A (Example)

IX		IXYS
C		Current Regulator
		Package style
P		TO-220 AB
Y		TO-252 (D-PAK)
10		Current Rating, 10 = 10 mA
M		Current Level A = Amps, M = mA, U = μA
45		Voltage rating 45 = 450 V
	(Blank)	DC Non-switchable
	A	AC non-switchable

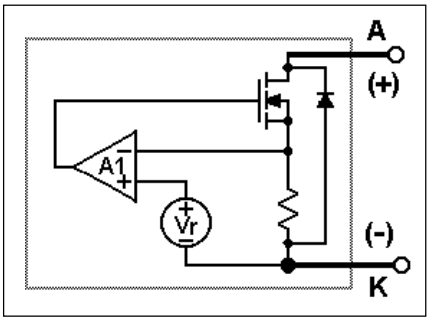
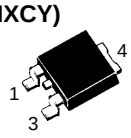
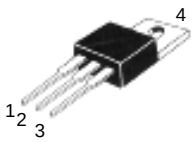


Fig. 2 Block diagram for the non-switchable regulator

TO-252 AA (IXCY)



TO-220 AB (IXCP)



Features

- Extremely stable current characteristics (±50 ppm/K)
- Minimum of 450 V breakdown
- Easily configured for bidirectional current sourcing
- 40 W continuous dissipation
- International standard packages JEDEC TO-220 and TO-252

Applications

- PABX current sources
- Telephone line terminations in PABXs and modems
- Highly stable voltage sources
- Surge limiters and voltage protection (DC and AC)
- Instantaneously reacting resetable fuses
- Waveform synthesizers
- Soft start-up circuits

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Non-Switchable DC Current Regulators

Symbol	Definition		Maximum Ratings	
V_{AK}	Drain Source Voltage		450/350	V
P_D	Power Dissipation	IXC_02M to IXC_50M	25	W
	(T_C = 25°C)	IXC_60M & IXC_100M	40	W
I_{RM}	Maximum Reverse Current		1	A
T_J	Junction Operating Temperature		-55 to +150	°C
T_{stg}	Storage Temperature		-55 to +150	°C
T_L	Temperature for soldering (max. 10 s)		260	°C
M_D	Mounting torque	with screw M3 (TO-220)	0.45/4	Nm/lb.in.
		with screw M3.5 (TO-220)	0.55/5	Nm/lb.in.

Symbol	Definition/Condition			Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{AK}*	Breakdown voltage	__M45	I_D = 1.5 $I_{A(P)}$	450			V
		__M35	I_D = 1.5 $I_{A(P)}$	350			V
$I_{A(P)}$	Plateau Current	02M__	V_{AK} = 10 V	1.9	2.0	2.5	mA
		10M__		9.0	10	11.8	mA
		20M__		18	20	22	mA
		30M__		28	30	35	mA
		40M__		36	40	44	mA
		50M__		45	50	55	mA
		60M__		56	60	64	mA
		100M__		88	100	110	mA
$\Delta I_{A(P)}/\Delta T$	Plateau Current Shift with Temperature		V_{AK} = 10 V		±50		ppm/K
$\Delta V_{AK}/\Delta I_{A(p)}$	Dynamic Resistance	02M__	V_{AK} = 10 V	800	900		kΩ
		10M__		160	180		kΩ
		20M__		78	85		kΩ
		30M__		40	45		kΩ
		40M__		32	35		kΩ
		50M__		19	21		kΩ
		60M__		15	17		kΩ
		100M__		8	9		kΩ
V_F	Diode forward voltage drop; I_F = 50mA					1.8	V

R_{thJC}	Thermal Resistance junction-to-case	IXC_02M to IXC_50M	5.0	K/W
		IXC_60M & IXC_100M	3.1	K/W
R_{thJA}	Thermal Resistance junction-to-ambient	TO-220	80	K/W
		TO-252	100	K/W

* Pulse test to limit power dissipation to within device capability.

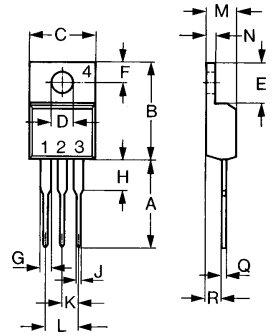
Pin connections

1 = No connection
2, 4 = Positive terminal A
3 = Negative terminal K

Product Marking

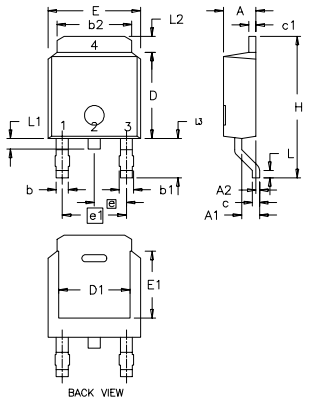
TO-220 types - full part number
TO-252 - last 7 alpha-numeric characters of the part number, e.g. CY02M45

TO-220 AB Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	12.70	13.97	0.500	0.550
B	14.73	16.00	0.580	0.630
C	9.91	10.66	0.390	0.420
D	3.54	4.08	0.139	0.161
E	5.85	6.85	0.230	0.270
F	2.54	3.18	0.100	0.125
G	1.15	1.65	0.045	0.065
H	2.79	5.84	0.110	0.230
J	0.64	1.01	0.025	0.040
K	2.54	BSC	0.100	BSC
M	4.32	4.82	0.170	0.190
N	1.14	1.39	0.045	0.055
Q	0.35	0.56	0.014	0.022
R	2.29	2.79	0.090	0.110

TO-252 AA Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28	BSC	0.090	BSC
e1	4.57	BSC	0.180	BSC
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

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Non-Switchable AC Current Regulators

Symbol	Definition		Maximum Ratings	
V_{AK}	Drain Source Voltage		450/350	V
P_D	Power Dissipation T_C = 25°C)		25	W
T_J	Junction Operating Temperature		-55 to +150	°C
T_{stg}	Storage Temperature		-55 to +150	°C
T_L	Temperature for soldering (max. 10 s)		260	°C
M_D	Mounting torque	with screw M3 (TO-220)	0.45/4	Nm/lb.in.
		with screw M3.5 (TO-220)	0.55/5	Nm/lb.in.

Symbol	Definition/Condition			Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{AK}*	Breakdown voltage at	__M45A	I_D = 1.5 $I_{A(P)}$	450			V
		__M35A	I_D = 1.5 $I_{A(P)}$	350			V
$I_{A(P)}$	Plateau Current	02M__		1.8	2.0	2.5	mA
		10M__	V_{AK} = 10 V	9.0	10	11.8	mA
		20M__		18	20	22	mA
		30M__		28	30	35	mA
		40M__		36	40	44	mA
		50M__		45	50	55	mA
$\Delta I_{A(P)}/\Delta T$	Plateau Current Shift with Temperature		V_{AK} = 10 V		±50		ppm/K
$\Delta V_{AK}/\Delta I_{A(p)}$	Dynamic Resistance	02M__	V_{AK} = 10 V	800	900		kΩ
		10M__		160	180		kΩ
		20M__		78	85		kΩ
		30M__		40	45		kΩ
		40M__		32	35		kΩ
		50M__		19	21		kΩ
V_F	Diode forward voltage drop; I_F = 50mA					1.8	V
R_{thJC}	Thermal Resistance junction-to-case					5	K/W
R_{thJA}	Thermal Resistance junction-to-ambient:				TO-220	80	K/W
					TO-252	100	K/W

* Pulse test to limit power dissipation to within device capability.
Device ratings and characteristics are per chip.

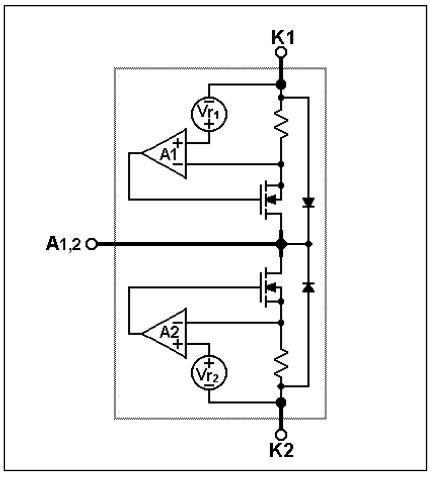

Fig. 3. Equivalent circuit for the AC current regulators.

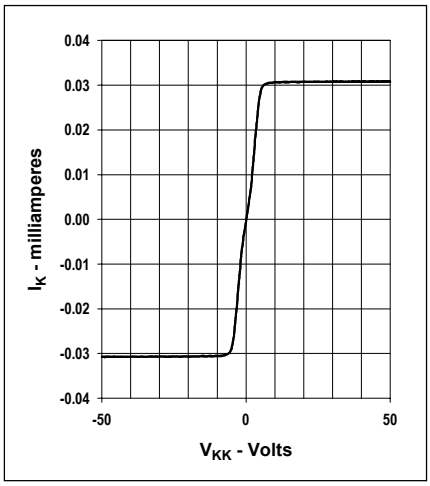

Fig. 4. Output Characteristics for the IXCP30M45A current regulator.

Pin connections

1 = Terminal K1
2, 4 = Terminal A1, 2
3 = Terminal K2

Product Marking

TO-220 types - full part number
TO-252 - last 8 alpha-numeric characters of the part number, e.g. CY02M45A

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Application Examples

DC and AC Overvoltage Suppression

The regulator can be used as a voltage surge suppressor. The device is again connected in series with the lead (Fig. 5) and would normally operate at a current level lower than the plateau (Fig. 6a).

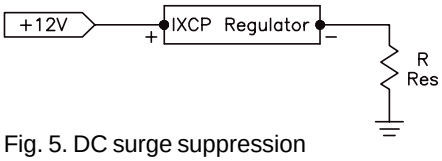


Fig. 5. DC surge suppression

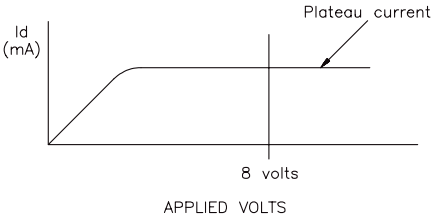


Fig. 6a. DC surge suppression

Any incoming voltage surge (Fig. 6b) less than the breakdown voltage of the regulator will be clamped by the IXCP regulator to voltage less than the plateau current times the effective resistance of the load.

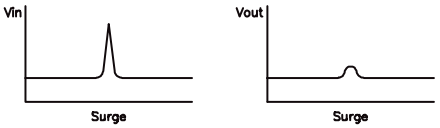


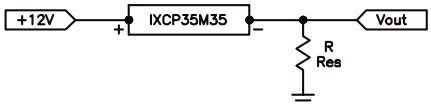
Fig. 6b. Incoming surge/output surge across load

Soft Start-Up Circuits

Here the regulator characteristic will clamp initial current surges which can occur when power is initially applied to a load. The device, with its 450 V capability could, for example, be used with a DC power supply or with AC mains to limit the initial high inrush of current into lamp filaments, thereby increasing the filament life several times. It could, therefore, be used effectively in lighting displays and in the transportation lighting industries.

Highly Stable Voltage Sources

Another obvious application would be to use the current regulator as a source of a highly stable current to produce a usable voltage reference (Fig. 7). This would be effectively independent of temperature and a low cost approach. A high voltage reference is also possible, thanks to their high breakdown voltages.



R = 100 Ω V_{out} = 3.5 V nominal
R = 50 Ω V_{out} = 1.75 V nominal
R = 25 Ω V_{out} = 0.875 V nominal

Fig. 7. Simple voltage source with high stability

Instantaneous "Fuse"

Another application would be protection against sudden voltage droops on voltage supply lines to logic cards in computing systems, resulting from one component suddenly shorting to ground. Normal fusing networks will draw considerable current during the time it takes for the fuse to clear. This could cause a sufficient dip in power rail voltage to cause malfunctions of the other logic cards, even with fast-blow fuses (Fig. 8). The current regulator in series with the logic card restricts the current to its own operating level (Fig. 9). Therefore the voltage supply does not become overloaded and the regulator remains intact.

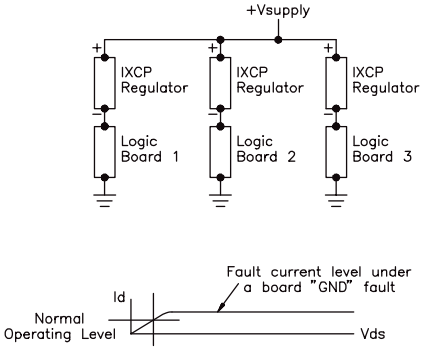


Fig.8. Low cost current regulators instead of fuses

The current regulator thus provides an "instantaneous fusing" function. When the logic component is replaced, the regulator resumes its normal functioning mode.

The obvious advantages to having this regulator as fuse substitute are:

- Prevents a "dip" in the power supply during a fault condition
- Regulator remains intact
- Can be easily tied in with logic to indicate a "down state" board

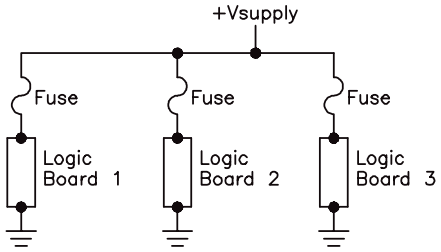


Fig. 9. Normal fusing links in series with each board

Testing & Handling Recommendations

- For initial assessment of the parts where the customer may test the device characteristics in free air without heat sinking, the continuous power dissipation should be kept within 1.5 W at ambient of 25°C. (R_{thJA} = 80 K/W for TO-220, and R_{thJA} = 100 K/W for TO-252)
- Normal electrostatic handling precautions for MOS devices should be adhered to.

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IXYS

Switchable Current Regulators

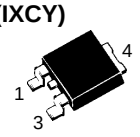
IXCP 10M35S
IXCY 10M35S
IXCP 10M45S
IXCY 10M45S

V_{AK} = 350/450 V
$I_{A(P)}$ = 2 - 100 mA
R_{DYN} = 9 - 900 kΩ

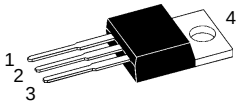
Symbol	Test Condition		Maximum Ratings	
V_{AKR}	T_J = 25°C to 150°C	10M35S	350	V
		10M45S	450	V
V_{AGR}	T_J = 25°C to 150°C	10M35S	350	V
V_{AGR}		10M45S	450	V
V_{GK}			±20	V
I_D	T_C = 25°C		-0.3	A
P_D	T_C = 25°C		40	W
T_J			-55 ... +150	°C
T_{stg}			-55 ... +150	°C
T_L	Temperature for Soldering (max. 10 s)		260	°C
M_D	Mounting torque	with screw M3 (TO-220)	0.45/4	Nm/lb.in.
		with screw M3.5 (TO-220)	0.55/5	Nm/lb.in.

Symbol	Test Condition		Characteristic Values (T_J = 25°C unless otherwise specified) min.	typ.	max.	
V_{AKR}	R_K = 300 Ω, (Fig. 4)	10M35S	350			V
		10M45S	450			V
$I_{A(P)}$	V_D = 10 V; R_K = 300 Ω; (Fig. 5)		7	10	15	mA
$V_{G(off)}$	I_D = 100 µA; V_D = 300 V	10M35S	-5			V
	I_D = 100 µA; V_D = 400 V	10M45S	-5			V
	Fig. 4					
I_{AV}	V_D= 300 V; V_{GK} = -10 V	10M35S			25	µA
	V_D= 400 V; V_{GK} = -10 V	10M45S			25	µA
	Fig. 4					
$\Delta V_{AK}/\Delta I_{A(p}$	Dynamic resistance; V_D= 10 V		10			kΩ
	R_K = 300 Ω; (Fig. 4)					
R_{thJC}	Thermal Resistance junction-to-case				3.1	K/W
R_{thJA}	Thermal Resistance junction-to-ambient	TO-220			80	K/W
		TO-252			100	K/W

TO-252 AA (IXCY)



TO-220 AB (IXCP)



Pin connections

1 = G, Control terminal;
2 and 4 = A (+) Positive terminal
3 = K (-), Negative terminal

Features

- Minimum of 350/450 V breakdown
- Resistor programmable current source
- 40 W continuous dissipation
- International standard packages JEDEC TO-220 and TO-252
- On/Off switchable current source

Applications

- Start-up circuits for SMPS
- Highly stable voltage sources
- Surge limiters and voltage protection
- Instantaneously reacting resetable fuses
- Soft start-up circuits

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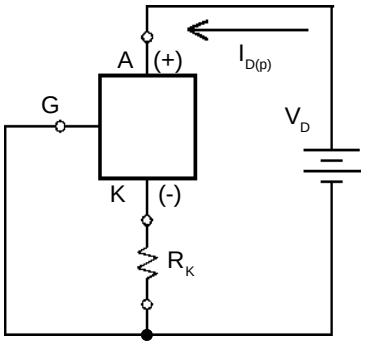


Fig. 1 Resistor R_K in series with negative pin to achieve different current levels

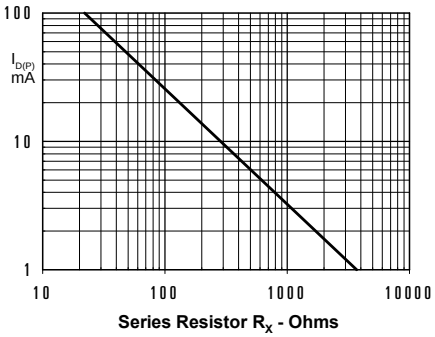


Fig. 2. Plateau current versus external resistance

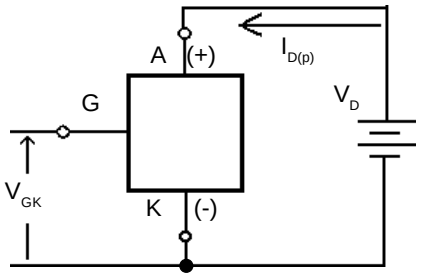


Fig. 3. Current regulator controlled by V_G

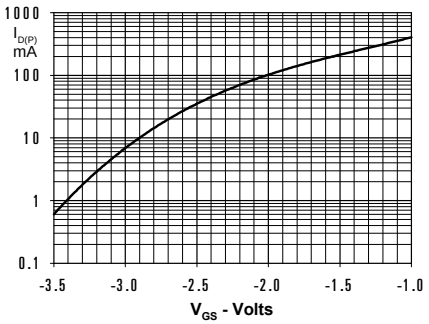
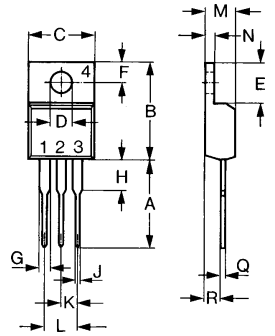


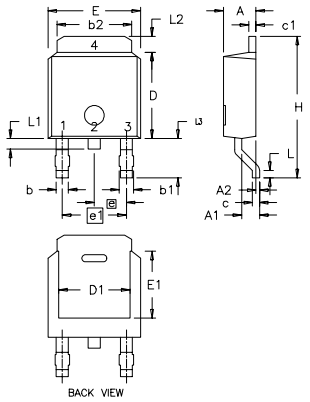
Fig. 4. Plateau current versus applied input voltage

TO-220 AB Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	12.70	13.97	0.500	0.550
B	14.73	16.00	0.580	0.630
C	9.91	10.66	0.390	0.420
D	3.54	4.08	0.139	0.161
E	5.85	6.85	0.230	0.270
F	2.54	3.18	0.100	0.125
G	1.15	1.65	0.045	0.065
H	2.79	5.84	0.110	0.230
J	0.64	1.01	0.025	0.040
K	2.54	BSC	0.100	BSC
M	4.32	4.82	0.170	0.190
N	1.14	1.39	0.045	0.055
Q	0.35	0.56	0.014	0.022
R	2.29	2.79	0.090	0.110

TO-252 AA Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28	BSC	0.090	BSC
e1	4.57	BSC	0.180	BSC
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	2.54	2.92	0.100	0.115

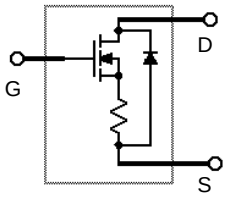
IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Gate Controlled Current Limiter

N-Channel, Enhancement Mode

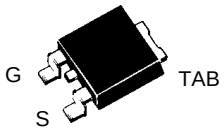
IXCP 01N90E
IXCY 01N90E

V_{DSS} = 900 V
$I_{D(limit)}$ = 250 mA
$R_{DS(on)}$ = 80 Ω

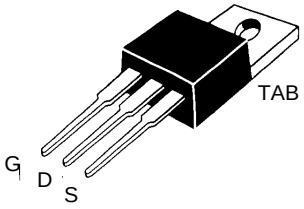


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	900	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	900	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
P_D	T_C = 25°C	40	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
M_d	Mounting torque with 3.5mm screw TO-220	0.55/5	Nm/lb.in.
Weight	TO-252 = 1 g, TO-220 = 4 g		

TO-252 (IXCY)



TO-220 (IXCP)



G = Gate, D = Drain,
S = Source, TAB = Drain

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 25 μA	900			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 25 μA	2.5		5	V
I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0			±50	nA
I_{DSS}	V_{DS} = $V_{DSS;}$ V_{GS} = 0 V			10	μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 mA Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			80	Ω
I_{DP}	Plateau Current; V_{DS} = 10 V, V_{GS} = 10V Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %	100		130	mA

Features

- High output resistance in the saturated mode of operation
- Rugged HDMOS™ process
- Stable peak drain current limit
- High voltage current regulator
- International standard packages

Applications

- Current regulation
- Over current and over voltage protection for sensitive loads
- Linear regulator

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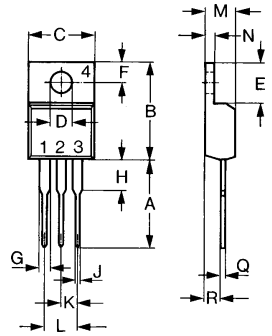
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 20 V; I_D = 100 mA, pulse test			40	mS
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		133		pF
C_{oss}			24		pF
C_{rss}			6.6		pF
$t_{d(on)}$	V_{DS} = 500 V, I_D = 50 mA V_{GS} = 10 V, R_G = 50 Ω (External)		15		ns
t_r			137		ns
$t_{d(off)}$			11		ns
t_f			131		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 500 V, I_D = 50 mA		7.5		nC
Q_{gs}			2.2		nC
Q_{gd}			3.0		nC
$\Delta I_{A(P)}/\Delta T$	Plateau Current Shift with Temperature V_{DS}= 10 V, V_{GS}= 10 V		±50		ppm/K
$\Delta V_{AK}/\Delta I_{A(p)}$	Dynamic Resistance V_{DS} = 10 V, V_{GS}= 10 V		125		kΩ
V_F	I_F = 50mA			1.8	V
R_{thJC}				3.1	K/W
R_{thCA}	TO-220		80		K/W
	TO-252		100		K/W

TO-220 AB Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
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M	4.32	4.82	0.170	0.190
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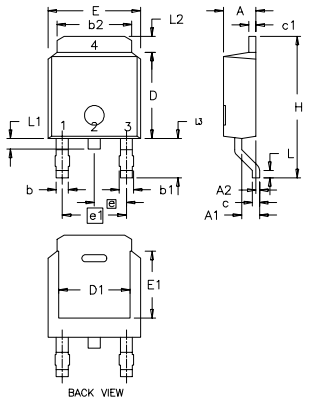
TO-252 AA Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
A2	0	0.13	0	0.005
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.32	5.21	0.170	0.205
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.170	0.205
e	2.28	BSC	0.090	BSC
e1	4.57	BSC	0.180	BSC
H	9.40	10.42	0.370	0.410
L	0.51	1.02	0.020	0.040
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
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I

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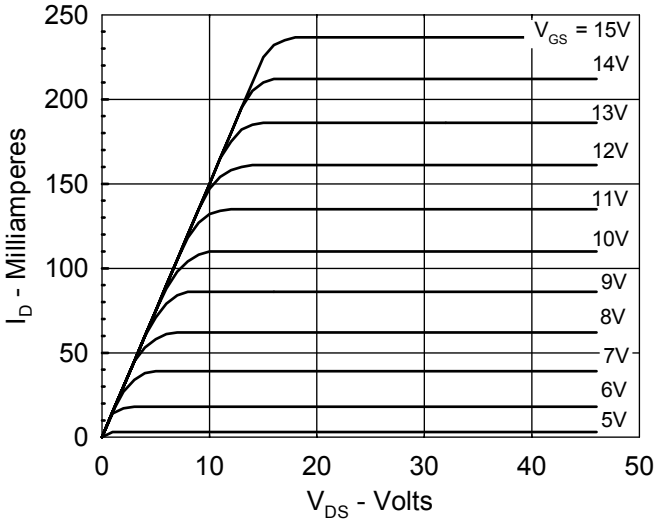

Figure 1, Output Characteristics at

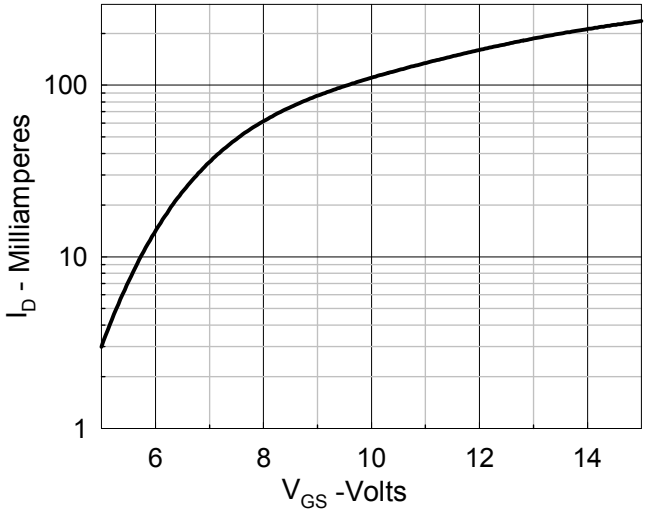

Figure 2. Drain Current vs.Gate Voltage

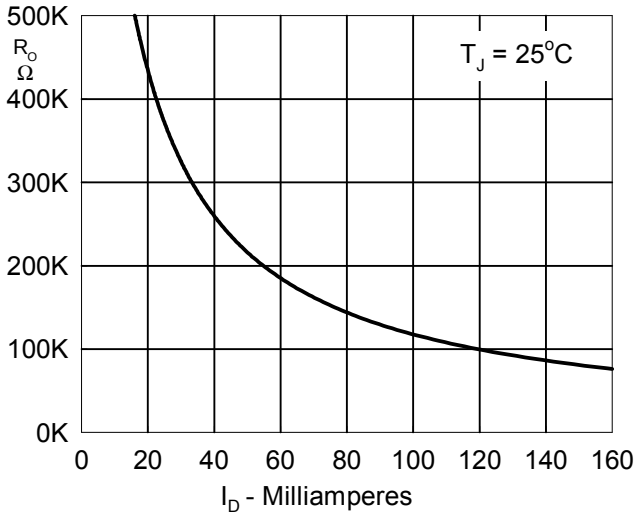

Figure 3. Dynamic Output Resistance R_O vs. Drain Current.

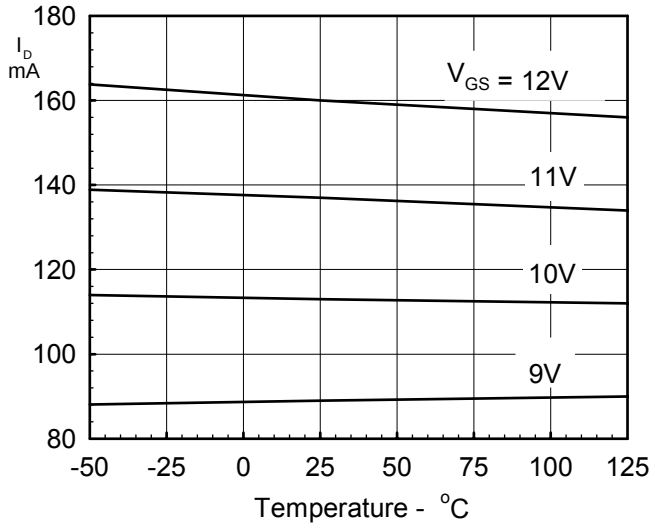

Figure 4. Drain Current vs, Temperature for a constant gate-source voltage.

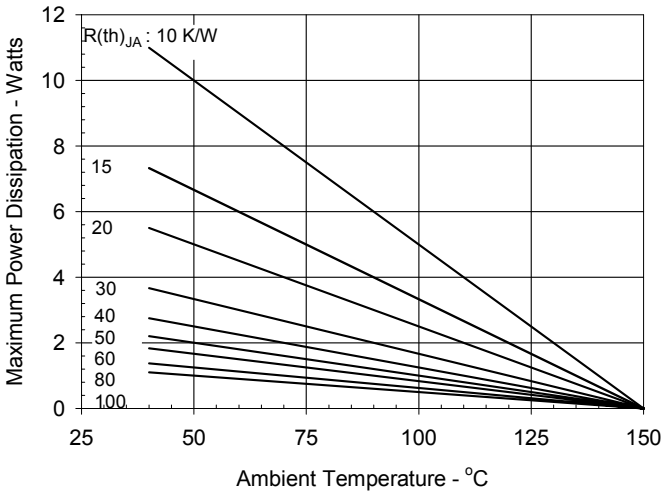

Figure 5. Allowable Power Dissipation for various heat sinking conditions. Note that the junction temperature can be derated by increasing the ambient temperature a like amount.

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Dual Pulse Width Modulation Controller, IXMS 150

Features

- Two complete, synchronous PWMs
- Wide frequency range: 10 kHz to 400 kHz
- 1 % gain matching between channels without external trim
- 1.6 % gain linearity
- Feedforward compensation to remove supply voltage ripple from load current
- Only 1 current sense resistor per phase
- Onchip overcurrent and short circuit protection
- Undervoltage lockout assures proper operation during power-up and -down
- Enable input for external fault protection

Applications

- Full, half, quarter, or microstepping 2-phase step motor position controller
- Dual DC servo motor torque controller
- Solenoid actuator force controller
- General 2-channel current-commanded PWM control

The IXMS is a high performance monolithic 2-channel PWM controller. It is designed and intended specifically to control the current in two independent PWM load circuits. Implemented in CMOS, the low-power IXMS 150 precisely controls the current in each of two separate power drivers (typically H-bridge power circuits) using unique sampling and signal processing techniques. Each channel contains an error amplifier, PWM, feedback amplifier, and protection circuitry. Protection features include over/excess current shutdown, min/max duty cycle clamp, undervoltage lockout, dead time insertion, and a shutdown input for over-temperature or other external fault circuitry. Other features are a common oscillator, feedforward circuit for motor supply compensation, and an on-chip negative bias generator.

The IXMS 150 has been optimized for microstep control 2-phase step motors. Due to its high accuracy, it allows a control system resolution in excess of 250 microsteps per step, or 50,000 steps per revolution with a 200 step motor. This greatly improves position resolution and accuracy, and virtually eliminates low speed velocity ripple and resonance effects at a fraction of the cost of a board-level microstepping system. Other applications that are ideal for the IXMS 150 include control of one or two DC servo motors, 2-phase AC motors, and synchronous reluctance motors in X-Y stage, plotters, printers, paper-handling systems, and robotics.

Type	Package	Temperature Range °C
IXMS 150 PSI	24-Pin Skinny DIP	-40 to 85

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