

DSPs and Paradigm Technology SRAMs

DSP chipsets are being built today with increasing SRAM (and other memory ROM, EEPROM, FLASH, etc.) integrated onto the silicon (50K words of SRAM in one case). Applications though are growing and clever hardware designers are coming up with new tricks to improve performance. This often requires significant expansion of internal memory outside the chipset. Paradigm's broad asynchronous memory offering compliments these requirements.

Texas Instruments DSPs

The TI TMS320 has numerous versions. The C3x has an external interface which can support X8, X16 and X32 of data SRAMs as well as X16 and X32 program memory. The C4x has two 32-bit buses which can address up to 2-G words of external memory. The C44 has two 24-bit busses which can address up to 16-M words of external memory. The C40 (the original member of the C4x family) can address 4-g of external memory. The C5x has a 16-bit address bus which, with control lines, can address 64K of data (64K of program usually in ROM, 64K of I/O and 32K global memory). The C8x supports 8, 16, 32 and 64 bit wide memories with 4G of addressing at 100 MFLOPs. The processor speed directly relates to the access time required and is identified with the table below. There is an attached drawing that shows a typical Fax Modem

block diagram. Specifically, it is a typical TI, but is generic enough to represent most designs.

Rockwell DSPs

The Rockwell DSP uses a non-multiplexed external bus with 8 data lines and 17 address lines, separate read and write control lines, and three chip select lines (romsel, ramsel and one other). Rockwell modem memory option recommendation:

FAMILY	SRAM SIZE	ACCESS TIME
RC336	32K byte (4K x 8)	45ns
RC56	32K byte (4K x 8)	45ns*
RC56	128K byte (16K x 8)	15ns*
RCDL56	128K byte (16K x 8)	15ns

*NOTE. If the RC56 uses ROM with access times of 45ns, then static RAM at equal speed is sufficient for full speed operation, but if slow 90ns ROM is used, then the static RAM must be 15ns for full speed operation.

Although the above referenced SRAM sizes are quite small, the 17 address lines allow for 128K x 8 of external memory which would be shared between ROM, SRAM and any other expansion devices. The external SRAM speeds would be at the listed access times in the table.

Texas Instrument DSP Speed vs. SRAM Memory Access Time

DSP Speed in MHz	100	90	80	70	60	50	40
SRAM Access Time	10	10	12	14	16	20	25
64Kx16, 3 volt	PDM31532 10ns	PDM31532 10ns	PDM31532 12ns	PDM31532 15ns	PDM31532 15ns	PDM31532 20ns	PDM31532 20ns
64Kx16, 5 volt	PDM41532 10ns	PDM41532 10ns	PDM41532 12ns	PDM41532 15ns	PDM41532 15ns	PDM41532 20ns	PDM41532 20ns
32Kx16, 3 volt 10ns	PDM31516 10ns	PDM31516 12ns	PDM31516 15ns	PDM31516 15ns	PDM31516 20ns	PDM31516 20ns	PDM31516
32Kx16, 5 volt 10ns	PDM41516 10ns	PDM41516 12ns	PDM41516 15ns	PDM41516 15ns	PDM41516 20ns	PDM41516 20ns	PDM41516
32KX8, 3 volt	PDM31256 10ns	PDM31256 10ns	PDM31256 12ns	PDM31256 15ns	PDM31256 15ns	PDM31256 20ns	PDM31256 20ns
32KX8, 5 volt	PDM41256 10ns	PDM41256 10ns	PDM41256 12ns	PDM41256 15ns	PDM41256 15ns	PDM41256 20ns	PDM41256 20ns
512Kx8, 3 volt			PDM31096 12ns	PDM31096 15ns	PDM31096 15ns	PDM31096 20ns	PDM31096 20ns
128Kx8, 3 volt 10ns	PDM31034 10ns	PDM31034 12ns	PDM31034 12ns	PDM31034 15ns	PDM31034 20ns	PDM31034 20ns	PDM31034

