

**Features**

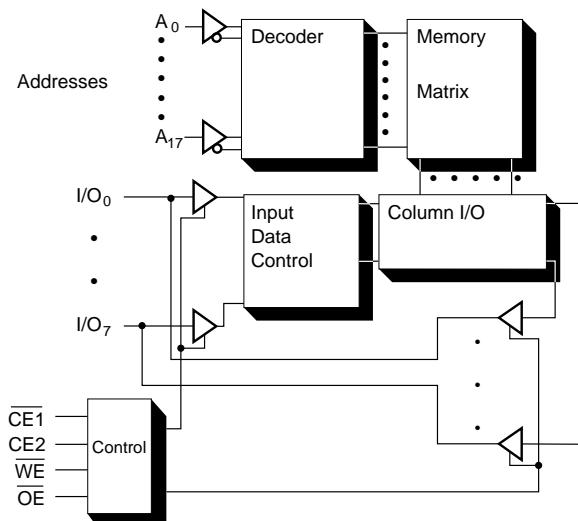
- High-speed access times  
Com'l: 70, 85 and 100ns
- Low power operation (typical)
  - PDM31048LL
  - Active: 65 mW
  - Standby: 7 $\mu$ W
- Single +3.3V ( $\pm 0.3V$ ) power supply
- TTL-compatible inputs and outputs
- I/Os are 5V tolerant
- Low data retention voltage: 1.5V
- Packages
  - Plastic TSOP (I) - T
  - Plastic STSOP (I) - ST

**Description**

The PDM31048LL is a very low power CMOS static RAM organized as 131,072 x 8 bits. Writing to this device is accomplished when the write enable ( $\overline{WE}$ ) and the chip enable ( $\overline{CE1}$ ) inputs are both LOW, and  $CE2$  is high. Reading is accomplished when  $\overline{WE}$  and  $CE2$  remain HIGH and  $\overline{CE1}$  and  $\overline{OE}$  are both LOW.

The PDM31048LL operates from a single +3.3V power supply and all the inputs and outputs are fully TTL-compatible. The device supports low data retention voltage for battery back-up operation with low current.

The PDM31048LL is available in a 32-pin plastic TSOP (I) and a 32-pin plastic STSOP (I).

**Functional Block Diagram**

## Pin Configurations

### TSOP (I), STSOP (I)

A11	1	32	OE
A9	2	31	A10
A8	3	30	CE1
A13	4	29	I/O7
WE	5	28	I/O6
CE2	6	27	I/O5
A15	7	26	I/O4
Vcc	8	25	I/O3
A17	9	24	Vss
A16	10	23	I/O2
A14	11	22	I/O1
A12	12	21	I/O0
A7	13	20	A0
A6	14	19	A1
A5	15	18	A2
A4	16	17	A3

### Pin Description

Name	Description
A17-A0	Address Inputs
I/O7-I/O0	Data Inputs/Outputs
OE	Output Enable Input
WE	Write Enable Input
CE1, CE2	Chip Enable Inputs
V <sub>CC</sub>	Power (+3.3V)
V <sub>SS</sub>	Ground

### Truth Table

OE	WE	CE1	CE2	I/O	MODE
X	X	H	X	Hi-Z	Standby
X	X	X	L	Hi-Z	Standby
L	H	L	H	D <sub>OUT</sub>	Read
X	L	L	H	D <sub>IN</sub>	Write
H	H	L	H	Hi-Z	Output Disable

NOTE: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = DON'T CARE

### Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Rating	Com'l.	Ind.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to Vss	-0.5 to +4.6	-0.5 to +4.6	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	20	20	mA
T <sub>j</sub>	Maximum Junction Temperature <sup>(2)</sup>	125	125	°C

- NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form: T<sub>j</sub> = T<sub>a</sub> + P \* θ<sub>ja</sub> where T<sub>a</sub> is the ambient temperature, P is average operating power and θ<sub>ja</sub> the thermal resistance of the package. For this product, use the following θ<sub>ja</sub> values:

SOJ: 78 °C/W  
TSOP: 112 °C/W

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage	3.0	3.3	3.6	V
$V_{SS}$	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

## DC Electrical Characteristics ( $V_{CC} = 3.3V \pm 0.3V$ )

Symbol	Parameter	Test Conditions	Min.	Typ. (2)	Max.	Unit
$I_{LI}$	Input Leakage Current	$V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}$	-1	—	1	µA
$I_{LO}$	Output Leakage Current	$V_{CC} = MAX., CE1 = V_{IH}, or CE2 = V_{IL}$ $V_{OUT} = V_{SS} to V_{CC}$	-1	—	1	µA
$V_{IL}$	Input Low Voltage		-0.3 <sup>(1)</sup>	—	0.8	V
$V_{IH}$	Input High Voltage		2.2	—	$V_{CC}+0.3$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2mA, V_{CC} = Min.$	—	—	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -1mA, V_{CC} = Min.$	2.4	—	—	V
$I_{CC}$	Operating Power Supply Current	$V_{CC} = MAX$ $CE1 = V_{IL}, CE2 = V_{IH}$ $I_{OUT} = 0mA$ $f = f_{MAX}$	—	—	40	mA
$I_{SB}$	Standby Current (TTL)	$V_{CC} = MAX$ $CE1 = V_{IH} or CE2 = V_{IL}$	—	—	1	mA
$I_{SB1}$	Full Standby Current (CMOS)	$V_{CC} = MAX$ $CE1 \geq V_{CC} - 0.2V, CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V or \leq 0.2V$	—	2 µA	40	µA

NOTE: 1.  $V_{IL}(min) = -3.0V$  for pulse width less than 20 ns. 2.  $V_{CC} = 3.3V, 25C$ .

## Data Retention Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ. (1)	Max.	Unit
$V_{DR}$	$V_{CC}$ for data retention	$\bar{CE}_1 \geq V_{CC} - 0.2V$ $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	1.5	—	—	V
$I_{CC\ DR}$	Data retention current	$\bar{CE}_1 \geq V_{CC} - 0.2V$ $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	—	1	20	$\mu A$
$t_{CDR}$	Chip deselect to data retention time	See waveform	0	—	—	ns
$t_R$	Recovery time	See waveform	$t_{RC}$	—	—	ns

NOTE: 1.  $V_{CC} = 3.3V$ , 25C.

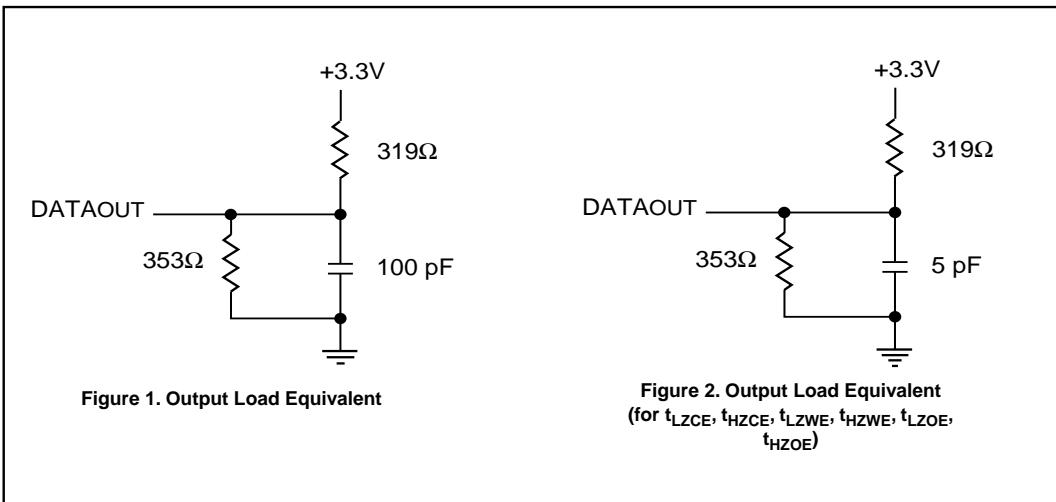
## Capacitance<sup>(1)</sup> ( $T_A = +25^\circ C$ , $f = 1.0$ MHz)

Symbol	Parameter	Max.	Unit
$C_{IN}$	Input Capacitance	6	pF
$C_{OUT}$	Output Capacitance	8	pF

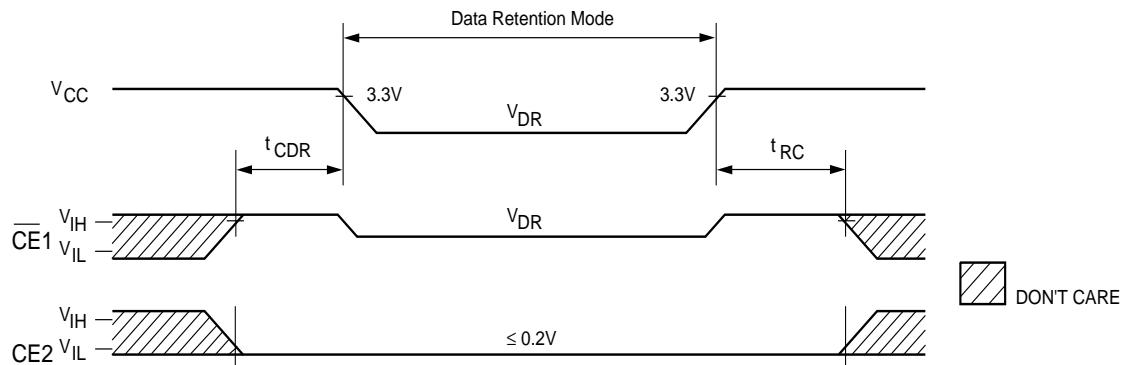
NOTE: 1. This parameter is determined by device characterization but is not production tested.

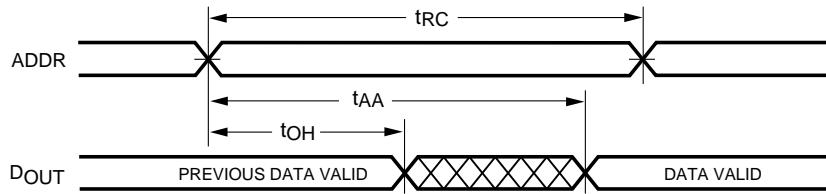
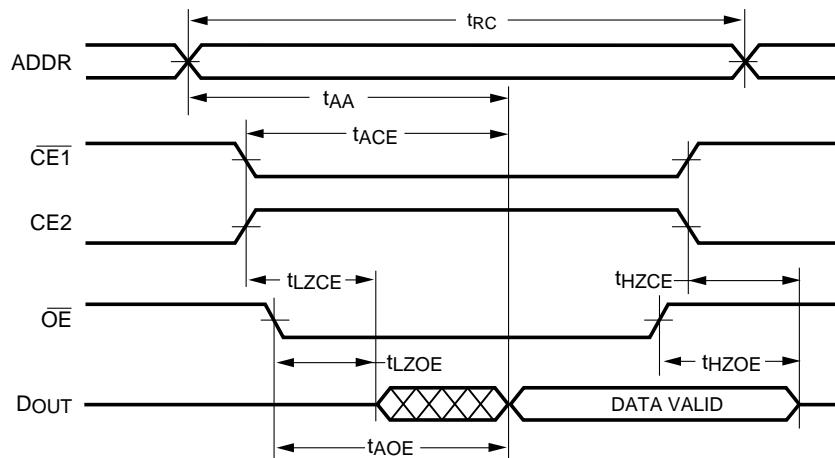
## AC Test Conditions

Input pulse levels	$V_{SS}$ to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

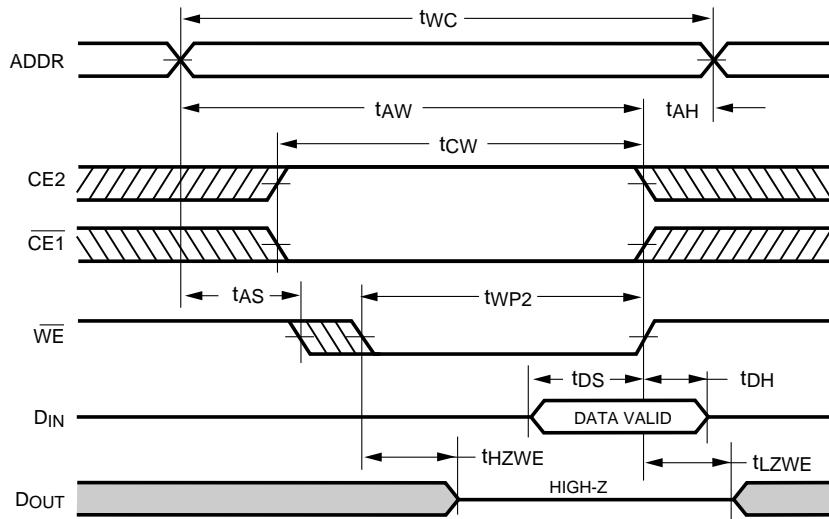
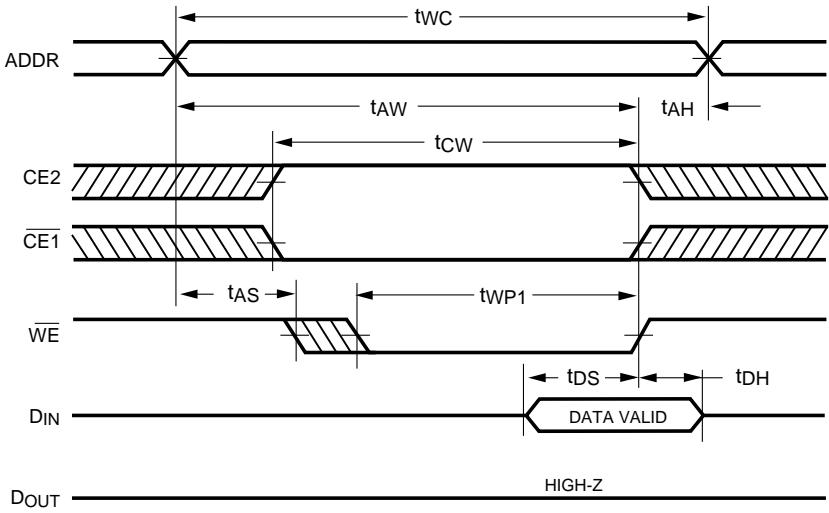


### Low $V_{CC}$ Data Retention Waveform



**Read Cycle No. 1<sup>(1)</sup>****Read Cycle No. 2<sup>(2)</sup>****AC Electrical Characteristics**

Description		-70		-85		-100		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	$t_{RC}$	70		85		100		ns
Address access time	$t_{AA}$		70		85		100	ns
Chip enable access time	$t_{ACE}$		70		85		100	ns
Output hold from address change	$t_{OH}$	10		10		10		ns
Chip enable to output in low Z <sup>(3,4,5)</sup>	$t_{LZCE}$	10		10		10		ns
Chip disable to output in high Z <sup>(3,4,5)</sup>	$t_{HZCE}$		35		35		35	ns
Output enable access time	$t_{AOE}$		50		50		50	ns
Output enable to output in low Z <sup>(4,5)</sup>	$t_{LZOE}$	10		10		10		ns
Output disable to output in high Z <sup>(4,5)</sup>	$t_{HZOE}$		30		30		30	ns

**Write Cycle No. 1 (Write Enable Controlled)****Write Cycle No. 2 (Chip Enable Controlled)**

## AC Electrical Characteristics

Description		-70		-85		-100		
WRITE Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Units
WRITE cycle time	$t_{WC}$	70		85		100		ns
Chip enable to end of write	$t_{CW}$	70		85		100		ns
Address valid to end of write	$t_{AW}$	70		85		100		ns
Address setup time	$t_{AS}$	0		0		0		ns
Address hold from end of write	$t_{AH}$	0		0		0		ns
Write pulse width	$t_{WP}$	50		50		50		ns
Data setup time	$t_{DS}$	40		40		40		ns
Data hold time	$t_{DH}$	0		0		0		ns
Write disable to output in low Z <sup>(4,5)</sup>	$t_{LZWE}$	5		5		5		ns
Write enable to output in high Z <sup>(4,5)</sup>	$t_{HZWE}$		30		30		30	ns

NOTES: (For two previous Electrical Characteristics tables)

1. The device is continuously selected. Chip Enable is held in its active state.
2. The address is valid prior to or coincident with the latest occurring Chip Enable.
3. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ .
4. This parameter is sampled.
5. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured  $\pm 500$  mV from steady state voltage.

## Ordering Information

