QUICKSWITCH® PRODUCTS HIGH-SPEED CMOS SYNCHROSWITCH™ QUAD 2:1 MUX/DEMUX

IDTQS3S257

FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- Bidirectional signal flow
- Flow-through pinout
- Zero propagation delay, zero ground bounce
- 4 banks of 2:1 Mux/Demux
- Port select synchronous to the clock
- Clock enable and Asynchronous switch enable
- "Bus-hold" terminators on the Demux side
- Undershoot clamp diodes on all switch and control pins
- Asynchronous SEL option
- Break-before-make feature
- Available in QSOP Package
- Bus-hold eliminates floating bus lines and reduces static power consumption

APPLICATIONS:

- Video, audio, graphics switching, muxing
- Bus funneling
- Voltage translation

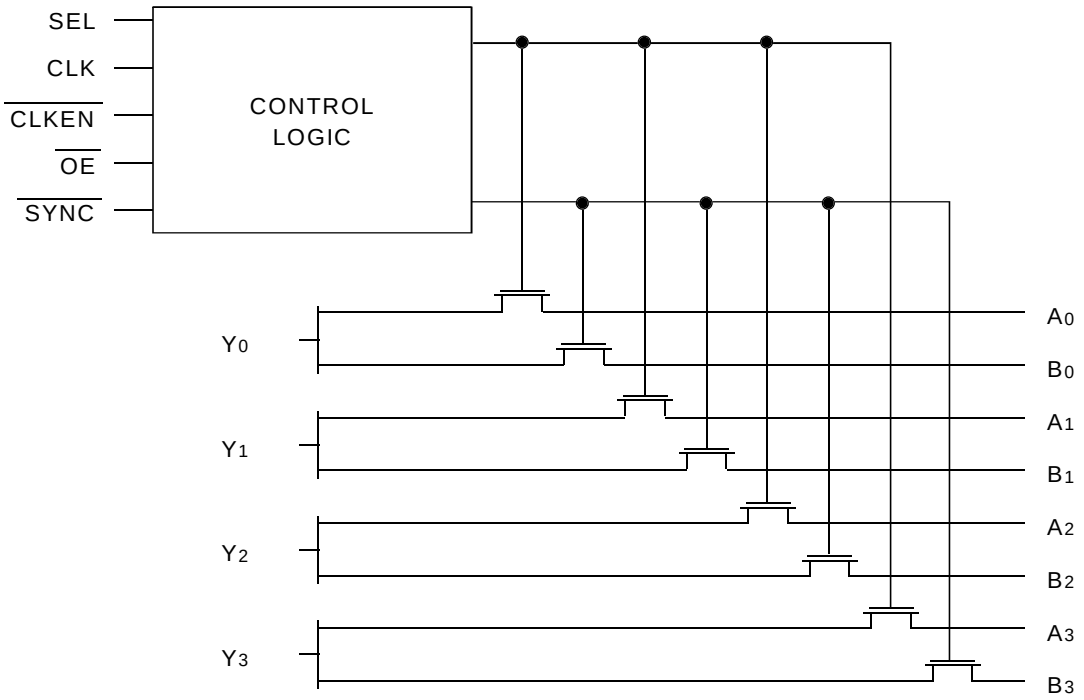
DESCRIPTION:

The QS3S257 is a high-speed CMOS Quad 2:1 multiplexer/demultiplexer. Port selection and connection, controlled by SEL signals, can be either asynchronous or synchronous. In the synchronous mode, the A or B port to Y port connection is updated on the rising edge of the input clock CLK. Once the port-to-port connection is made, data flow can be bi-directional with a typical 250ps propagation delay through the switch. Clock Enable, overriding Asynchronous Enable, and Asynchronous Select controls provide additional design flexibility. Synchronous controls eases timing constraints in many high speed data mux/demux applications, such as bank interleaving. The QS3S257 can also be used in 5V to 3.3V translation.

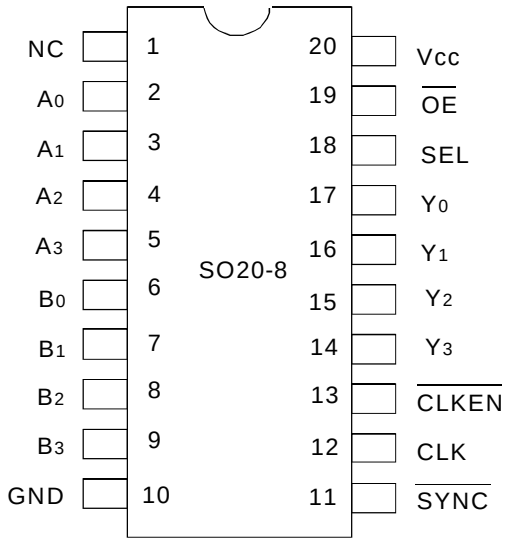
QuickSwitch Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

The QS3S257 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Supply Voltage to Ground	– 0.5 to +7	V
V_{TERM}(3)	DC Switch Voltage V_S	– 0.5 to +7	V
V_{TERM}(3)	DC Input Voltage V_{IN}	– 0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation (T_A = 85°C)	.82	W
T_{STG}	Storage Temperature	– 65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, V_{IN} = 0V, V_{OUT} = 0V)

Pins		Typ.	Max. (1)	Unit
Control Inputs		4	5	pF
Quickswitch Channels	Demux	5	7	pF
(Switch OFF)	Mux	7	9	pF

NOTE:
1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

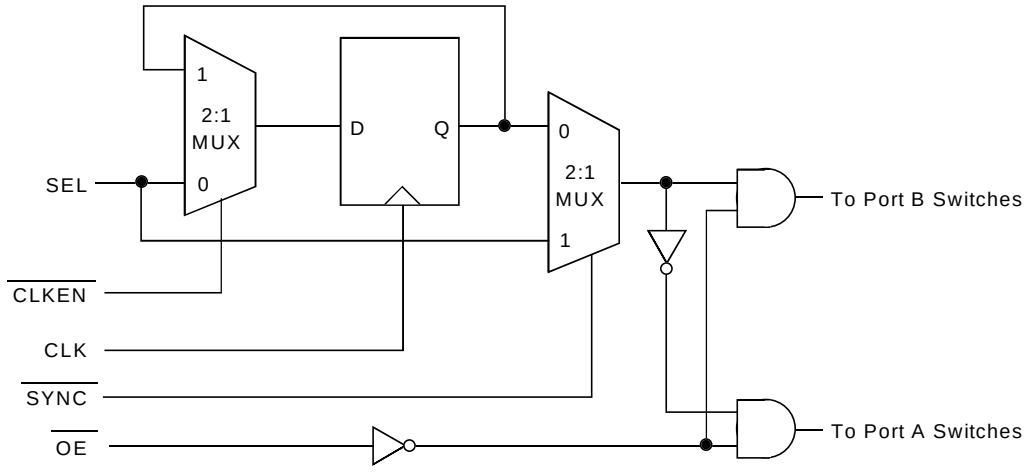
Pin Names	I/O	Description
A_0 - A_3	I/O	Demux Port A
B_0 - B_3	I/O	Demux Port B
Y_0 - Y_3	I/O	Mux Port Y
SEL	I	Select Input
CLK	I	Clock
$\overline{CLKEN}$	I	Clock Enable
$\overline{OE}$	I	Output Enable
$\overline{SYNC}$	I	Synchronous Enable

FUNCTION TABLE[1]

Control Inputs					Port Status				Function
$\overline{SYNC}$	$\overline{OE}$	CLKn	$\overline{CLKEN}$	SEL	Y_0	Y_1	Y_2	Y_3	
L	L	↑	L	L	A_0	A_1	A_2	A_3	Select Port A
L	L	↑	L	H	B_0	B_1	B_2	B_3	Select Port B
L	H	↑	L	X	No change in Mux connection				Hold Previous Data [2] (Switch OFF)
L	L	↑	H	X	No change in Mux connection				Hold Previous Mux connection [3] (Switch ON)
L	H	↑	H	X	No change in Mux connection				Hold Previous Data [4] (Switch OFF)
H	L	X	X	L	A_0	A_1	A_2	A_3	Select Port A
H	L	X	X	H	B_0	B_1	B_2	B_3	Select Port B
H	H	X	X	X	No change in Mux connection				Hold Previous Data [2] (Switch OFF)

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
2. Mux switches are turned off and the terminators (last value latches) hold the previous data state. The port connection can be changed by the SEL input.
3. The contents of the "Mux select register" are unchanged and the previous Mux connection is unchanged. The output (Mux port) data state will depend on the present data state of the input (Demux port).
4. The contents of the "Mux select register" are unchanged and the last value latches hold the previous data state.

CONTROL LOGIC



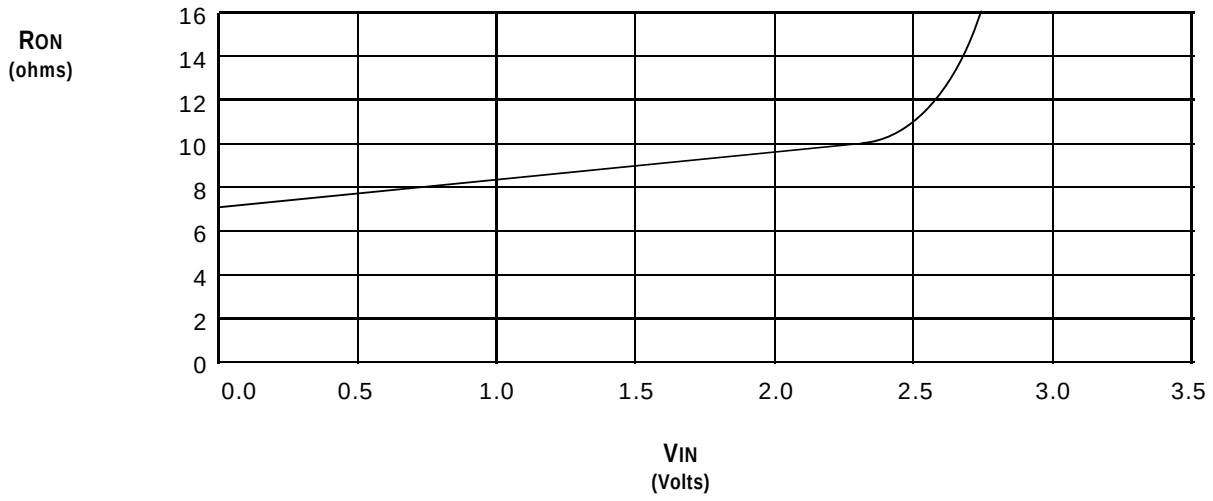
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
I_{IN}	Input Leakage Current (Control Inputs)	$0V \le V_{IN} \le Vcc$	—	±0.1	±1	µA
R_{ON}	Switch ON Resistance	Vcc = Min., V_{IN} = 0V, I_{ON} = 30mA	—	7	9	Ω
R_{ON}	Switch ON Resistance	Vcc = Min., V_{IN} = 2.4V, I_{ON} = 15mA	—	10	13	
V_P	Pass Voltage (2)	V_{IN} = Vcc = 5V, I_{OUT} = -5µA	3.7	4	4.2	V

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Pass Voltage guaranteed but not production tested.

TYPICAL ON RESISTANCE vs V_{IN} AT V_{CC} = 5V



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or Vcc, f = 0	3	µA
ΔI_{CC}	Power Supply Current per Control Input HIGH [2]	V_{CC} = Max., V_{IN} = 3.4V, f = 0	1.5	mA
I_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A/B and Y pins open Control Input Toggling at 50% Duty Cycle	0.25	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input (V_{IN} = 3.4V, control inputs only). A/B and Y pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A/B and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

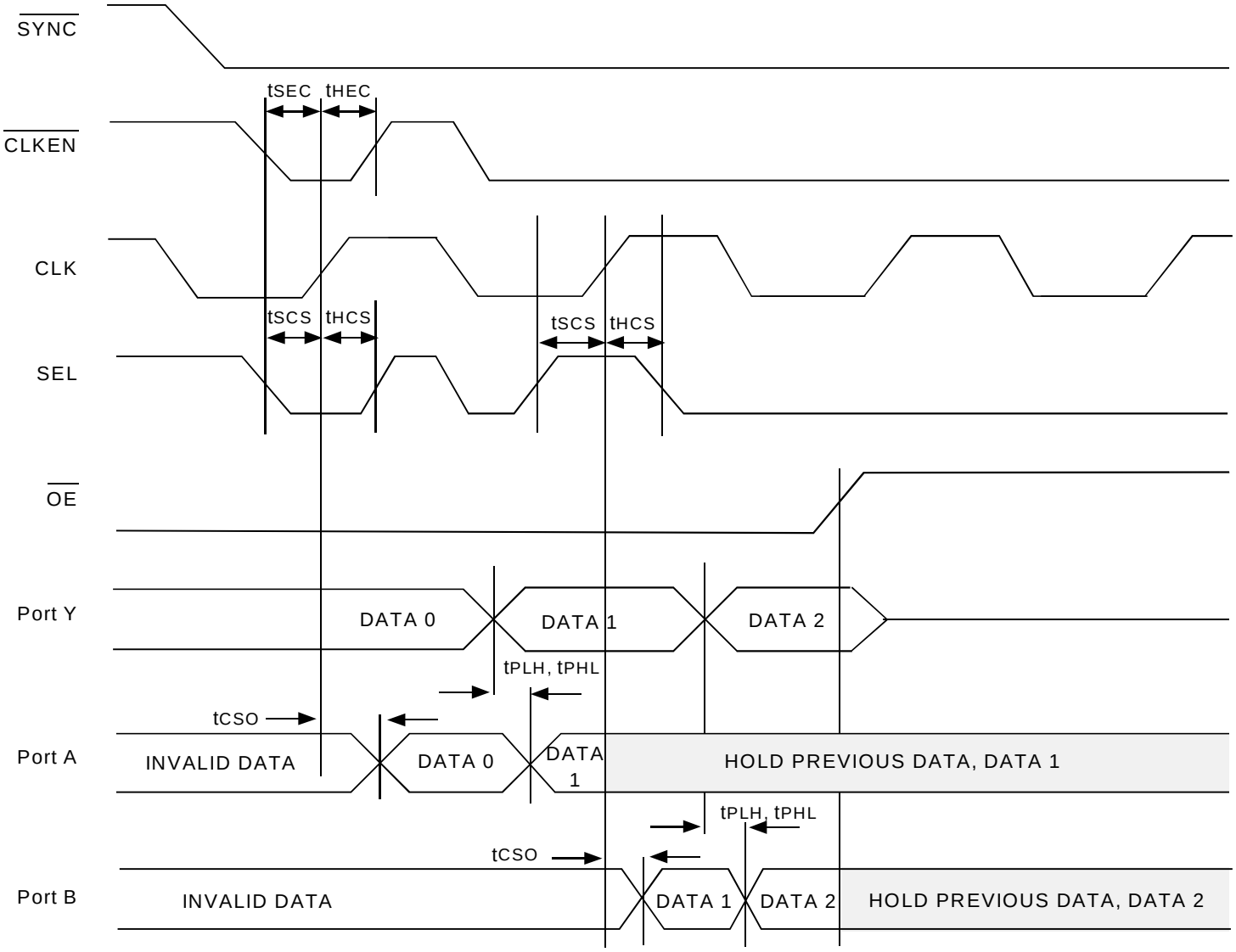
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

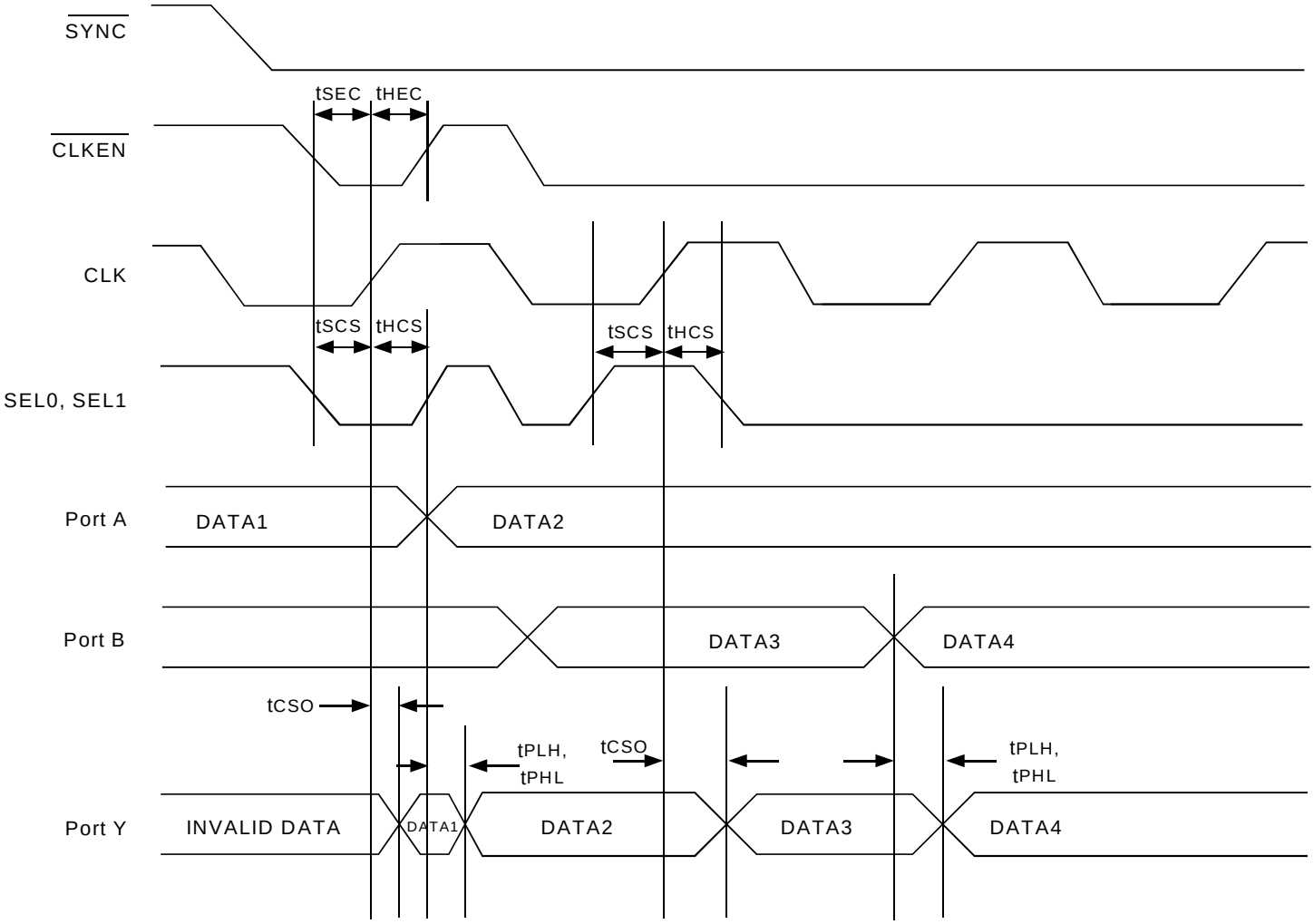
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delays [1,2] A/B to Y, Y to A/B	—	0.25	—	ns
t_{SEC}	Clock Enable to Clock Setup Time	3	—	—	ns
t_{HEC}	Clock Enable to Clock Hold Time	0	—	—	ns
t_{CSO}	Clock to A,B Switch Turn-On Delay [3]	0.5	—	7	ns
t_{ASO}	Asynchronous Select to A,B Switch Turn-On Delay [3]	0.5	—	7	ns
t_W	Clock Pulse Width (High)	3	—	—	ns
t_{SCS}	SEL to Clock Setup Time	3	—	—	ns
t_{HCS}	SEL to Clock Hold Time	0	—	—	ns
t_{PZL} t_{PZH}	Asynchronous Enable to Switch Turn-On Delay [3]	1.5	—	5.2	ns
t_{PLZ} t_{PHZ}	Asynchronous Enable to Switch Turn-Off Delay [1,3]	1.5	—	4.8	ns

NOTES:
1. This parameter is guaranteed but not production tested.
2. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
3. Minimums guaranteed but not production tested.

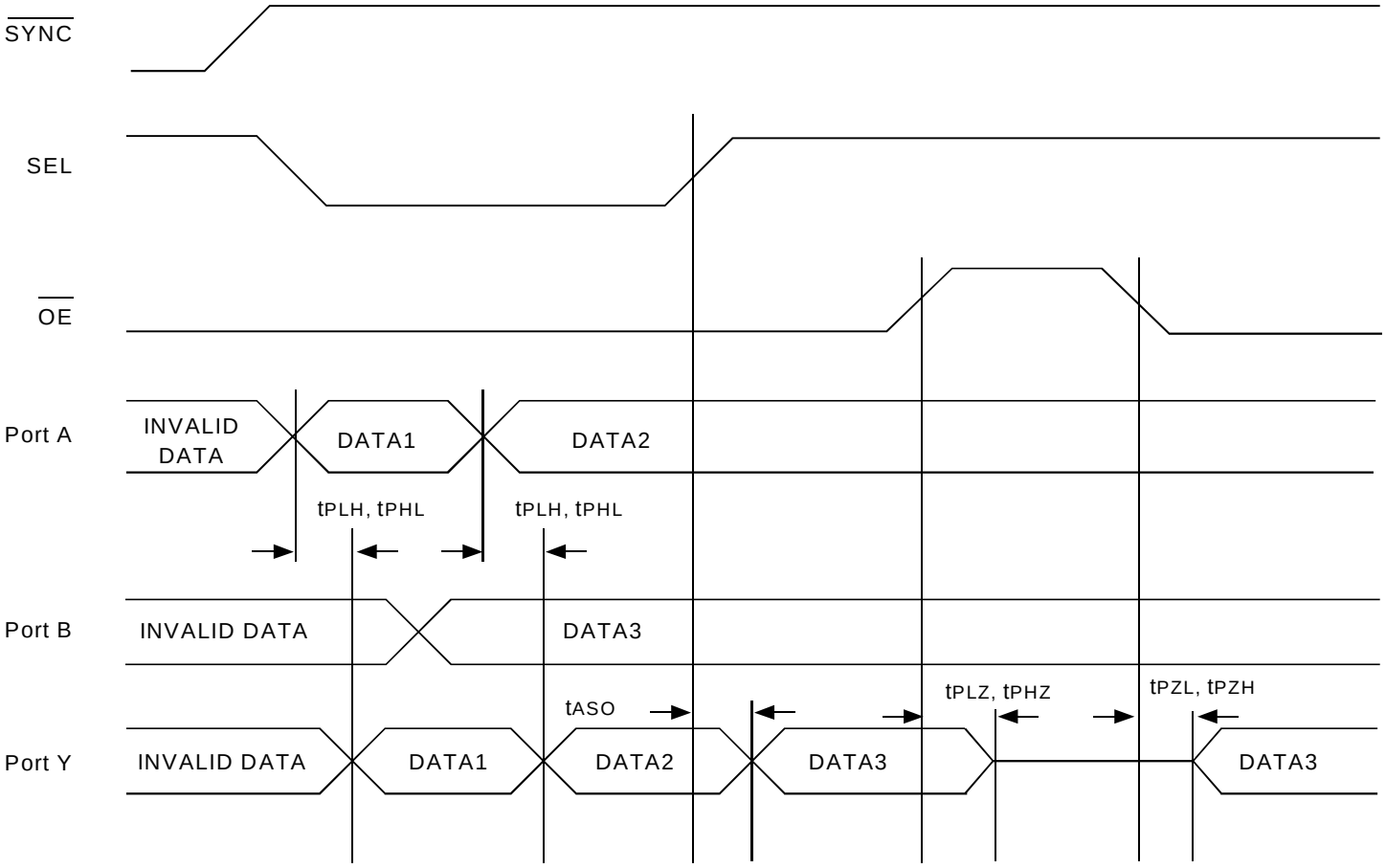
TIMING WAVEFORMS - SYNCHRONOUS MODE, DEMUX FUNCTION



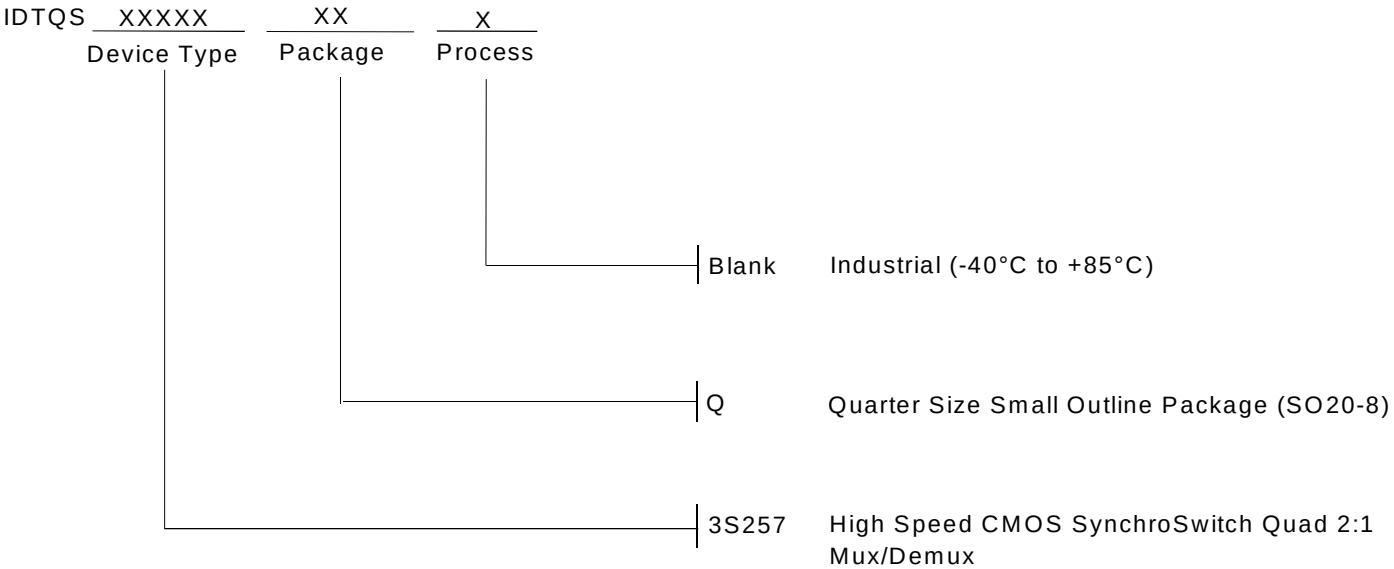
TIMING WAVEFORMS - SYNCHRONOUS MODE, MUX FUNCTION



TIMING WAVEFORMS - ASYNCHRONOUS MODE, MUX FUNCTION



ORDERING INFORMATION



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