QUICKSWITCH® PRODUCTS
HIGH-SPEED CMOS
QUICKSWITCH MULTIWIDTH™
24:6 MUX/DEMUX

IDTQS33X253

FEATURES:

– Enhanced N channel FET with no inherent diode to Vcc
– Bidirectional switches connect inputs to outputs
– 24:6 Mux/Demux switches
– Zero propagation delay, zero ground bounce
– Individual controls for each bank
– Undershoot clamp diodes on all switch and control pins
– TTL-compatible control inputs
– Available in 48-pin QVSOP Package

APPLICATIONS

– Logic replacment
– Video, audio, graphics switching, muxing
– Hot-swapping, hot-docking
– Voltage translation (5V to 3.3V)

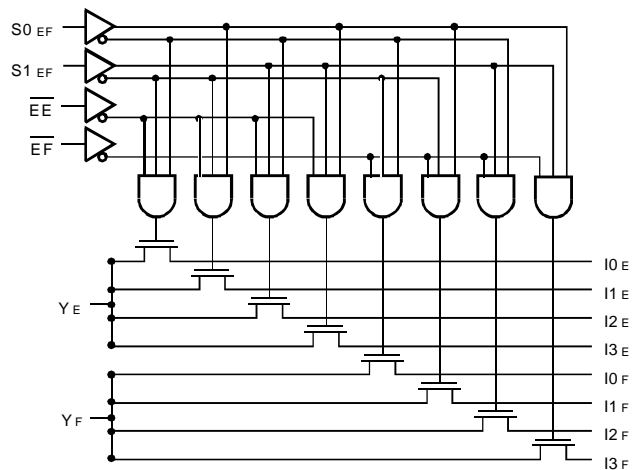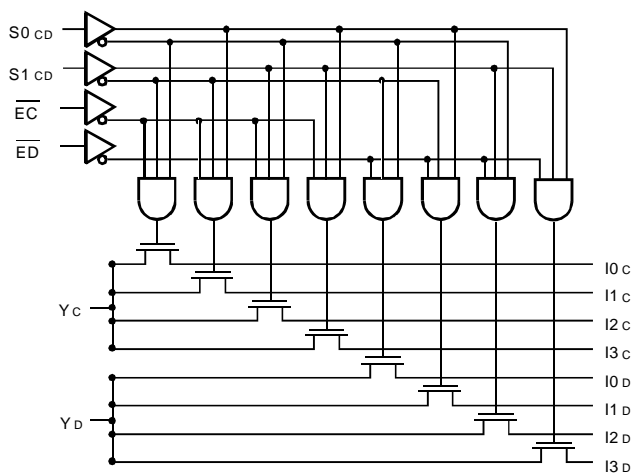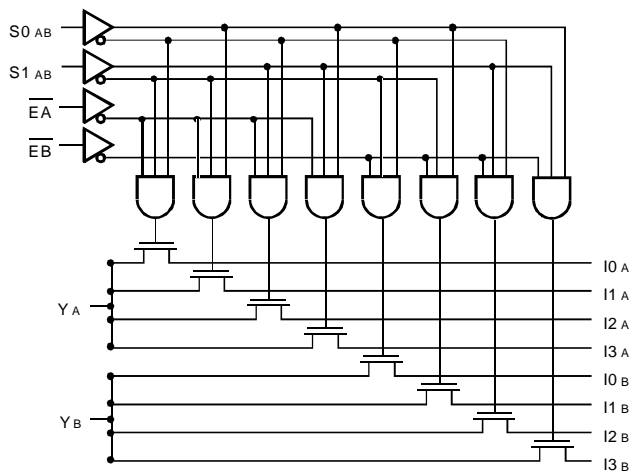## DESCRIPTION:

The QS33X253 is a high-speed CMOS 24:6 (3, dual 4:1) multiplexer/demultiplexer. The QS33X253 is a member of the MultiWidth™ family and is functionally compatible to three of the QuickSwitch version of the 74F253, 74FCT253, and the 74ALS/AS/LS253 Dual 4:1 multiplexers. The low ON resistance of the QS33X253 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. TTL-compatible control circuitry with "Break-before-make" feature avoids bus contention on the demux side. This part is ideal for video switching and four way memory bank interleaving applications.

Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

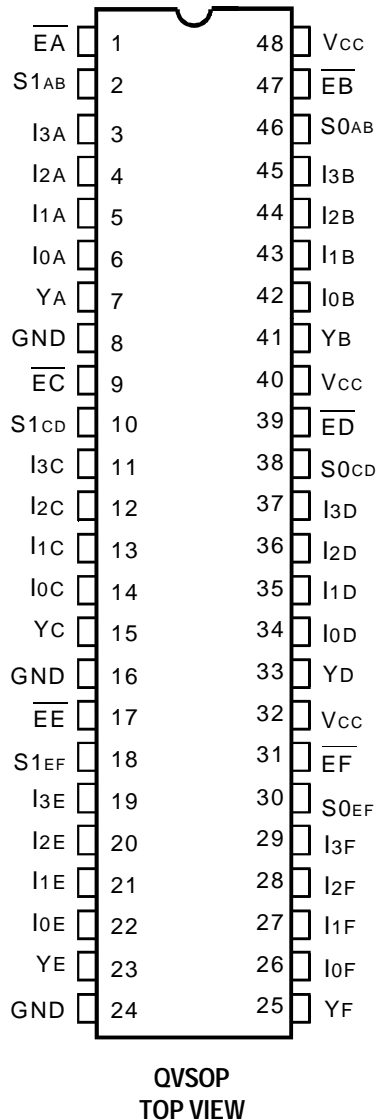The QS33X253 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

DSC-5761/-

PIN CONFIGURATION

$\overline{EA}$	1		48	V_{CC}
$S1_{AB}$	2		47	$\overline{EB}$
$I3_A$	3		46	$S0_{AB}$
$I2_A$	4		45	$I3_B$
$I1_A$	5		44	$I2_B$
$I0_A$	6		43	$I1_B$
Y_A	7		42	$I0_B$
GND	8		41	Y_B
$\overline{EC}$	9		40	V_{CC}
$S1_{CD}$	10		39	$\overline{ED}$
$I3_C$	11		38	$S0_{CD}$
$I2_C$	12		37	$I3_D$
$I1_C$	13		36	$I2_D$
$I0_C$	14		35	$I1_D$
Y_C	15		34	$I0_D$
GND	16		33	Y_D
$\overline{EE}$	17		32	V_{CC}
$S1_{EF}$	18		31	$\overline{EF}$
$I3_E$	19		30	$S0_{EF}$
$I2_E$	20		29	$I3_F$
$I1_E$	21		28	$I2_F$
$I0_E$	22		27	$I1_F$
Y_E	23		26	$I0_F$
GND	24		25	Y_F

QVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	I/O	Description
Ixx	I	Data Inputs
S0xx, S1xx	I	Select Inputs
$\overline{Ex}$	I	Enable Inputs
Yx	O	Data Outputs

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Description	Max.	Unit
V_{TERM}[2]	Supply Voltage to Ground	– 0.5 to +7	V
V_{TERM}[3]	DC Switch Voltage V_S	– 0.5 to +7	V
V_{TERM}[3]	DC Input Voltage V_{IN}	– 0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation (T_A = 85°C)	.5	W
T_{STG}	Storage Temperature	– 65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

CAPACITANCE

$(T_A = +25^O C, f = 1.0MHz, V_{IN} = 0V, V_{OUT} = 0V)$

Pins		Typ.	Max. [1]	Unit
Control Inputs		4	5	pF
Quickswitch Channels	Demux	5	7	pF
(Switch OFF)	Mux	14	16	pF

NOTE:
1. This parameter is guaranteed at characterization but not tested.

FUNCTION TABLE[1, 2]

Enable		Select		Outputs		
$\overline{EA}$	$\overline{EB}$	$S1_{AB}$	$S0_{AB}$	Y_A	Y_B	Function
H	X	X	X	Hi-Z	X	Disable A
X	H	X	X	X	Hi-Z	Disable B
L	L	L	L	$I0_A$	$I0_B$	$S1 - 0 = 0$
L	L	L	H	$I1_A$	$I1_B$	$S1 - 0 = 1$
L	L	H	L	$I2_A$	$I2_B$	$S1 - 0 = 2$
L	L	H	H	$I3_A$	$I3_B$	$S1 - 0 = 3$

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. This table represents the function for block "AB".
   The "CD" block nomenclature substitutes "A" for "C" and "B" for "D".
   The "EF" block nomenclature substitutes "A" for "E" and "B" for "F".

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I_{IN}	Input Leakage Current (Control Inputs)	$0V \leq V_{IN} \leq V_{CC}$	—	—	±1	μA
I_{OZ}	Off-State Current (Hi-Z)	$0V \leq V_{OUT} \leq V_{CC}$	—	—	±1	μA
R_{ON}	Switch ON Resistance	V_{CC} = Min., V_{IN} = 0V, I_{ON} = 30mA	—	7	10	Ω
R_{ON}	Switch ON Resistance	V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15mA	—	10	15	Ω
V_P	Pass Voltage [2]	V_{IN} = V_{CC} = 5V, I_{OUT} = -5μA	3.7	4	4.2	V

NOTES:

1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Pass voltage is guaranteed but not production tested.

TYPICAL ON RESISTANCE vs V_{IN} AT V_{CC} = 5V
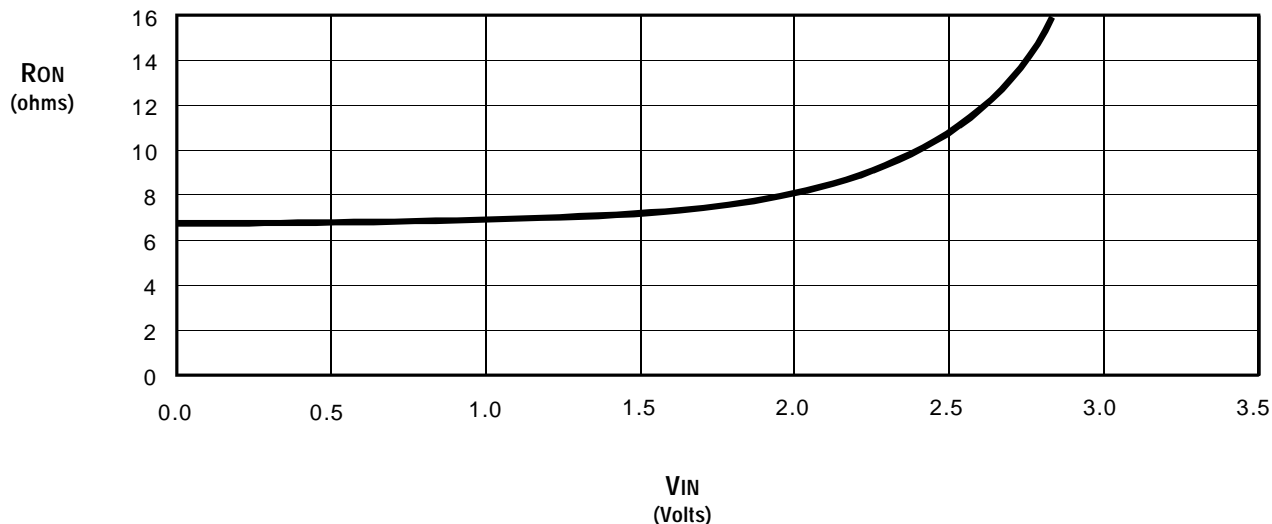
POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	9	µA
ΔI_{CC}	Power Supply Current per Control Input HIGH[2]	V_{CC} = Max., V_{IN} = 3.4V , f = 0	1.5	mA
I_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., I and Y pins open Control Input Toggling at 50% Duty Cycle	0.25	mA/MHz

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). I and Y pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE
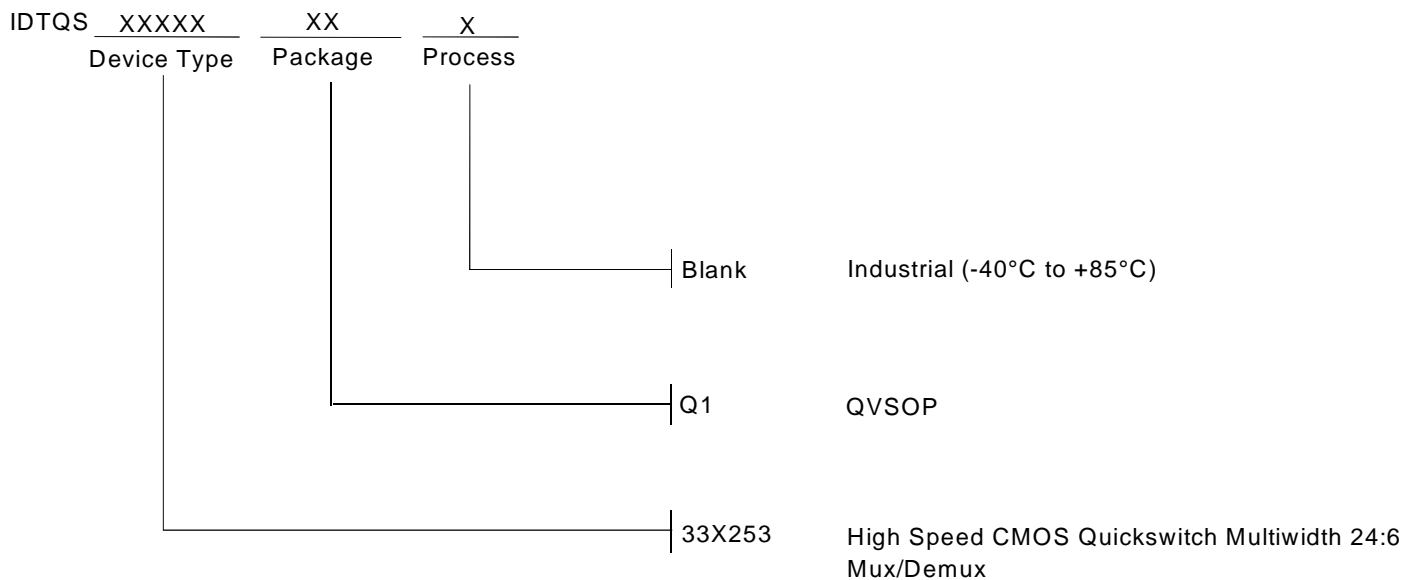
T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Parameter	Min. [1]	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay [2, 3] In to Y	—	—	0.25	ns
t_{PZL} t_{PZH}	Switch Turn-On Delay Sn to Y	0.5	—	6.6	ns
t_{PZL} t_{PZH}	Switch Turn-Off Delay $\overline{En}$ to Y	0.5	—	6	ns
t_{PLZ} t_{PHZ}	Switch Turn-Off Delay [2] $\overline{En}$ to Y, Sn to Y	0.5	—	6	ns

NOTES:

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed but not tested
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

ORDERING INFORMATION

```
IDTQS   XXXXX        XX        X
        Device Type  Package   Process
```

Blank — Industrial (-40°C to +85°C)

Q1 — QVSOP

33X253 — High Speed CMOS Quickswitch Multiwidth 24:6 Mux/Demux