QUICKSWITCH® PRODUCTS 3.3V HIGH SPEED DOUBLE-WIDTH BUS SWITCH

IDTQS32XV245

FEATURES:

- 5Ω bi-directional switches connect inputs to outputs
- Pin Compatibility with QS3245
- 250ps Propagation Delay
- Undershoot Clamp Diodes on all Switch and Control Inputs
- LVTTL-Compatible Control Inputs
- Available in 40-pin QVSOP Package

APPLICATIONS:

- 3.3V to 2.5V Voltage translation
- 2.5V to 1.8V Voltage translation
- PCI Bus isolation hot swap

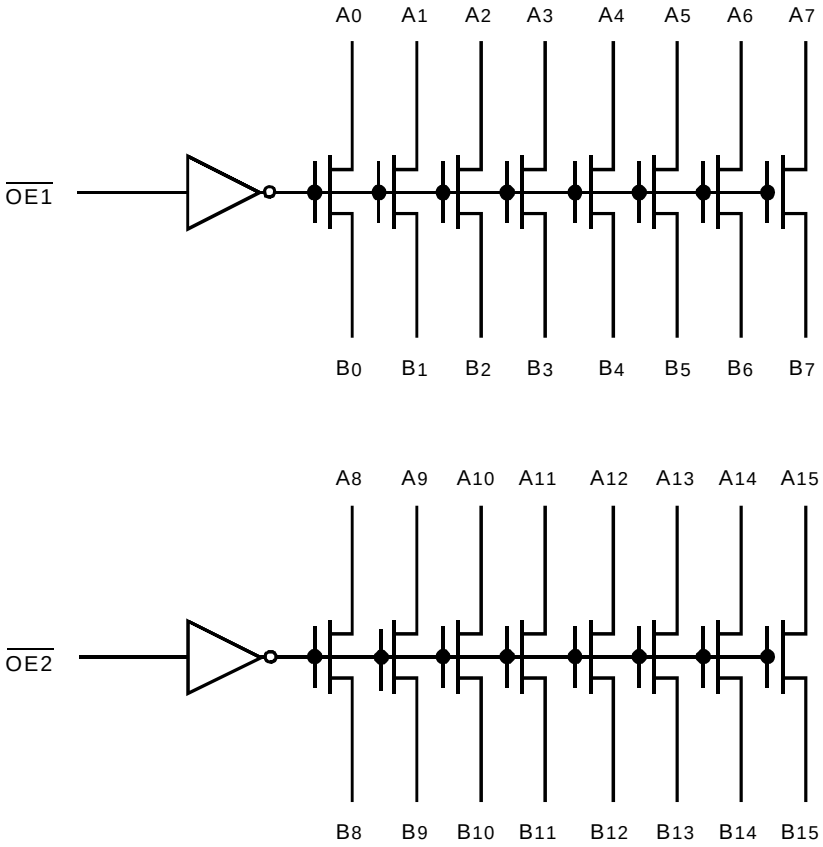
DESCRIPTION:

The QS32XV245 is a 16-bit high speed bus switch controlled by LVTTL-compatible active low enable signal. When closed, the switches exhibit near zero propagation delay without generating additional ground bounce or switching noise.

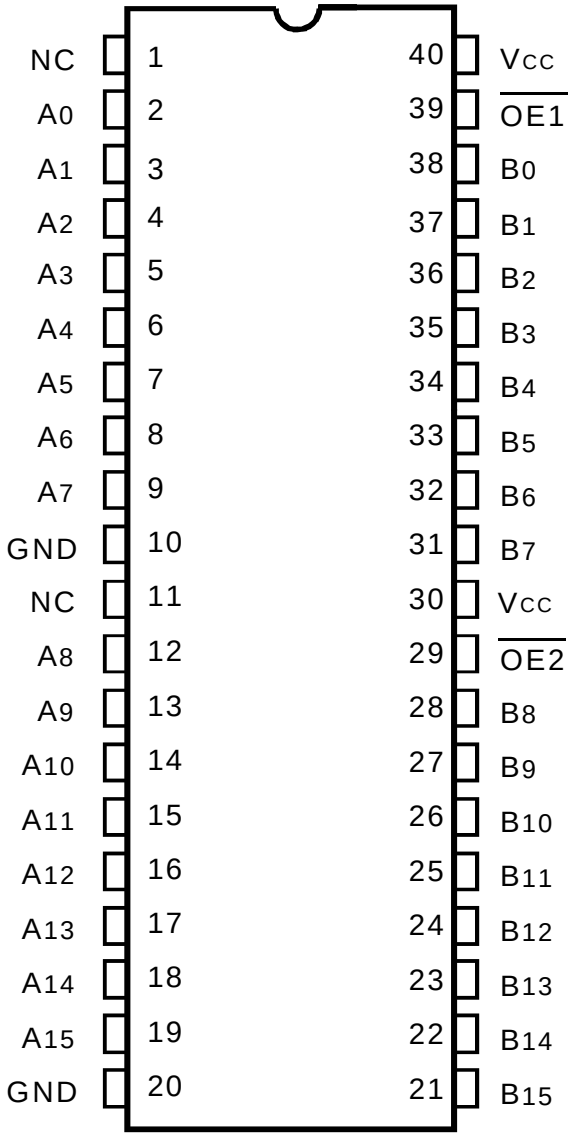
The QS32XV245 is specially designed for direct interface between 3.3V and 2.5V devices without any external components. When operating from a 3.3V supply, the logic high level at the switch output is clamped to 2.5V when the switch input signal exceeds 2.5V. This device can be used for switching 2.5V buses without signal attenuation. The ON resistance at 3.3V V_{CC} is less than 5Ω typical, providing near zero propagation delay through the switch. Absence of DC path from switch I/O pins to V_{CC} or ground makes QS32XV245 an ideal device for hot swapping applications.

The QS32XV245 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Supply Voltage to Ground	– 0.5 to 4.6	V
V_{TERM}(3)	DC Switch Voltage V_S	– 0.5 to 4.6	V
V_{TERM}(3)	DC Input Voltage V_{IN}	– 0.5 to 4.6	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	– 3	V
V_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation	0.6	W
T_{STG}	Storage Temperature	-65 to 150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Control Inputs		4	6	pF
CI/O	Quickswitch Channels	Switch OFF	5	7	pF

NOTE:
1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable
An	Data I/Os
Bn	Data I/Os

FUNCTION TABLE (1)

$\overline{OE_1}$	$\overline{OE_2}$	A_0 - A_7	A_8 - A_{15}	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	B_0 - B_7	Hi-Z	Connect
H	L	Hi-Z	B_8 - B_{15}	Connect
L	L	B_0 - B_7	B_8 - B_{15}	Connect

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   Z = High-Impedence

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = – 40°C To +85°C

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V_{IL}	Input LOW Voltage Level	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I_{IN}	Input Leakage Current (Control Inputs)	$0V \le V_{IN} \le V_{CC}$	—	—	±1	µA
I_{OZ}	Off-State Current (Hi-Z)	$0V \le V_{OUT} \le V_{CC}$, Switches OFF	—	±0.001	±1	µA
R_{ON}	Switch ON Resistance	V_{CC} = Min., V_{IN} = 0V, I_{ON} = 8mA	—	5	7	Ω
		V_{CC} = Min., V_{IN} = 1.7V, I_{ON} = 8mA	—	15	20	Ω
		V_{CC} = 2.3V, V_{IN} = 0V, I_{ON} = 8mA	—	7	—	Ω
		V_{CC} = 2.3V, V_{IN} = 1.3V, I_{ON} = 8mA	—	25	—	Ω
V_P	Pass Voltage	V_{IN} = V_{CC} = 3.3V, I_{OUT} = -5µA	2.5	2.7	2.9	V
		V_{IN} = V_{CC} = 2.5V, I_{OUT} = -5µA	—	1.8	—	V

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)	Min.	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	—	6	µA
ΔI_{CC}	Power Supply Current(2) per Input HIGH	V_{CC} = Max., V_{IN} = 3V or V_{CC}, f = 0 per Control Input	—	50	µA
I_{CCD}	Dynamic Power Supply Current per MHz (3)	V_{CC} = Max., A and B Pins Open, Control Input Toggling @ 50% Duty Cycle	—	0.15	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input (V_{IN} = 3.4V). A and B pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Min. (1)	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay (1,2) An to/from Bn	—	—	0.25	ns
t_{PZL} t_{PZH}	Switch Turn-On Delay $\overline{OE}n$ to An/Bn	0.5	—	6.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-Off Delay (1) $\overline{OE}n$ to An/Bn	0.5	—	4	ns

NOTES:
1. This parameter is guaranteed but not production tested.
2. The time constant for the switch alone is of the order of 0.25ns at C_L = 30pF. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

TYPICAL ON RESISTANCE vs V_{IN} AT V_{CC} = 3.3V

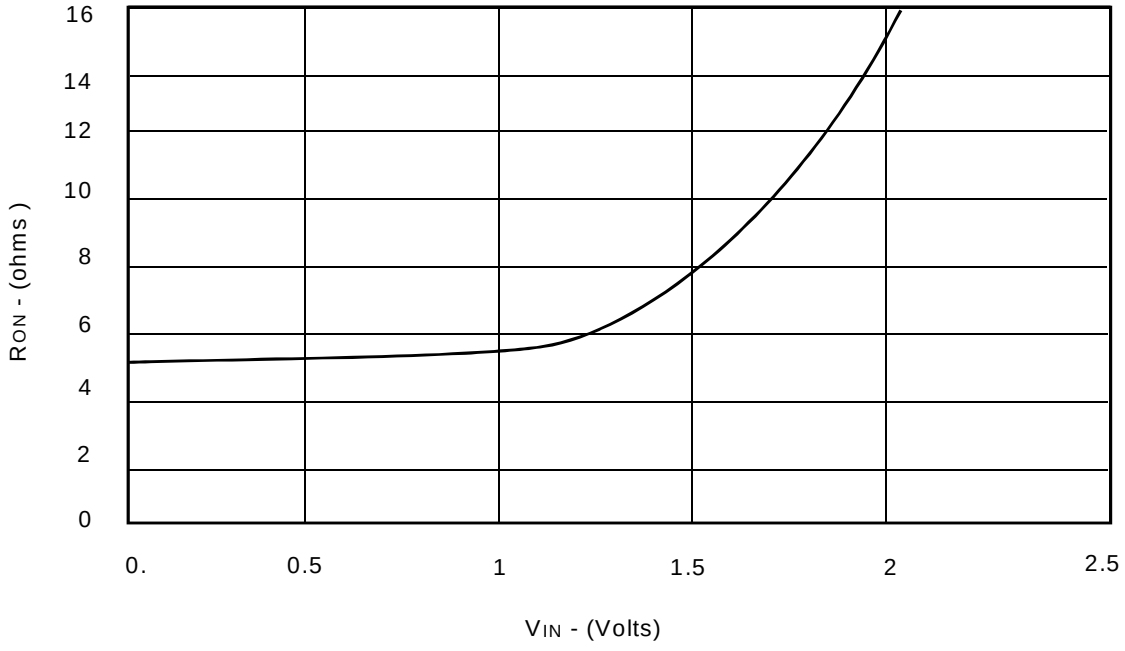
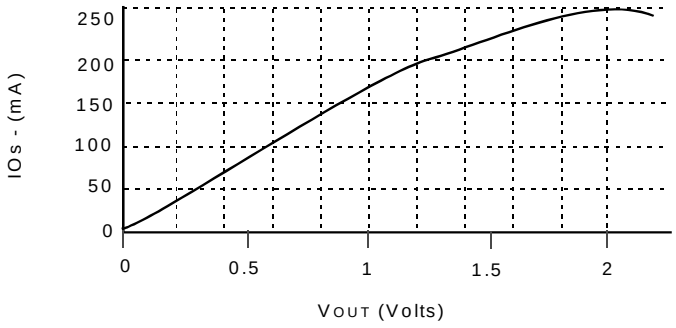


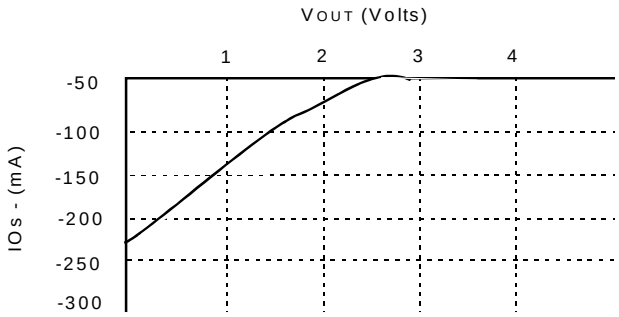
Figure. 1

OUTPUT VI CHARACTERISTICS



Outputs Low Characteristic

Figure. 2



Outputs High Characteristic

Figure. 3

PASS VOLTAGE vs Vcc

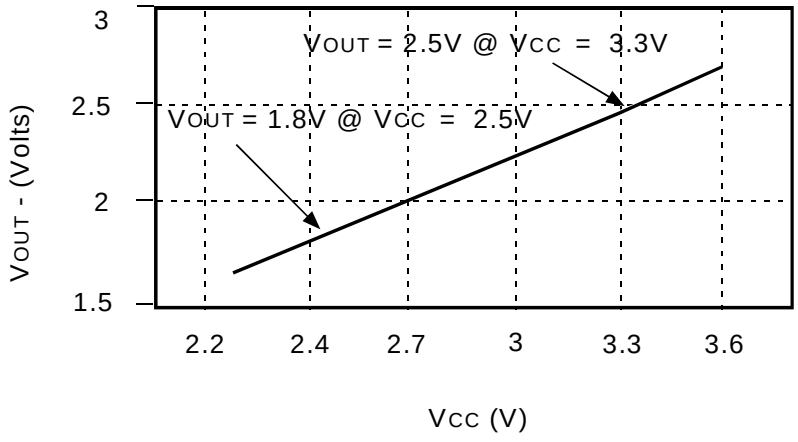


Figure. 4

3.3V TO 2.5V VOLTAGE TRANSLATION

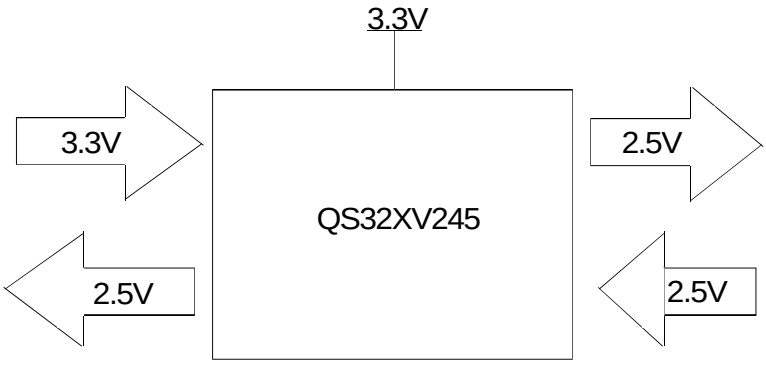


Figure. 5

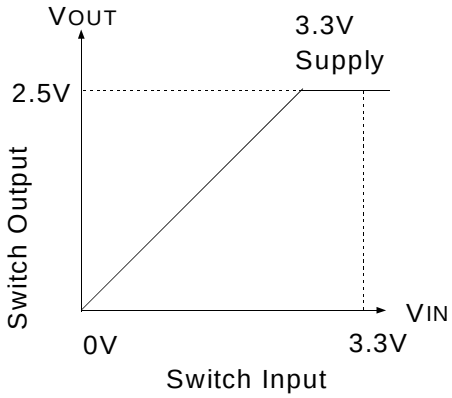


Figure. 6

2.5V TO 1.8V VOLTAGE TRANSLATION

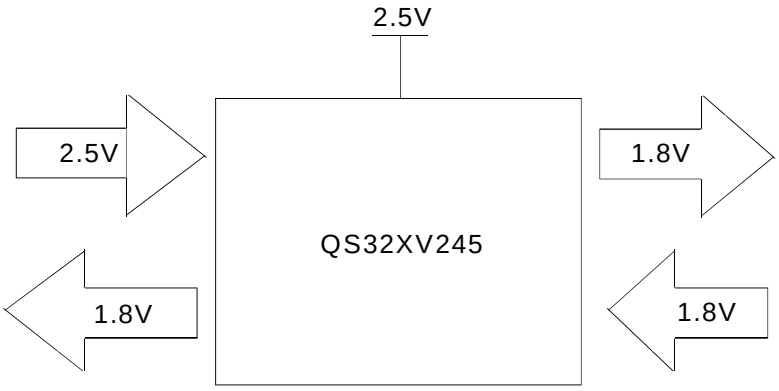


Figure. 7

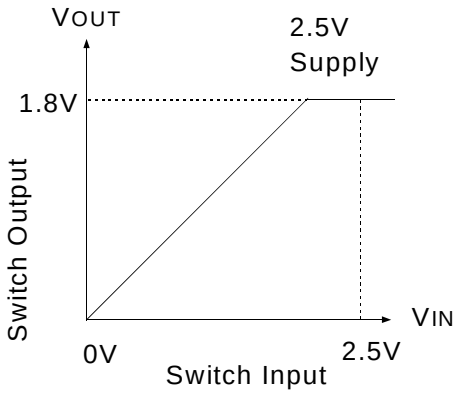
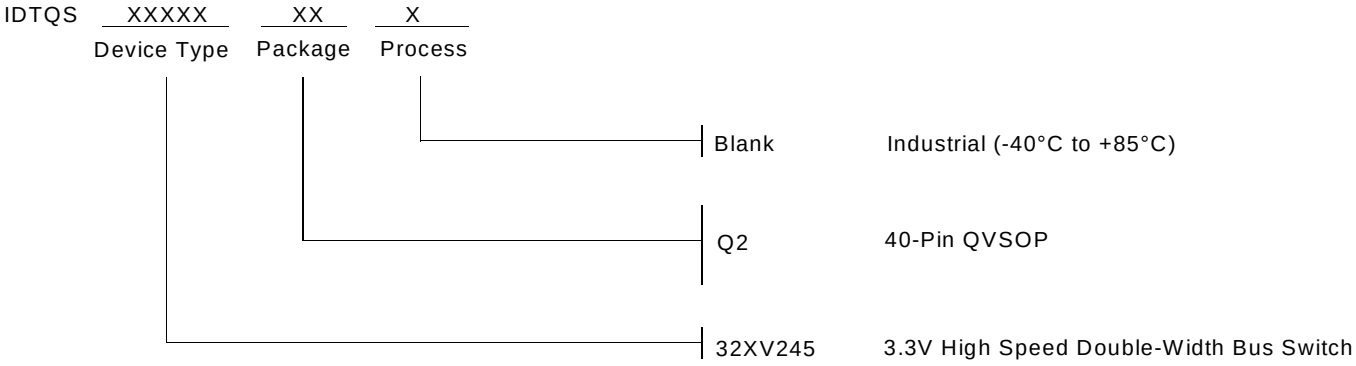


Figure. 8

ORDERING INFORMATION



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