

## QUICKSWITCH<sup>®</sup> PRODUCTS HIGH-SPEED CMOS 24-BIT BUS SWITCH

## FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero ground bounce
- TTL-compatible input and output levels
- Undershoot clamp diodes on all switch and control pins

**FUNCTIONAL BLOCK DIAGRAM** 

Available in 56-pin SSOP and TSSOP Packages

## **APPLICATIONS**

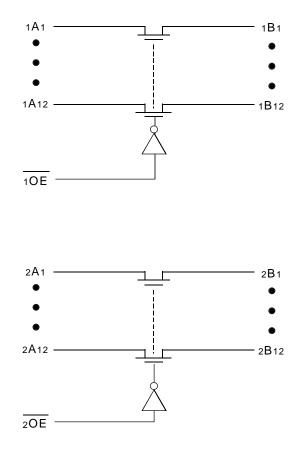
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Logic replacement (data processing)
- Power conservation
- Capacitance reduction and isolation
- Bus isolation
- Clock gating

# DESCRIPTION:

The QS316211 provides a set of 24 high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS316211 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The device operates as a 24-bit bus switch. When  $\overline{10E}$  is low, 1An is connected to 1Bn. When  $\overline{20E}$  is low, 2An is connected to 2Bn.

The QS316211 is ideal for switching wide digital buses, 5V to 3.3V translation, and for hot plug buffering.

The QS316211 is characterized for operation at -40°C to +85°C.



### INDUSTRIAL TEMPERATURE RANGE

#### **NOVEMBER 1999**

#### INDUSTRIALTEMPERATURERANGE

#### **PIN CONFIGURATION**

I		-,		1
NC 🗌	1	$\bigcirc$	56	10E
1A1	2		55	2OE
1A2	3		54	1B1
1A3	4		53	1B2
1A4	5		52	1B3
1A5	6		51	1B4
1A6	7		50	1B5
GND	8		49	GND
1A7	9		48	1B6
1A8	10		47	1B7
1A9	11		46	1B8
1A10	12		45	1B9
1A11	13		44	1B10
1A12	14	SO56-1	43	1B11
2A1	15	SO56-2	42	1B12
2A2	16		41	2B1
Vcc 🗌	17		40	2B2
2A3	18		39	2B3
GND	19		38	GND
2A4	20		37	2B4
2A5	21		36	2B5
2A6	22		35	2B6
2A7	23		34	2B7
2A8	24		33	2B8
2A9	25		32	2B9
2A10	26		31	2B10
2A11	27		30	2B11
2A12	28		29	2B12
l				J

SSOP/ TSSOP TOP VIEW

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Supply Voltage to Ground	– 0.5 to +7	V
VTERM <sup>(3)</sup>	DC Switch Voltage Vs	– 0.5 to +7	V
VTERM <sup>(3)</sup>	DC Input Voltage VIN	– 0.5 to +7	V
VAC	AC Input Voltage (pulse width ≤20ns)	-3	V
Ιουτ	DC Output Current	120	mA
Рмах	Maximum Power Dissipation (TA = 85°C)	.93	W
Tstg	Storage Temperature	- 65 to +150	°C

#### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. Vcc Terminals.
- 3. All terminals except Vcc.

### CAPACITANCE

 $(TA = +25^{\circ}C, f = 1.0MHz, VIN = 0V, VOUT = 0V)$ 

Pins	Тур.	Max. <sup>(1)</sup>	Unit
Control Inputs	4.5	6	pF
Quickswitch Channels (Switch OFF)	5.5	7	pF

NOTE:

1. This parameter is guaranteed but not production tested.

### **PIN DESCRIPTION**

Pin Names	I/O	Description
xA1 - xA12	I/O	Bus A
xB1 - xB12	I/O	Bus B
10E - 20E	I	Data Select

#### **FUNCTION TABLE(1)**

10E	20E	1An	2An	Function
L	L	1Bn	2Bn	1An to 1Bn, 2An to 2Bn
L	Н	1Bn	Z	1An to 1Bn
Н	L	Z	2Bn	2An to 2Bn
Н	Н	Z	Z	Disconnect

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

Z = High-Impedence

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: Industrial: TA = -40°C to +85°C, Vcc =  $5.0V \pm 10\%$ 

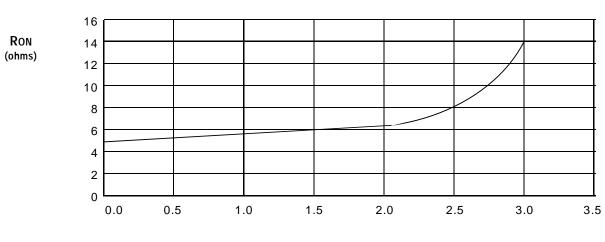
Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2	_	-	V
VIL	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	-	_	0.8	V
lin	Input Leakage Current (Control Inputs)	$0V \le VIN \le Vcc$	-	0.01	±1	μA
loz	Off-State Current (Hi-Z)	$0V \le VOUT \le Vcc$ , Switches OFF	_	0.01	±1	μA
Ron	Switch ON Resistance	Vcc = Min., VIN = 0V, ION = 30mA	-	5	7	Ω
Ron	Switch ON Resistance	Vcc = Min., VIN = 2.4V, ION = 15mA	_	10	12	Ω
Vp	Pass Voltage <sup>(2)</sup>	$VIN = Vcc = 5V$ , $IOUT = -5\mu A$	3.7	4	4.2	V

NOTES:

1. Typical values are at Vcc = 5.0V,  $T_A = 25^{\circ}C$ .

2. Pass voltage is guaranteed but not production tested.

## **TYPICAL ON RESISTANCE vs Vin AT Vcc = 5V**



VIN (Volts)

## **POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Max.	Unit
Icco	Quiescent Power Supply Current	Vcc = Max., VIN = GND or Vcc, f = 0	3	μA
ΔΙcc	Power Supply Current per Control Input HIGH <sup>(2)</sup>	Vcc = Max., V <sub>IN</sub> = 3.4V, f = 0	2.5	mA
Ісср	Dynamic Power Supply Current per MHz <sup>(3)</sup>	Vcc = Max., A and B pins open	0.25	mA/MHz
		Control Input Toggling at 50% Duty Cycle		

#### NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

2. Per TLL driven input (VIN = 3.4V). A and B pins do not contribute to  $\Delta$ Icc.

3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

#### $Ta = -40^{\circ}C \text{ to } +85^{\circ}C, Vcc = 5.0V \pm 10\%$

CLOAD = 50pF, RLOAD =  $500\Omega$  unless otherwise noted.

Symbol	Parameter	Min. <sup>(1)</sup>	Тур.	Max.	Unit
<b>t</b> PLH	Data Propagation Delay <sup>(2,3)</sup>	_	_	0.25 <sup>(3)</sup>	
<b>t</b> PHL	xAn to xBn, xBn to xAn				ns
tPZL	Switch Turn-on Delay	1 Г	_	6.5	
<b>t</b> PZH	nOE to xAn, xBn	1.5			ns
tPLZ	Switch Turn-off Delay <sup>(2)</sup>	1 5	_	6.2	
<b>t</b> PHZ	nOE to xAn, xBn	1.5			ns

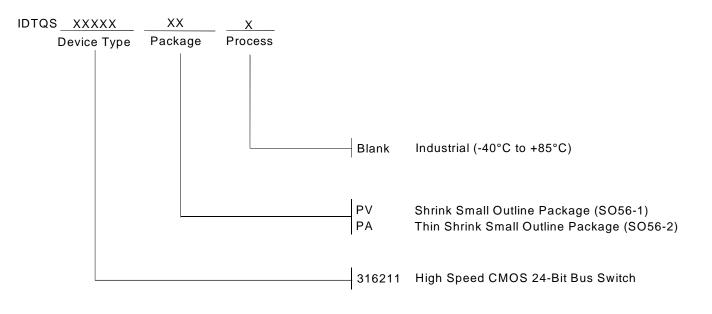
NOTES:

1. Minimums are guaranteed but not production tested.

2. This parameter is guaranteed but not production tested.

3. The time constant for the switch alone is of the order of 0.25ns for CL = 50pF. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

### **ORDERING INFORMATION**





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