



**QUICKSWITCH® PRODUCTS**  
**HIGH-SPEED CMOS**  
**18-BIT BUS EXCHANGE SWITCH**

**IDTQS316209**

**FEATURES:**

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero ground bounce
- TTL-compatible input and output levels
- Undershoot clamp diodes on all switch and control pins
- Available in 48-pin SSOP and TSSOP Packages

**APPLICATIONS**

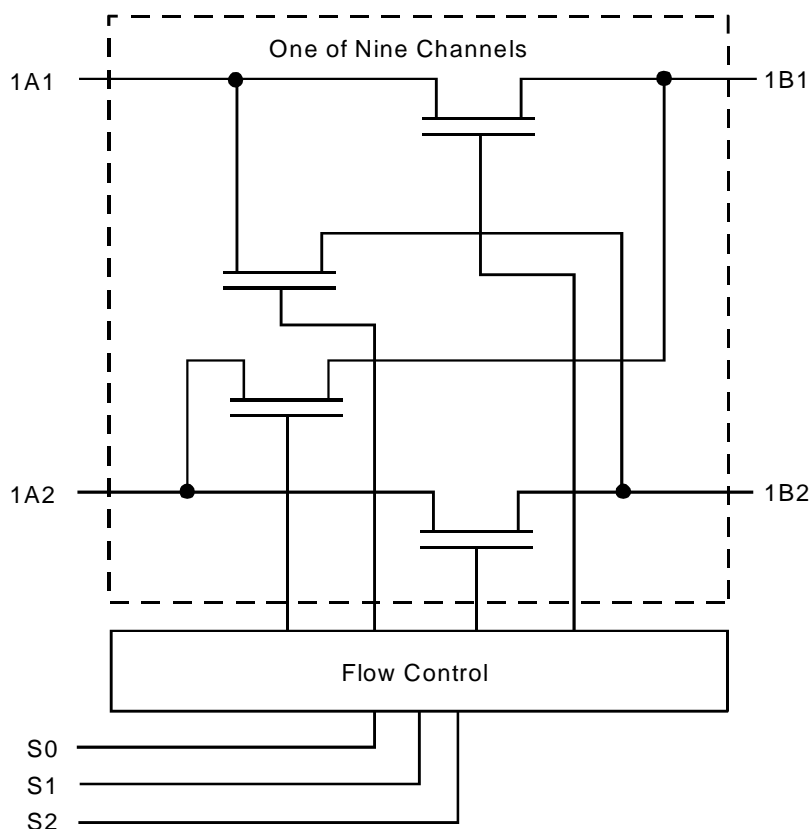
- Resource sharing
- Crossbar switching
- Hot-swapping, hot-docking
- Bus isolation
- Voltage translation (5V to 3.3V)

**DESCRIPTION:**

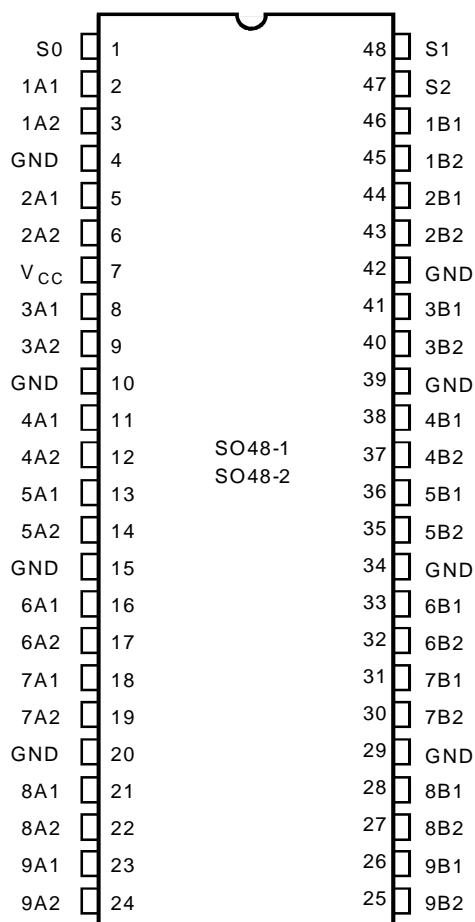
The QS316209 provides a set of 18 high-speed CMOS TTL-compatible bus-exchange switches. The low ON resistance of the QS316209 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. This device operates as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signals through the data-select (S0-S2) terminals.

The QS316209 is characterized for operation at -40°C to +85°C.

**FUNCTIONAL BLOCK DIAGRAM**



## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Symbol	Description	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Supply Voltage to Ground	- 0.5 to +7	V
V <sub>TERM</sub> <sup>(3)</sup>	DC Switch Voltage V <sub>S</sub>	- 0.5 to +7	V
V <sub>TERM</sub> <sup>(3)</sup>	DC Input Voltage V <sub>IN</sub>	- 0.5 to +7	V
V <sub>AC</sub>	AC Input Voltage (pulse width ≤20ns)	-3	V
I <sub>OUT</sub>	DC Output Current	120	mA
P <sub>MAX</sub>	Maximum Power Dissipation (T <sub>A</sub> = 85°C)	0.85	W
T <sub>STG</sub>	Storage Temperature	- 65 to +150	°C

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> Terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE

(T<sub>A</sub> = +25°C, f = 1.0MHz, V<sub>IN</sub> = 0V, V<sub>OUT</sub> = 0V)

Pins	Typ.	Max. <sup>(1)</sup>	Unit
Control Inputs	4	5	pF
Quickswitch Channels (Switch OFF)	7.5	9	pF

### NOTE:

- This parameter is guaranteed but not production tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
1An - 9An	I/O	Bus A
1Bn - 9Bn	I/O	Bus B
S0 - S2	I	Data Select

## FUNCTION TABLE<sup>(1)</sup>

S2	S1	S0	xA1	xA2	Function
L	L	L	Z	Z	Disconnect
L	L	H	xB1	Z	xA1 to xB1
L	H	L	xB2	Z	xA1 to xB2
L	H	H	Z	xB1	xA2 to xB1
H	L	L	Z	xB2	xA2 to xB2
H	L	H	Z	Z	Disconnect
H	H	L	xB1	xB2	xA1 to xB1, xA2 to xB2
H	H	H	xB2	xB1	xA1 to xB2, xA2 to xB1

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High-Impedence

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

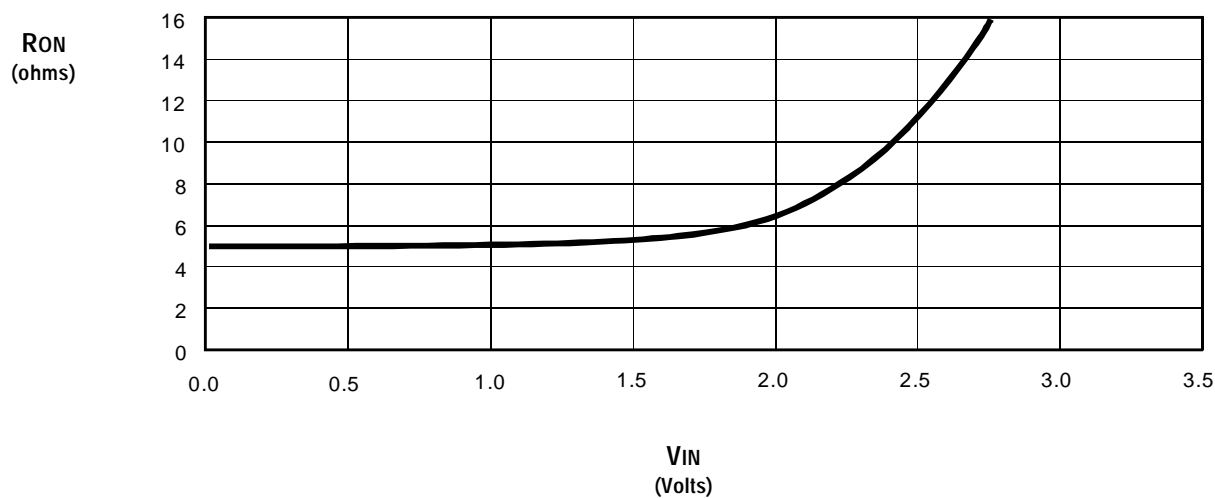
Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2	—	—	V
$V_{IL}$	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$I_{IN}$	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$ , Control Inputs	—	0.01	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	Off-State Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$ , Switches OFF	—	0.01	$\pm 1$	$\mu\text{A}$
$R_{ON}$	Switch ON Resistance	$V_{CC} = \text{Min.}$ , $V_{IN} = 0\text{V}$ , $I_{ON} = 30\text{mA}$	—	5	7	$\Omega$
$R_{ON}$	Switch ON Resistance	$V_{CC} = \text{Min.}$ , $V_{IN} = 2.4\text{V}$ , $I_{ON} = 15\text{mA}$	—	10	14	$\Omega$
$V_P$	Pass Voltage <sup>(2)</sup>	$V_{CC} = 5\text{V}$ , $I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

### NOTES:

- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .
- Pass voltage is guaranteed but not production tested.

## TYPICAL ON RESISTANCE vs $V_{IN}$ AT $V_{CC} = 5\text{V}$



## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Max.	Unit
I <sub>CCQ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub> , f = 0	3	μA
ΔI <sub>CC</sub>	Power Supply Current per Control Input HIGH <sup>(2)</sup>	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V, f = 0	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current per MHz <sup>(3)</sup>	V <sub>CC</sub> = Max., A and B pins open Control Input Toggling at 50% Duty Cycle	0.25	mA/MHz

### NOTES:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- Per TLL driven input (V<sub>IN</sub> = 3.4V, control inputs only). A and B pins do not contribute to ΔI<sub>CC</sub>.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0V ± 10%

C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Parameter	Min. <sup>(1)</sup>	Typ.	Max.	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Data Propagation Delay <sup>(2,4)</sup> xAn to xBn, xBn to xAn	—	—	0.25 <sup>(3)</sup>	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Switch Turn-on Delay Sn to xAn, xBn	1.5	—	6.5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Switch Turn-off Delay <sup>(2)</sup> Sn to xAn, xBn	1.5	—	6.2	ns

### NOTES:

- Minimums are guaranteed but not production tested.
- This parameter is guaranteed but not production tested.
- The time constant for the switch alone is of the order of 0.25ns for C<sub>L</sub> = 50pF.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ORDERING INFORMATION

IDTQS	XXXXX	XX	X		
	Device Type	Package	Process		
			Blank	Industrial (-40°C to +85°C)	
		PV		Shrink Small Outline Package (SO48-1)	
		PA		Thin Shrink Small outline (SO48-2)	
	316209			High Speed CMOS 18-Bit Bus-Exchange Switch	



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