Integrated Device Technology, Inc.

10-BIT, TWO PORT BUS SWITCH

IDT74FST3861
PRODUCT PREVIEW

FEATURES:

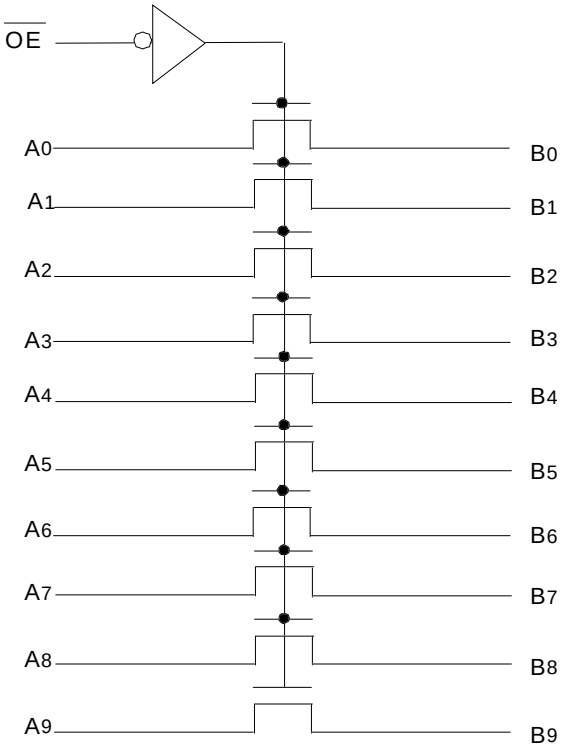
- Bus switches provide zero delay paths
- Extended commercial range of –40°C to +85°C
- Low switch on-resistance:
  FST3xxx –5Ω
  FST32xxx –28Ω
- TTL-compatible input and output levels
- ESD >2000v per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in SOIC, QSOP and TSSOP

DESCRIPTION:

The FST3861 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. They generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to source junction of this FET is adequately forward-biased, the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has not insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

FUNCTIONAL BLOCK DIAGRAM



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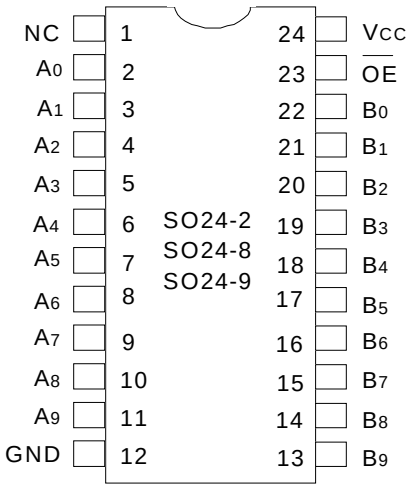
PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
Ax	A Port Bits
Bx	B Port Bits

4246 tbl 01

PIN CONFIGURATION



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SOIC/QSOP/TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Maximum Continuous Channel Current	128	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC}, Control and Switch terminals

FUNCTION TABLE

Inputs $\overline{OE}$	Outputs
L	Connect A to B
H	Disconnect A from B

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CAPACITANCE(1)

Symbol	Parameter	Conditions(2)	Typ.	Unit
C_{IN}	Control Input Capacitance		8	pF
$C_{I/O}$	Switch Input/Output Capacitance	Switch Off	13	pF

4246 tbl 04

NOTES:
1. Capacitance is characterized but not tested.
2. T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Condition Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Control Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Control Input LOW Voltage	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Control Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Control Input LOW Current		V_I = GND	—	—	±1	
I_{OZH}	Current During	V_{CC} = Max., V_O = 0 to 5V		—	—	±1	µA
I_{OZL}	Bus Switch DISCONNECT			—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OFF}	Switch Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±1	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	3	µA

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BUS SWITCH IMPEDANCE OVER OPERATING RANGE

Following Condition Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
R_{ON}	Switch On Resistance(2)	V_{CC} = Min., V_{IN} = 0.0V I_{ON} = 48mA	—	5	7	Ω
		V_{CC} = Min., V_{IN} = 2.4V I_{ON} = 15mA	—	10	15	
I_{OS}	Short Circuit Current, A to B(3)	A(B) = 0V, B(A) = V_{CC}	100	—	—	mA

4246 tbl 06

NOTES:
1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. The voltage drop between the indicated ports divided by the current through the switch.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4,5]	V_{CC} = Max. Outputs Open 1 Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.4	mA/ MHz/ Enable
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open 1 Enable Pin Toggling fi = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	4.0	mA
			V_{IN} = 3.4 V_{IN} = GND	—	3.3	4.8	

4246 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
   T_A = –40°C to +85°C
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND. Switch inputs do not contribute to ΔI_{CC}.
4. This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency. Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. C_{PD} = I_{CCD}/V_{CC}
   C_{PD} = Power Dissipation Capacitance
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (fiN)
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Control Input Frequency
   N = Number of Control Inputs Toggling at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Condition Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Description[1]	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay A to B, B to A[2]	—	—	0.25	ns
t_{PZH} t_{PZL}	Switch CONNECT Delay $\overline{OE}$ to A or B	1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch DISCONNECT Delay $\overline{OE}$ to A or B	1.5	—	5.5	ns
$\lvert Q_{CI} \rvert$	Charge Injection During Switch DISCONNECT $\overline{OE}$ to A or B[3]	—	1.5	—	pC

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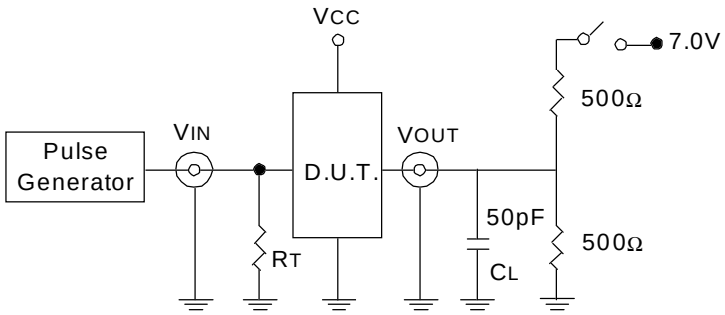
NOTES:
1. See test circuits and waveforms.
2. The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.
3. $\lvert Q_{CI} \rvert$ Is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers.
   $\lvert Q_{DCI} \rvert$ Is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

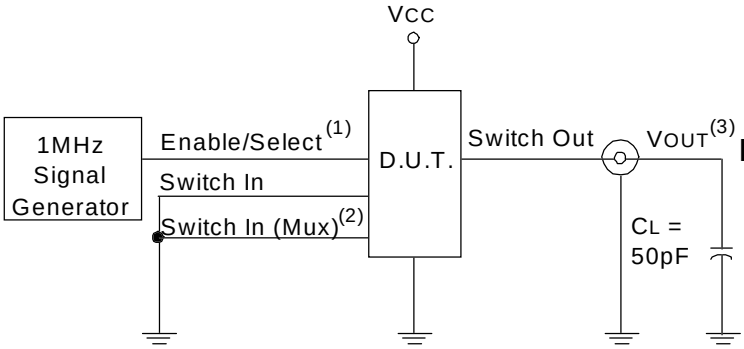
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

4246 lnk 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

CHARGE INJECTION



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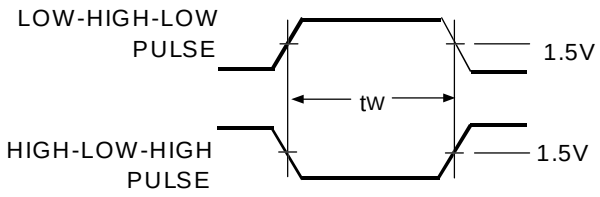
NOTES:

1. Select is used with multiplexers for measuring $|Q_{DCI}|$ during multiplexer select. During all other tests Enable is used.
2. Used with multiplexers to measure $|Q_{DCI}|$ only.
3. Charge Injection = $\Delta V_{OUT} C_L$, with Enable toggling for $|Q_{CI}|$ or Select toggling for $|Q_{DCI}|$. ΔV_{OUT} is the change in V_{OUT} and is measured with a 10MΩ probe.

PULSE WIDTH



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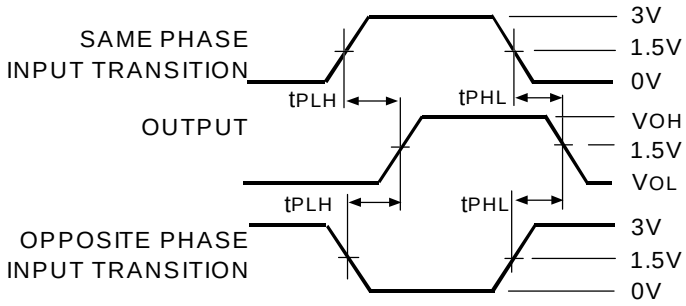
PROPAGATION DELAY



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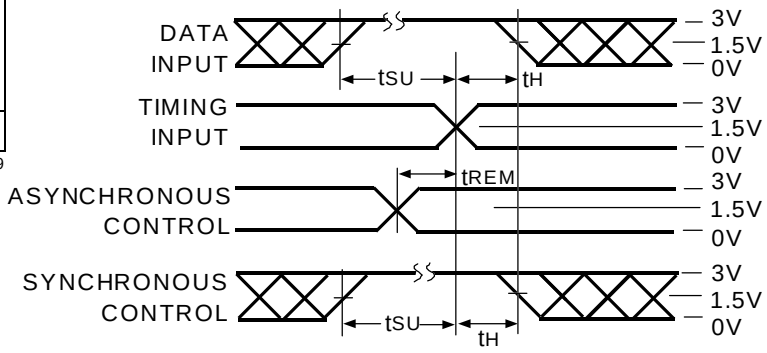
SET-UP, HOLD AND RELEASE TIMES



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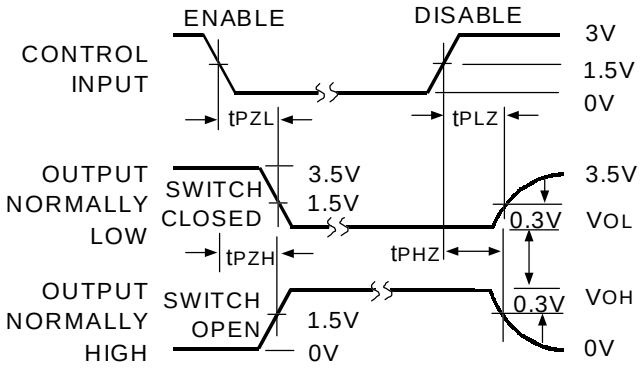
ENABLE AND DISABLE TIMES



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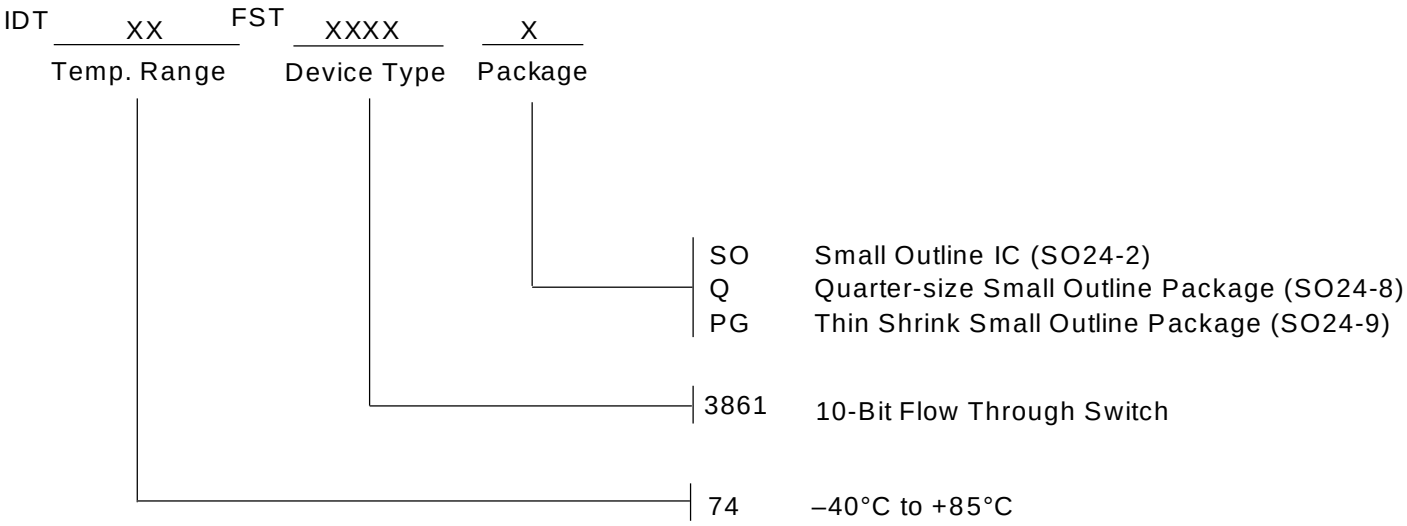
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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