20-BIT BUS EXCHANGE SWITCH

IDT74FST163383

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of –40°C to +85°C
- Low switch on-resistance: 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in SSOP, TSSOP, and TVSOP Packages

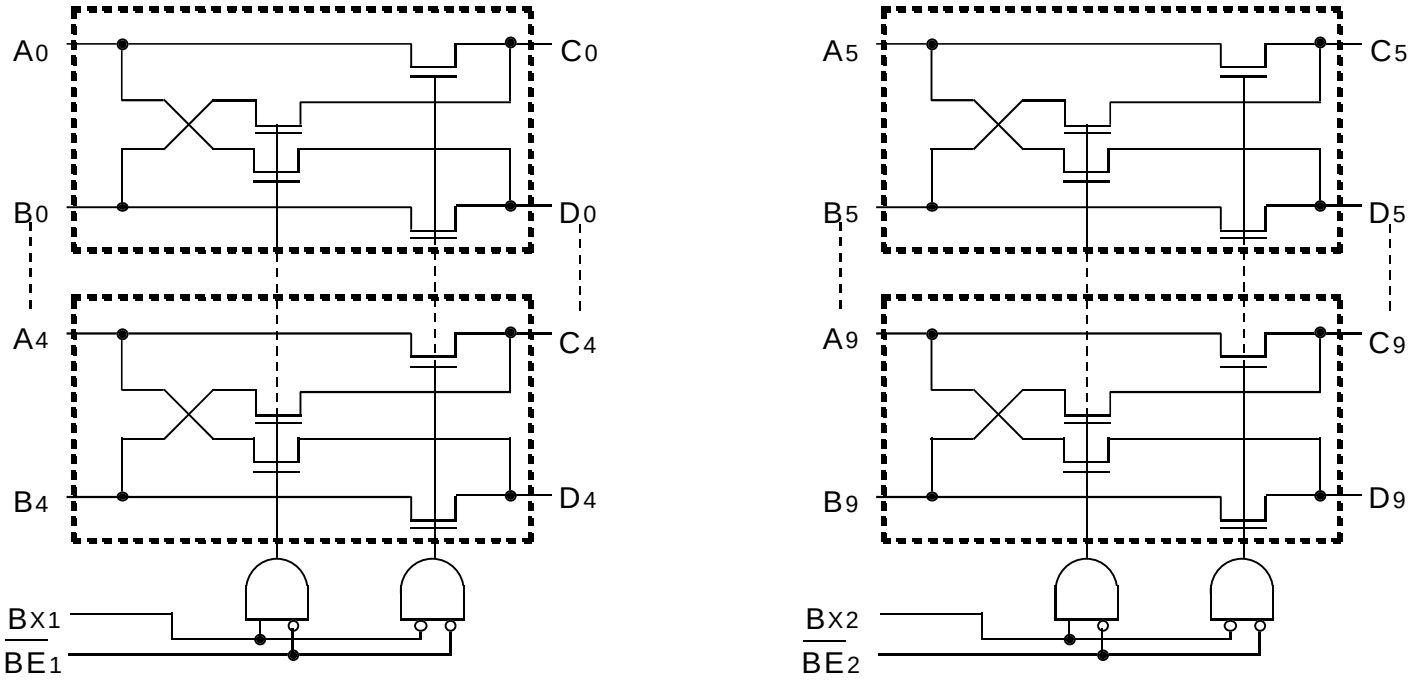
DESCRIPTION:

The FST163383 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has hot insertion capability.

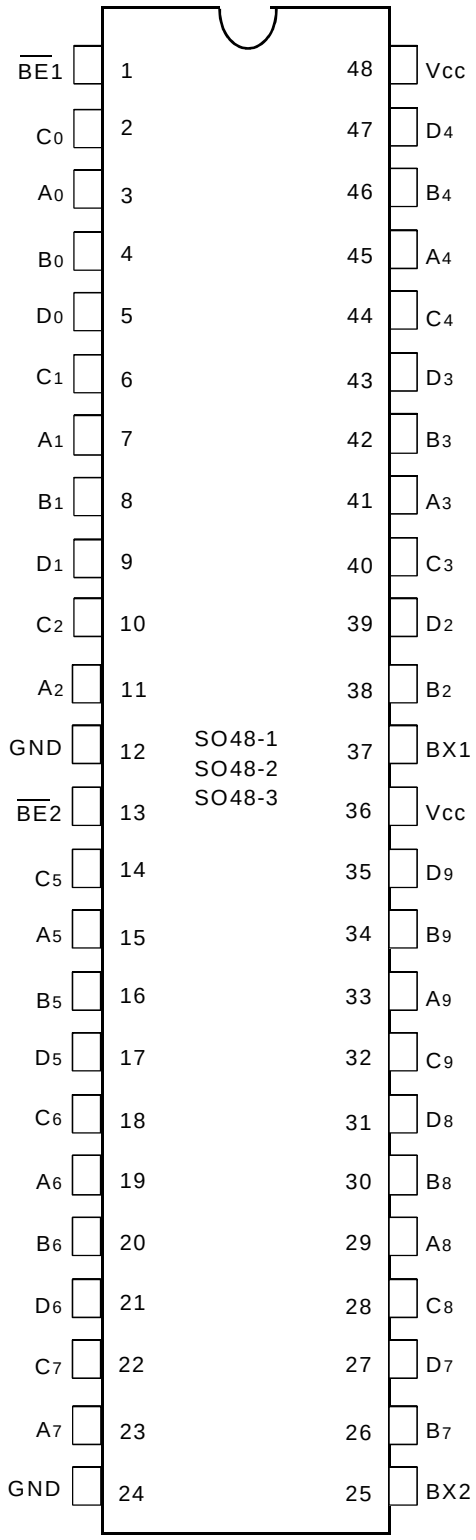
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST163383 provides four 4-bit TTL- compatible ports that supports 2 way bus exchange. The BX pin controls the bus exchange and the BE pin serves as the enable pin.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Maximum Continuous Channel Current	128	mA

FST LINK

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc, Control, and Switch terminals.

CAPACITANCE (1)

Symbol	Parameter	Conditions(2)	Typ.	Unit
C_{IN}	Control Input Capacitance		4	pF
$C_{I/O}$	Switch Input/Output Capacitance	Switch Off		pF

NOTES:
1. Capacitance is characterized but not tested.
2. T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

PIN DESCRIPTION

Pin Names	I/O	Description
A_{0-9}, B_{0-9}	I/O	Buses A, B
C_{0-9}, D_{0-9}	I/O	Buses C, D
$\overline{BE}_{1,2}$	I	Bus Switch Enable (Active LOW)
$BX_{1,2}$	I	Bus Exchange

FUNCTION TABLE (1)

$\overline{BE}_1$	BX_1	A_{0-4}	B_{0-4}	Description
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C_{0-4}	D_{0-4}	Connect
L	H	D_{0-4}	C_{0-4}	Exchange

$\overline{BE}_2$	BX_2	A_{5-9}	B_{5-9}	Description
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C_{5-9}	D_{5-9}	Connect
L	H	D_{5-9}	C_{5-9}	Exchange

NOTE:
1. H = HIGH Voltage level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance[4]	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 30mA		—	5	7	Ω
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15mA		—	10	15	Ω
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	3	µA

FCT LINK

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open Enable Pins Toggling (20 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	6	8	mA
			V_{IN} = 3.4 V_{IN} = GND	—	6.5	9.5	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Control Input Frequency
   N = Number of Control Inputs Toggling at f_i

All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

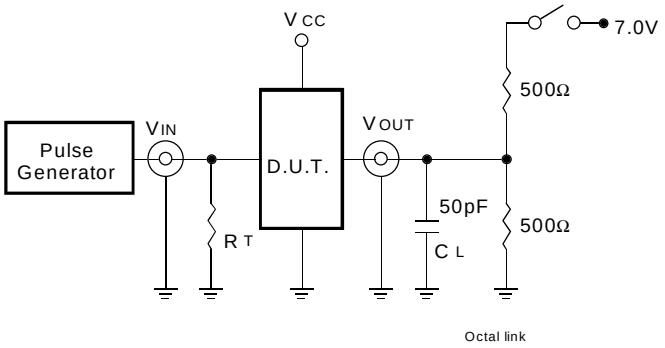
Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Description	Condition[1]	Min.[2]	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay Ai to Ci, Di Bi to Ci, Di[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	ns
t_{BX}	Switch Multiplex Delay BX to Ai, Bi, Ci, Di		1.5	—	6.5	ns
t_{PZH} t_{PZL}	Switch Turn on Delay BE to Ai, Bi, Ci, Di		1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay BE to Ai, Bi[3]		1.5	—	5.5	ns
$\|Q_{CI}\|$	Charge Injection, Typical[5,7]		—	1.5	—	pC
$\|Q_{CDI}\|$	Charge Injection, Typical[6,7]		—	0.5	—	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Measured at switch turn off through bus multiplexer, (e.g.- A to C = >A to D), load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.
7. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

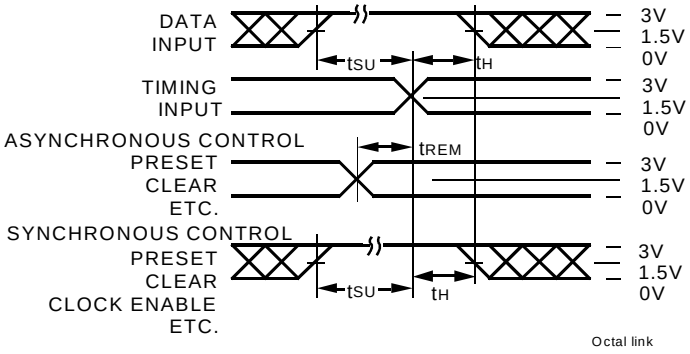
FCT LINK

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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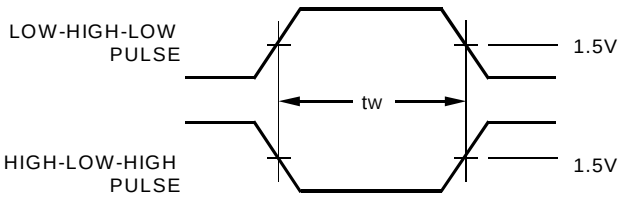
PULSE WIDTH



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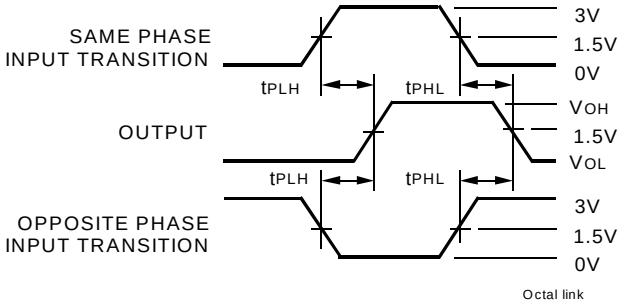
PROPAGATION DELAY



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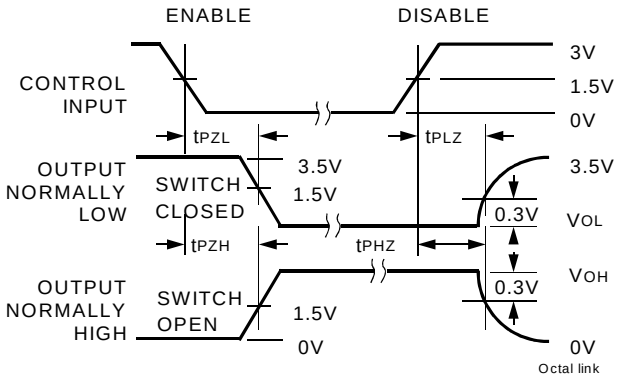
ENABLE AND DISABLE TIMES



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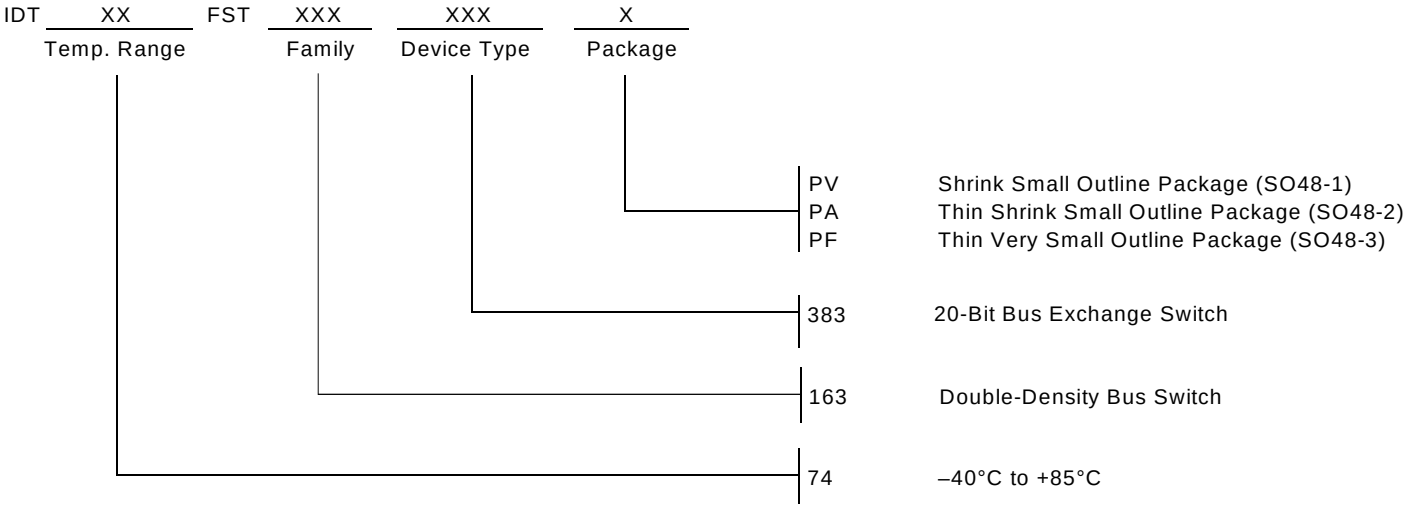
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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