HIGH-SPEED CMOS 8-BIT BUS INTERFACE REGISTER TRANSCEIVER

IDTQS74FCT2652T/AT

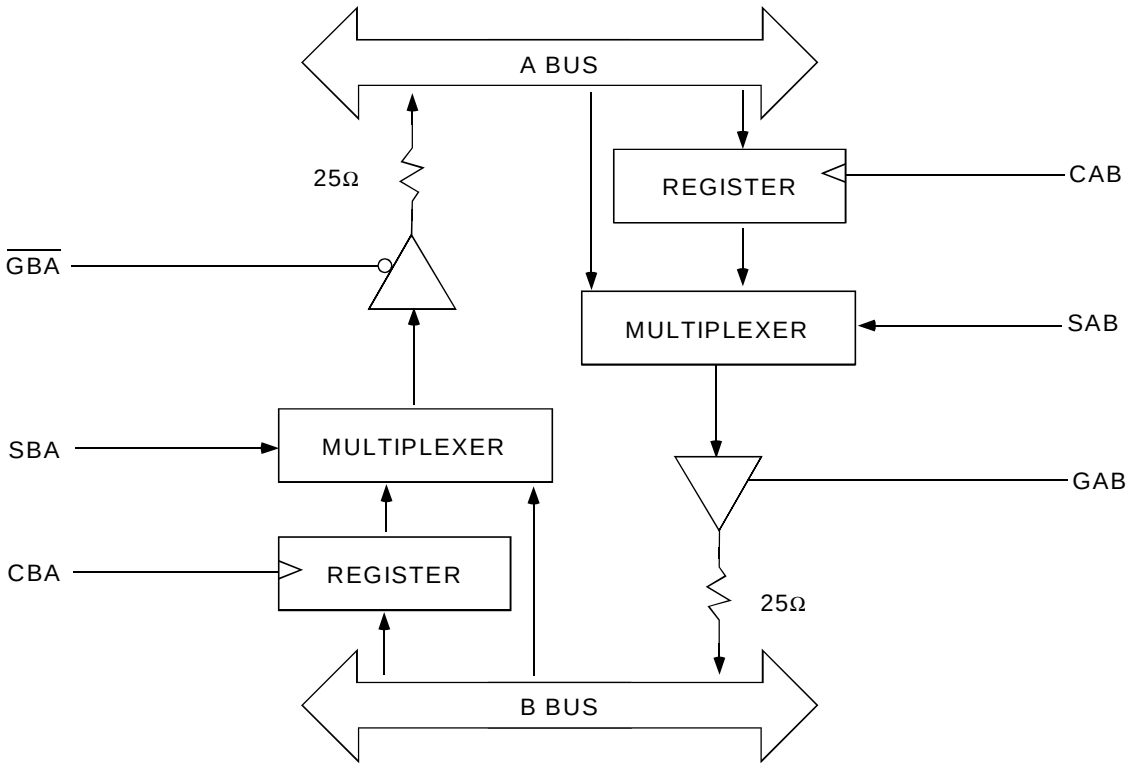
FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. and A speed grades
- I_{OL} = 12mA
- Available in SOIC and QSOP packages

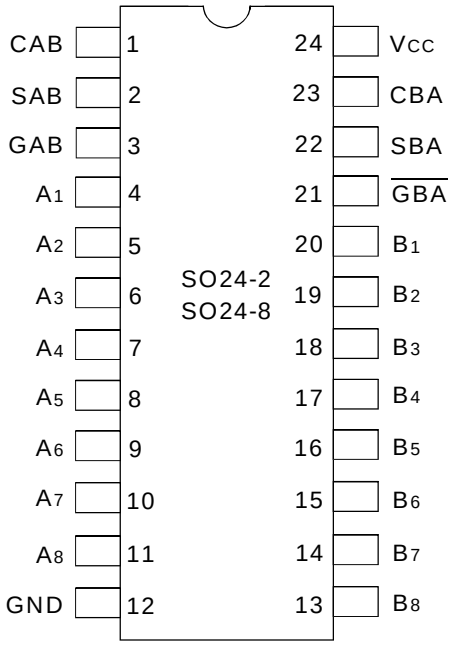
DESCRIPTION:

The IDTQS74FCT2652T is an 8-bit high-speed CMOS TTL-compatible registered bus transceiver with 3-state outputs and a 25Ω resistor, useful for driving transmission lines and reducing system noise. The 2652 series parts can replace the 652 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +7	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current Max Sink Current/Pin	120	mA
I_{IK}	Input Diode Current, $V_{IN} < 0$	– 20	mA
I_{OK}	Output Diode Current, $V_{OUT} < 0$	– 50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	—	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	—	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
Ax	I/O	Side A Inputs or 3-State Outputs
Bx	I/O	Side B Inputs or 3-State Outputs
CAB	I	Clock A to Register
CBA	I	Clock B to Register
SAB	I	A Bus or Reg to B
SBA	I	B Bus or Reg to A
GAB	I	Enable A to B
$\overline{GBA}$	I	Enable B to A

FUNCTION TABLE (1)

Inputs						Outputs		
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	Ax	Bx	Function
L	H	—	—	—	—	Z	Z	Disabled
L	L	—	—	—	—	A	Z	Output A
H	H	—	—	—	—	Z	B	Output B
H	L	—	—	—	—	A	B	Output A and B
—	—	↑	—	—	—	—	—	Load A Register
—	—	—	↑	—	—	—	—	Load B Register
—	—	—	—	L	—	—	—	A Bus to B Bus
—	—	—	—	H	—	—	—	A Reg to B Bus
—	—	—	—	—	L	—	—	B Bus to A Bus
—	—	—	—	—	H	—	—	B Reg to A Bus

NOTE:
1. H = HIGH
   L = LOW
   ↑ = LOW-to-HIGH Transition
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	V_{TLH} - V_{THL} for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	0 ≤ V_{IN} < Vcc	—	—	±5	µA
I_{IL}	Input LOW Current						
I_{OZ}	Off-State Output Current (Hi-Z)	V_{CC} = Max.	0 ≤ V_{IN} ≤ Vcc	—	—	±5	µA
I_{OR}	Current Drive	V_{CC} = Max., V_{OUT} = 2.0V(2)		50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25° C(2)		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -15mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12mA	—	—	0.5	V
R_{OUT}	Output Resistance	V_{CC} = Min.	I_{OL} = 12mA	20	28	40	Ω

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. These parameters are guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. freq = 0 $0V \le V_{IN} \le 0.2V$ or $Vcc-0.2V \le V_{IN} \le Vcc$	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[2] freq = 0	—	2	mA
I_{CCD}	Supply Current per Input per MHz	V_{CC} = Max. Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or Vcc[3,4]	—	0.25	mA/MHz

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NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input (V_{IN} = 3.4V).
3. For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

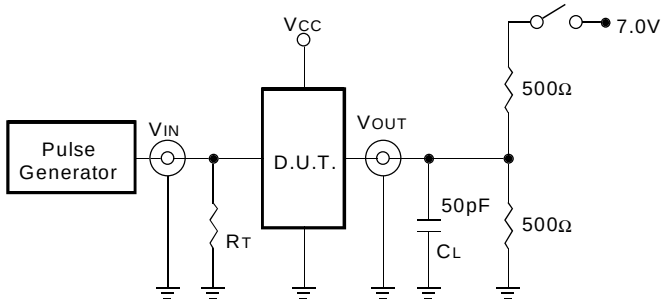
SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

Symbol	Parameter	74FCT2652T		74FCT2652AT		Unit
		Min.	Max.	Min.	Max.	
t_{PHLB} t_{PLHB}	Bus to Bus Delay [2]	2	9	2	6.3	ns
t_{PZH} t_{PZL}	Output Enable Time [2]	2	10	2	9.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time [2]	2	9	2	6.3	ns
t_{PHLC} t_{PLHC}	Clock to Bus Delay [2]	2	9	2	6.3	ns
t_{PHLS} t_{PLHS}	SBA/SAB to Bus Delay [2]	2	11	2	7.7	ns
t_{SU}	Data Setup Time	4	—	2	—	ns
t_H	Data Hold Time	2	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW [3]	6	—	5	—	ns

NOTES:
1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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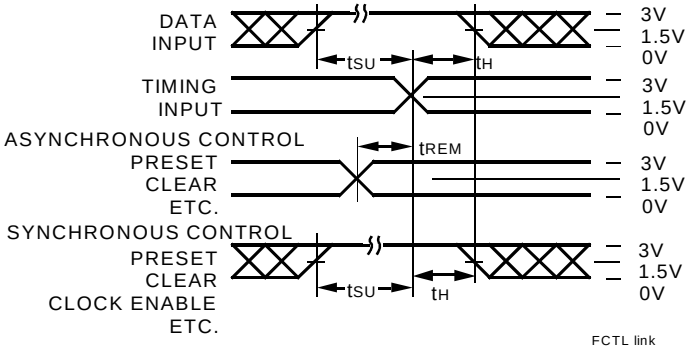
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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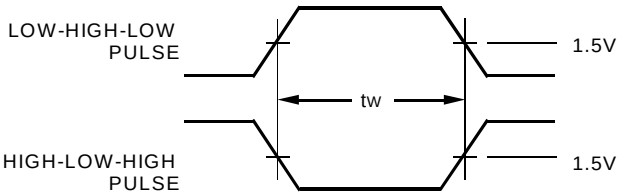
PULSE WIDTH



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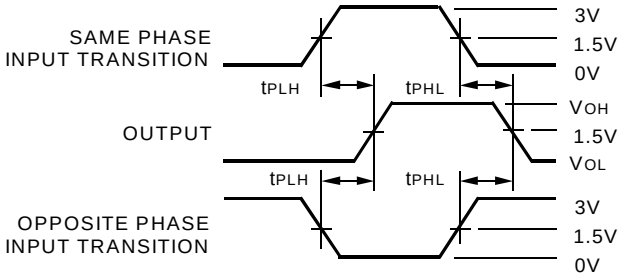
PROPAGATION DELAY



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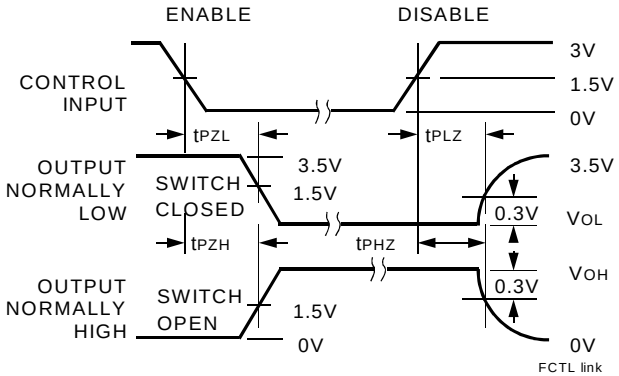
ENABLE AND DISABLE TIMES



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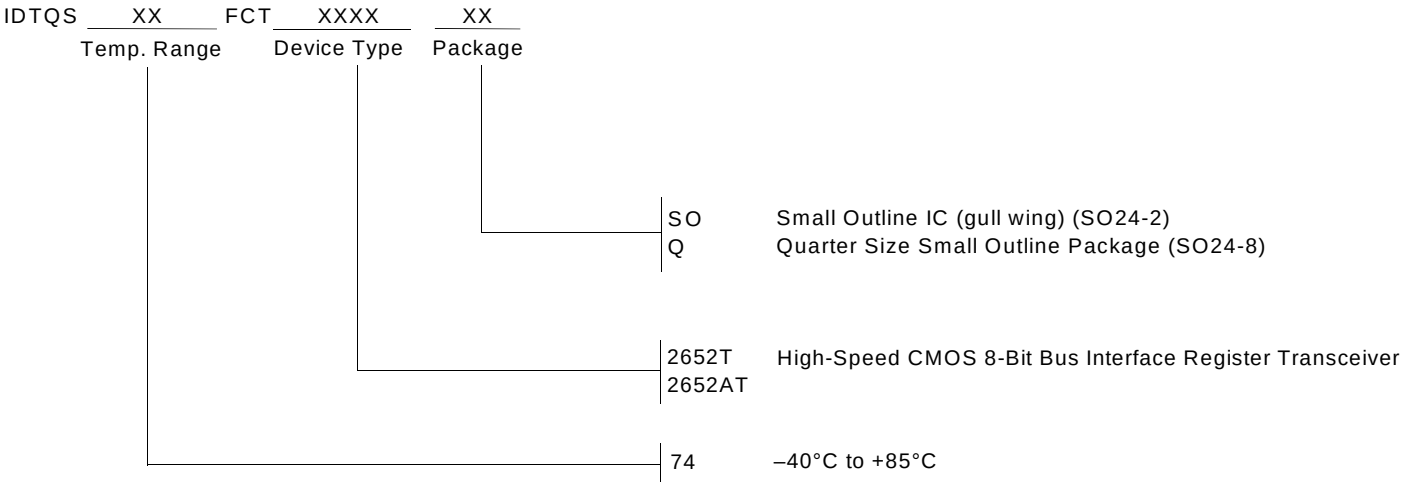
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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