



HIGH-SPEED CMOS 8-INPUT MULTIPLEXER

IDTQS74FCT251AT

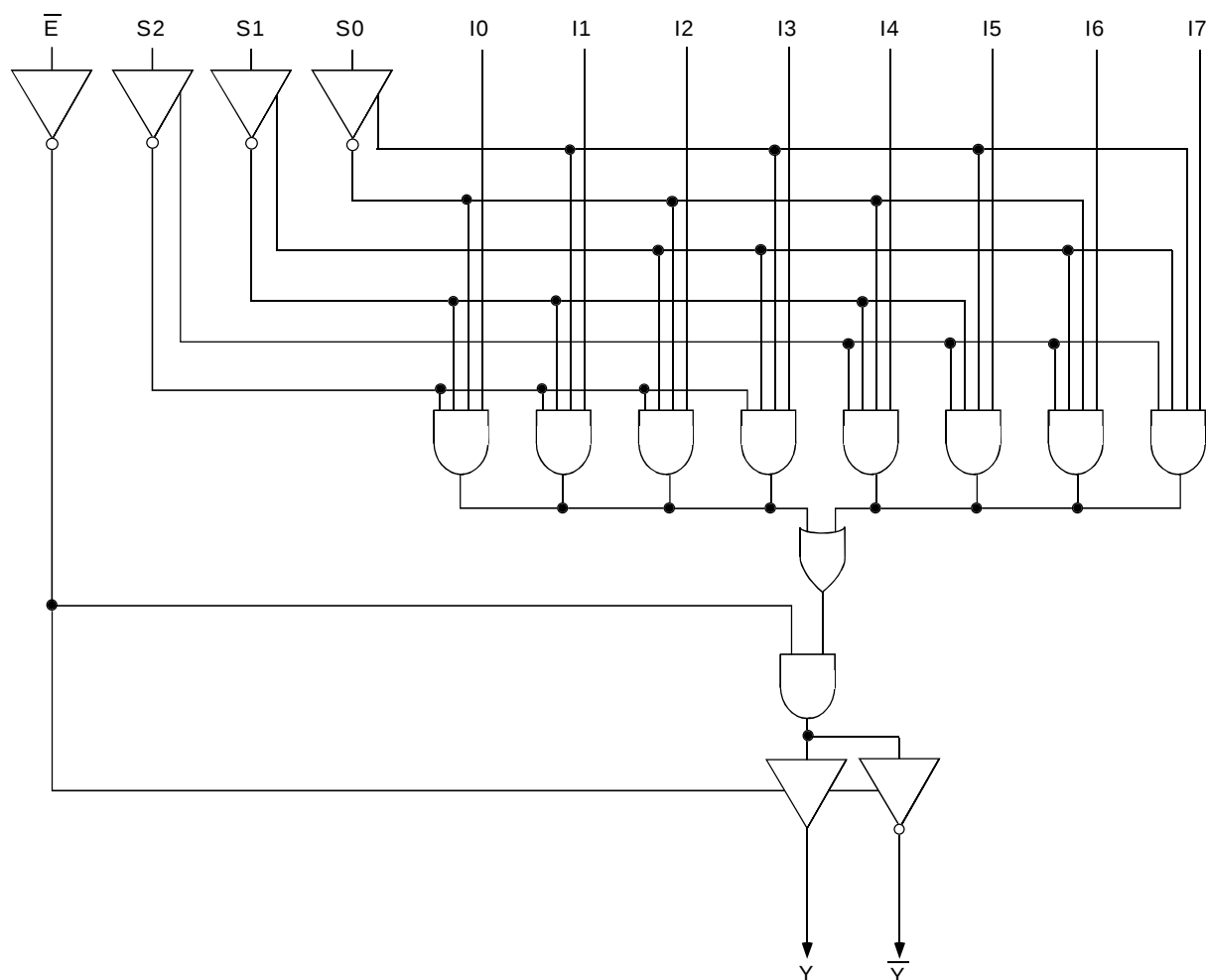
FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- $I_{OL} = 48\text{mA}$
- Available in SOIC and QSOP packages

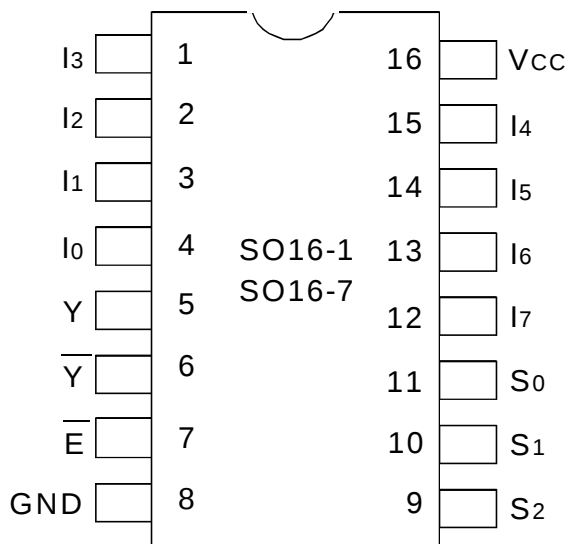
DESCRIPTION:

The IDTQS74FCT251T is a high-speed CMOS TTL-compatible 8-input multiplexer with 3-state outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +7	V
T _{STG}	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current Max Sink Current/Pin	120	mA
I _{IK}	Input Diode Current, V _{IN} < 0	– 20	mA
I _{OK}	Output Diode Current, V _{OUT} < 0	– 50	mA

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN} ⁽²⁾	Input Capacitance	V _{IN} = 0V	4	—	pF
C _{IN} ⁽³⁾	Input Capacitance	V _{IN} = 0V	8	—	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	—	pF

NOTES:

- This parameter is measured at characterization but not tested.
- Pins 1-3, 10, 11, 13-15.
- Pins 4, 7, 9, 12.

PIN DESCRIPTION

Pin Names	I/O	Description
I _x	I	Data In
S _x	I	Select
$\bar{E}$	I	Enable
Y, $\bar{Y}$	O	Data Out

FUNCTION TABLE ⁽¹⁾

$\bar{E}$	Select			Outputs		Function
	S2	S1	S0	Y	$\bar{Y}$	
H	X	X	X	Z	Z	Disable
L	L	L	L	I ₀	$\bar{I}_0$	S2-0 = 0
L	L	L	H	I ₁	$\bar{I}_1$	S2-0 = 1
L	L	H	L	I ₂	$\bar{I}_2$	S2-0 = 2
L	L	H	H	I ₃	$\bar{I}_3$	S2-0 = 3
L	H	L	L	I ₄	$\bar{I}_4$	S2-0 = 4
L	H	L	H	I ₅	$\bar{I}_5$	S2-0 = 5
L	H	H	L	I ₆	$\bar{I}_6$	S2-0 = 6
L	H	H	H	I ₇	$\bar{I}_7$	S2-0 = 7

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedence

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} < V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current						
I_{OZ}	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	± 5	μA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_{OUT} = \text{GND}^{(2)}$		-60	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$, $T_A = 25^{\circ}\text{C}^{(2)}$		—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 48\text{mA}$	—	—	0.5	V

NOTES:

- Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = 25^{\circ}\text{C}$.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ freq = 0	—	2	mA
I_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

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NOTES:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$).
- For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

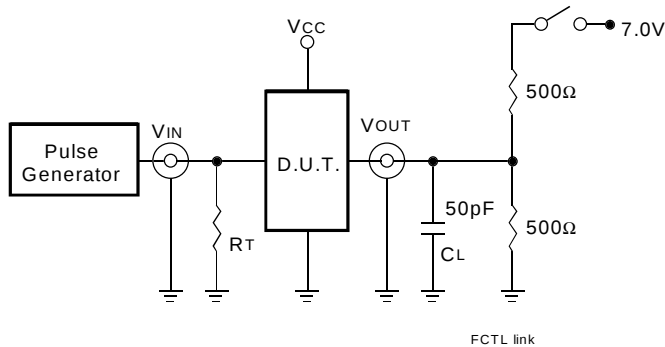
Symbol	Parameter⁽²⁾	Min.	Max.	Unit
t _{LY}	Propagation Delay In to Y or $\bar{Y}$	1.5	5.2	ns
t _{SY}	Propagation Delay Sn to Y or $\bar{Y}$	1.5	6.6	ns
t _{PZH} t _{PZL}	Output Enable Time $\bar{E}$ to Yx or $\bar{Y}$	1.5	6	ns
t _{PHZ} t _{PLZ}	Output Enable Time $\bar{E}$ to Yx or $\bar{Y}$ ⁽³⁾	1.5	6	ns

NOTES:

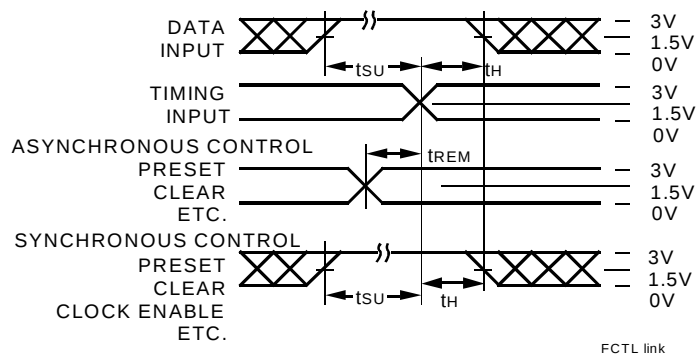
1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

TEST CIRCUITS AND WAVEFORMS

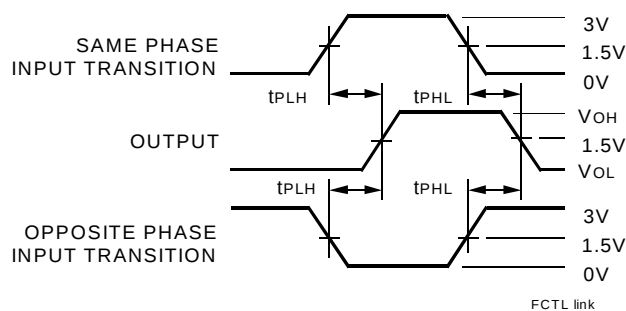
TEST CIRCUITS FOR ALL OUTPUTS



SET-UP, HOLD, AND RELEASE TIMES



PROPAGATION DELAY



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

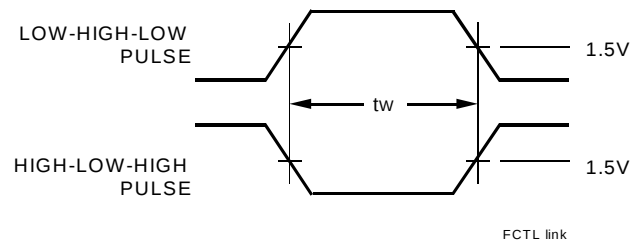
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DEFINITIONS:

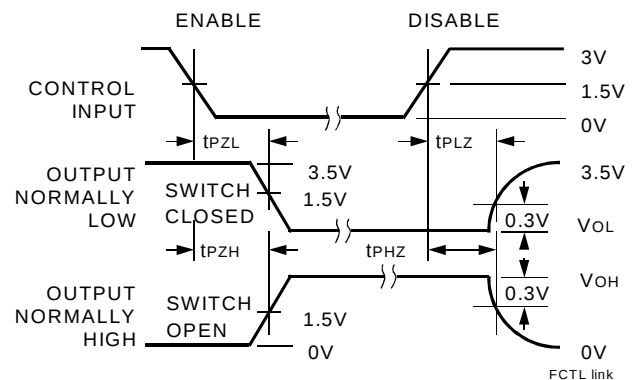
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

PULSE WIDTH



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $Z_o \leq 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDTQS	XX	FCT	XXXX	XX	
Temp. Range			Device Type	Package	
				SO	Small Outline IC (gull wing) (SO16-1)
				Q	Quarter Size Small Outline Package (SO16-7)
			251AT		High-Speed CMOS 8-Input Multiplexer
				74	−40°C to +85°C



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