



HIGH-SPEED CMOS QUAD 2-INPUT MULTIPLEXER

IDTQS74FCT2157AT/CT

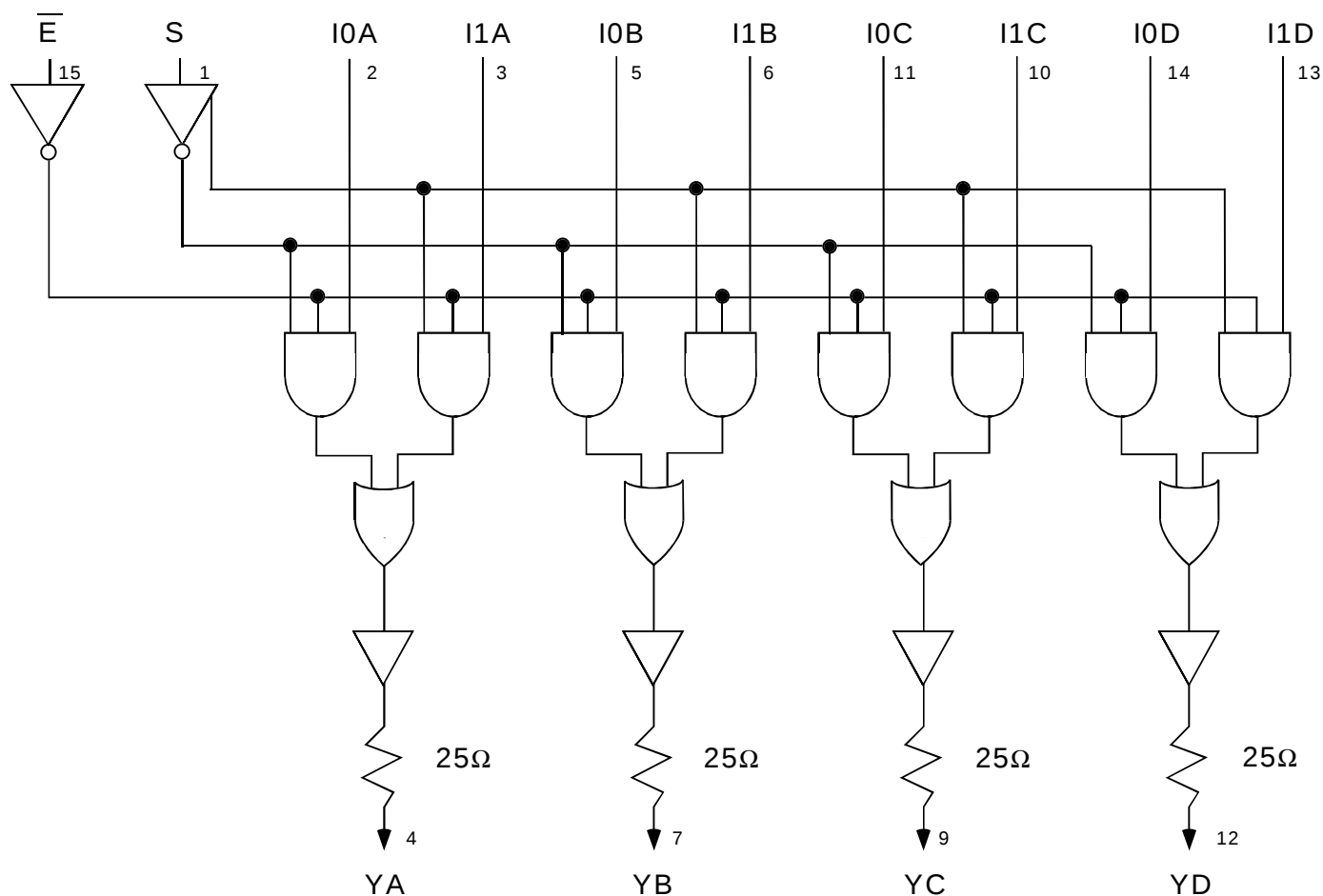
FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25 Ω series resistor outputs reduce reflection and other system noise
- A and C speed grades with 4.3ns for C
- $I_{OL} = 12\text{mA}$
- Available in SOIC, QSOP, and S1 packages

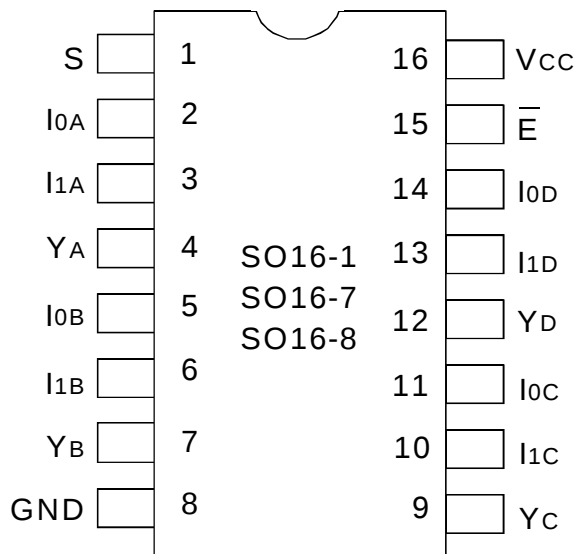
DESCRIPTION:

The IDTQS74FCT2157T is a high-speed CMOS TTL-compatible, quad, 2-input multiplexer with a 25 Ω resistor output, useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP/ S1
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +7	V
T _{STG}	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current Max Sink Current/Pin	120	mA
I _{IK}	Input Diode Current, V _{IN} < 0	– 20	mA
I _{OK}	Output Diode Current, V _{OUT} < 0	– 50	mA

FCTL

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4	—	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	—	pF

FCT_2

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I0A - I0D	Data Inputs
I1A - I1D	Data Inputs
$\bar{E}$	Enable Input (Active LOW)
S	Select Input
YA - YD	Outputs

FUNCTION TABLE⁽¹⁾

Inputs						Function
$\bar{E}$	S	YA	YB	YC	YD	
H	X	L	L	L	L	Disable
L	L	I0A	I0B	I0C	I0D	Select 0
L	H	I1A	I1B	I1C	I1D	Select 1

NOTE:

- H = High Voltage Level
X = Don't Care
L = Low Voltage Level

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs	—	0.2	—	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $0 \leq V_{IN} < V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current					
I_{OR}	Current Drive	$V_{CC} = \text{Max.}$, $V_{OUT} = 2V^{(2)}$	50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$, $T_A = 25^{\circ}\text{C}^{(2)}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$	—	—	0.5	V
R_{OUT}	Output Resistance	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$	20	28	40	Ω

NOTES:

1. Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = 25^{\circ}\text{C}$.
2. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ freq = 0	—	2	mA
I_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

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NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$).
3. For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4\text{V})$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Output Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Following Conditions Apply Unless Otherwise Specified:

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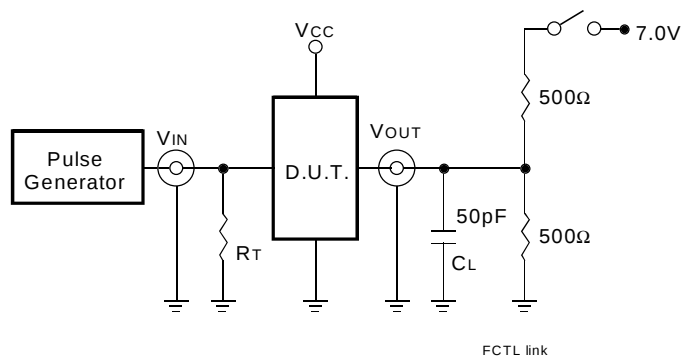
Symbol	Parameter	74FCT2157AT		74FCT2157CT		Unit
		Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay I _{xx} to Y _x	1.5	5	1.5	4.3	ns
t _{PLH} t _{PHL}	Propagation Delay S to Y _x	1.5	7	1.5	5.2	ns
t _{PLH} t _{PHL}	Propagation Delay $\bar{E}$ to Y _x	1.5	6	1.5	4.8	ns

NOTE:

1. $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

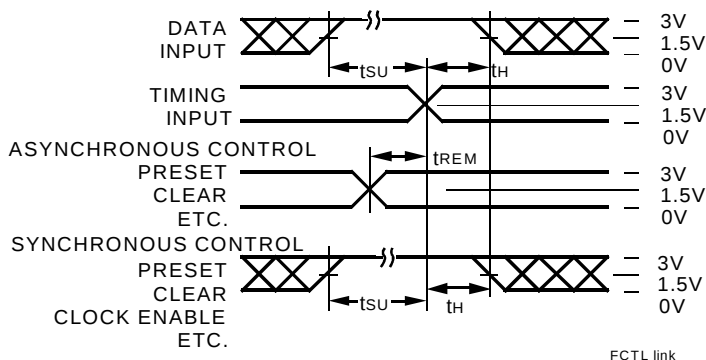
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

DEFINITIONS:

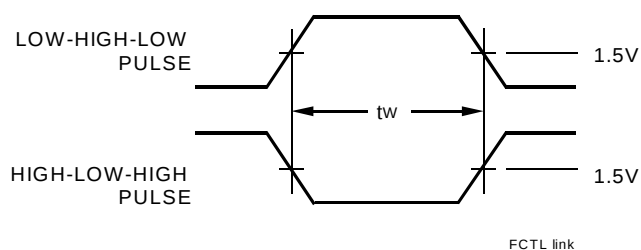
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

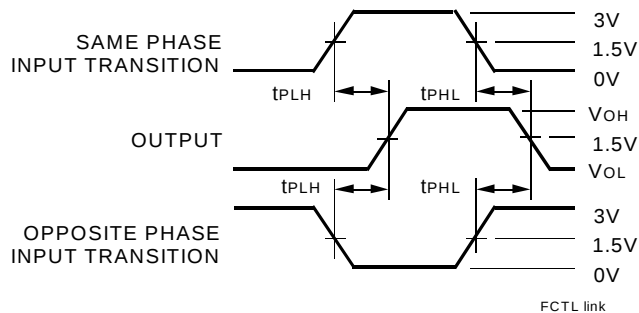
SET-UP, HOLD, AND RELEASE TIMES



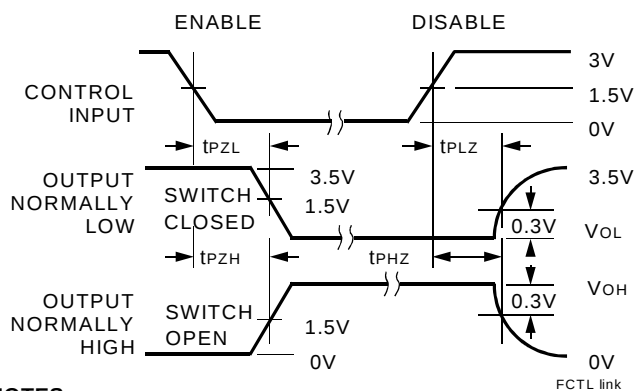
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION

IDTQS	XX	FCT	XXXX	XX	
	Temp. Range		Device Type	Package	
				SO	Small Outline IC (gull wing) (SO16-1)
				Q	Quarter Size Small Outline Package (SO16-7)
				S1	Small Outline IC (gull wing) (SO16-8)
			2157AT 2157CT		High-Speed CMOS Quad 2-Input Multiplexer
				74	−40°C to +85°C



CORPORATE HEADQUARTERS

2975 Stender Way
Santa Clara, CA 95054

for SALES:

800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

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